PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Book IC02a 1988

Video and associated systems

Bipolar, MOS

Types MAB8031AH to TDA 1524A

VIDEO AND ASSOCIATED SYSTEMS
BIPOLAR, MOS
Types MAB8031AH to TDA1524A

SELECTION GUIDE

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Extended temperature range: −40 to + 85 °C.
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NUMERICAL INDEX

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MAF80A39HLP	128	–	ROM-less version of MAB8049H; automotive temperature; reduced frequency	DIL-40; SOT-129	43
MAF8040HLP	256	–	ROM-less version of MAB8050H; extended temperature	DIL-40; SOT-129	43
MAF80A40HLP	256	–	ROM-less version of MAB8050H; automotive temperature; reduced frequency	DIL-40; SOT-129	43
MAF8048HP	64	1K	like MAB8048H; extended temperature	DIL-40; SOT-129	43
MAF80A48HP	64	1K	like MAB8048H; automotive temperature; reduced frequency	DIL-40; SOT-129	43
MAF8049HP	128	2K	like MAB8049H; extended temperature	DIL-40; SOT-129	43
MAF80A49HP	128	2K	like MAB8049H; automotive temperature; reduced frequency	DIL-40; SOT-129	43
MAF8050HP	256	4K	like MAB8050H; extended temperature	DIL-40; SOT-129	43
MAF80A50HP	256	4K	like MAB8050H; automotive temperature; reduced frequency	DIL-40; SOT-129	43
MAF8051AHP	128	4K	like MAB8051AH; extended temperature	DIL-40; SOT-129	39
MAF8051AHWP	128	4K	like MAB8051AH; extended temperature	PLCC-44; SOT-187	39
MAF80A51AHP	128	4K	like MAB8051AH; automotive temperature; reduced frequency	DIL-40; SOT-129	39
MAF80A51AHWP	128	4K	like MAB8051AH; automotive temperature; reduced frequency	PLCC-44; SOT-187	39
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MAF8411P	64	1K	plus 8-bit LED driver; extended temperature	DIL-28; SOT-117	45
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Operating temperature range: 0 to 70 °C.
Extended temperature range: −40 to + 85 °C.
Automotive temperature range: −40 to + 110 °C.

type description	RAM	ROM	description	package code	page
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MAF8422P	64	2K	plus 8-bit LED driver; extended temperature	DIL-20; SOT-146	47
MAF84A22P	64	2K	plus 8-bit LED driver; automotive temperature; reduced frequency	DIL-20; SOT-146	47
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MAF84A41P	128	4K	plus 8-bit LED driver; automotive temperature; reduced frequency	DIL-28; SOT-117	45
MAF8442P	128	4K	plus 8-bit LED driver; extended temperature	DIL-20; SOT-146	47
MAF84A42P	128	4K	plus 8-bit LED driver; automotive temperature; reduced frequency	DIL-20; SOT-146	47
MAF8461P	128	6K	plus 8-bit LED driver; extended temperature	DIL-28; SOT-117	45
MAF84A61P	128	6K	plus 8-bit LED driver; automotive temperature; reduced frequency	DIL-28; SOT-117	45
PCB80C31 BHP-3	128	–	ROM-less version of PCB80C51BH-3	DIL-40; SOT-129	49
PCB80C31 BHWP-3	128	–	ROM-less version of PCB80C51BH-3	PLCC-44; SOT-187	49
PCB80C39P	128	–	ROM-less version of PCB80C49	DIL-40; SOT-128	51
PCB80C39WP	128	–	ROM-less version of PCB80C49	PLCC-44; SOT-187	51
PCB80C49P	128	2K	mask programmable ROM	DIL-40; SOT-129	51
PCB80C49WP	128	2K	mask programmable ROM	PLCC-44; SOT-187	51
PCB80C51 BHP-3	128	4K	mask-programmable ROM	DIL-40; SOT-129	49
PCB80C51 BHWP-3	128	4K	mask-programmable ROM	PLCC-44; SOT-187	49
PCB80C552WP	256	–	ROM-less version of PCB83C552	PLCC-68; SOT-188	53
PCB80C652P	256	–	ROM-less version of PCB83C652	DIL-40; SOT-129	55
PCB80C652WP	256	–	ROM-less version of PCB83C652	PLCC-44; SOT-187	55
PCB80C654H	256	–	ROM-less version of PCB83C654	QFD-44; SOT-205A	57
PCB80C654P	256	–	ROM-less version of PCB83C654	DIL-40; SOT-129	57
PCB80C654WP	256	–	ROM-less version of PCB83C654	PLCC-44; SOT-187	57
PCB83C552WP	256	8K	plus I^2C bus hardware	PLCC-68; SOT-188	53
PCB83C652P	256	8K	plus I^2C bus hardware	DIL-40; SOT-129	55
PCB83C652WP	256	8K	plus I^2C bus hardware	PLCC-44; SOT-187	55
PCB83C654H	256	8K	plus I^2C bus hardware	QFD-44; SOT-205A	57
PCB83C654P	256	8K	plus I^2C bus hardware	DIL-40; SOT-129	57
PCB83C654WP	256	8K	plus I^2C bus hardware	PLCC-44; SOT-187	57
PCF80C31 BHP-3	128	–	ROM-less version of PCB80C51BH-3 extended temperature	DIL-40; SOT-129	49

Operating temperature range: 0 to 70 °C.
Extended temperature range: −40 to + 85 °C.
Automotive temperature range: −40 to + 110 °C.

type number	RAM	ROM	description	package code	page
SINGLE-CHIP 8-BIT MICROCONTROLLERS (continued)					
PCF80CA31 BHP-3	128	–	ROM-less version of PCB80C51BH-3 extended temperature	DIL-40; SOT-129	49
PCF80C31 BHWP-3	128	–	ROM-less version of PCB80C51BH-3 extended temperature	PLCC-44; SOT-187A	49
PCF80CA31 BHWP	128	–	ROM-less version of PCB80C51BH-3 automotive temperature	PLCC-44; SOT-187A	49
PCF80C39P	128	–	ROM-less version of PCB80C49; extended temperature	DIL-40; SOT-129	51
PCF80C49P	128	2K	like PCB80C49; extended temperature	DIL-40; SOT-129	51
PCF80C51 BHP-3	128	–	ROM-less version of PCB80C51BH-3 extended temperature	DIL-40; SOT-129	49
PCF80CA51 BHP-3	128	–	ROM-less version of PCB80C51BH-3 extended temperature	DIL-40; SOT-129	49
PCF80C51 BHWP-3	128	–	ROM-less version of PCB80C51BH-3 extended temperature	PLCC-44; SOT-187A	49
PCF80CA51 BHWP-3	128	–	ROM-less version of PCB80C51BH-3 automotive temperature	PLCC-44; SOT-187A	49
PCF84C00B	256	–	bond-out version PCF84CXX family	28/28 Piggy-back	67
PCF84C00T	256	–	bond-out version PCF84CXX family	VSO-56; SOT-190	67
PCF84C12P	64	1K	extended temperature	DIL-20; SOT-146	69
PCF84C12T	64	1K	extended temperature	SO-20; SOT-163A	69
PCF84C21P	64	2K	extended temperature	DIL-28; SOT-117	67
PCF84C21T	64	2K	extended temperature	SO-28; SOT-136A	67
PCF84C41P	128	4K	bond-out version PCF84CXX	DIL-28; SOT-117	67
PCF84C41T	128	4K	bond-out version PCF84CXX	SO-28; SOT-136A	67
PCF84C81P	256	8K	extended temperature	DIL-28; SOT-117	67
PCF84C81T	256	8K	extended temperature	SO-28; SOT-136A	67

MAINTENANCE TYPE LIST

The types listed below are not included in this handbook. Detailed information will be supplied on request.

SAA1056P	PLL frequency synthesizer
SAA1061	LED driver/output port expander
SAA1082	remote transmitter
SAA3027	infrared remote control transmitter
SAA5020	teletext timing chain circuit (625 lines)
SAA5025D	teletext timing chain for USA 525 line system (USTIC); 40 characters per row, 24 rows (8 TV lines per row)
SAA5030	teletext video processor
SAA5040A	teletext acquisition and control circuit; giving boxed status information for display
SAA5040B	teletext acquisition and control circuit; without status box
SAA5040C	teletext acquisition and control circuit; giving different boxed status information for display
SAA5041	teletext acquisition and control circuit; different remote control commands
SAA5042	teletext acquisition and control circuit; different remote control commands
SAA5043	teletext acquisition and control circuit; different boxed status information for display
SAA5045	gearing and address logic array (GALA) for USA teletext; 525 line system
SAA5050	teletext character generator (English)
SAA5051	teletext character generator (German)
SAA5052	teletext character generator (Swedish)
SAA5053	teletext character generator (Italian)
SAA5054	teletext character generator (Belgian)
SAA5055	teletext character generator (US ASCII)
SAA5056	teletext character generator (Hebrew)
SAA5057	teletext character generator (Cyrillic)
SAA5058	teletext character generator (African)
SAA5070	peripheral IC for viewdata (LUCY); μC controlled
SAA5230	teletext video processor
SAA9010	picture enhancement processor
SAA9020	field memory controller
SAB3034	analogue and timing circuit (A & T)
SAF3019	clock/timer with serial I/O; μC controlled
TDA2502	tacho motor speed controller
TDA2503	track sensing amplifier for VCR
TDA3540; Q	IF amplifier and demodulator; npn tuners
TDA3541; Q	IF amplifier and demodulator; pnp tuners
TDA3571B	sync combination with transmitter identification
TDA3576B	sync combination with transmitter identification

TDA3590	SECAM processor circuit	(successor TDA3590A)
TDA3591	SECAM processor circuit	(successor TDA3591A)
TDA3650	vertical deflection circuit	
TDA3701	PAL sync processor for VCR	
TDA3710	chrominance signal/mixer for VCR	
TDA3720	SECAM processor for VCR	(successor TDA3725)
TEA1002	PAL colour encoder and video summer	(successor TEA2000)

GENERAL

Type designation
Rating systems
Handling MOS devices

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic type number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 3).

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit }
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.
3. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line
W : Lead chip-carrier (LCC)
X : Leadless chip-carrier (LLCC)
Y : Pin grid array (PGA)

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

DEVICE DATA

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8051AH family of single-chip 8-bit microcontrollers is manufactured in an advanced 2 μ NMOS process. The family consists of the following members:

- MAB8031AH: ROM-less version of the MAB8051AH
- MAB8051AH: 4 K bytes mask-programmable ROM, 128 bytes RAM

Both types are available in 8, 10 and 12 MHz versions and 15 MHz for the MAB8031AH. In the following, the generic term "MAB8051AH" is used to refer to both family members.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 K bytes of program memory and/or up to 64 K bytes of data storage.

The MAB8051AH contains a non-volatile 4 K x 8 read-only program memory (not ROM-less version); a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/event counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O power for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and timing circuits. For systems that require extra capability, the MAB8051AH can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of 255 instructions; 44% one-byte, 41% two-byte and 15% three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs. Multiply, divide, subtract and compare are among the many instructions added to the standard MAB8048H instruction set.
For further detailed information see users manual 'Single-chip 8-bit microcontrollers'.

Features

- 4 K x 8 ROM (8051AH only), 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- Full duplex serial port
- External memory expandable to 128 K
- Boolean processing
- 218 bit-addressable locations
- On-chip oscillator
- Five-source interrupt structure with two priority levels
- 58% of instructions executed in 1 μs; multiply and divide in 4 μs (at 12 MHz clock)
- Enhanced architecture with:
  - non-page-oreinted instructions
  - direct addressing
  - four 8-bit register banks
  - stack depth up to 128-bytes
  - multiply, divide, subtract and compare
- Available with extended temperature range: −40 to + 85 °C (MAF8031/51AH)
- Available with automotive temperature range: −40 to + 100 °C (MAF80A31/51AH)

PACKAGE OUTLINES

MAB8031/51AHP; MAF8031/51AHP; MAF80A31/51AHP: 40-lead DIL; plastic (SOT-129).
MAB8031/51AHWP; MAF8031/51AHWP; MAF80A31/51AHWP: 44-lead, plastic leaded-chip-carrier (PLCC); SOT-187.

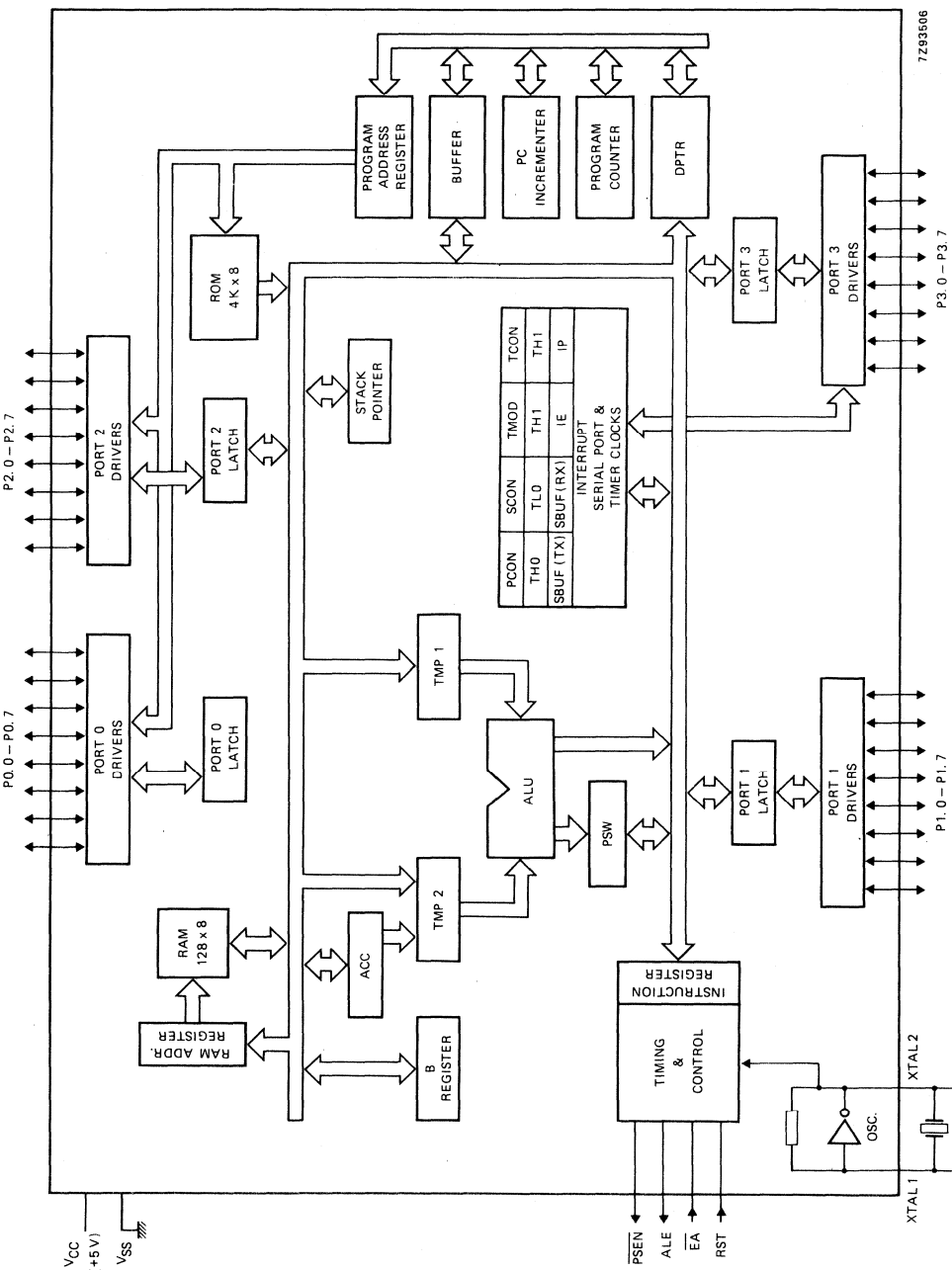


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8052AH is a member of the MAB8051AH family with a higher performance. This single-chip 8-bit microcontroller is manufactured in an advanced 2 μ NMOS process. For this version the following members exist:

- MAB8032AH: ROM-less version of the MAB8052AH
- MAB8052AH: 8 K bytes mask programmable ROM, 256 bytes RAM

Both types are available in 12 MHz versions. In the following, the generic term "MAB8052AH" is used to refer to both family members.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 K bytes of program memory and/or up to 64 K bytes of data storage.

The MAB8052AH contains a non-volatile 8 K x 8 read-only program memory (not ROM-less version); a volatile 256 x 8 read/write data memory; 32 I/O lines; three 16-bit timer/event counters; a six-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and timing circuits. For systems that require extra capability, the MAB8052AH can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of 255 instructions; 44% one-byte, 41% two-byte and 15% three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.
For further detailed information see the '8051' section of the 'Single-chip 8-bit microcontroller user manual'.

Features

- 8 K x 8 ROM (8052AH only), 256 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- Full-duplex serial port
- External memory expandable to 128 K
- Boolean processing
- 218 bit-addressable locations
- On-chip oscillator
- Six-source interrupt structure with two priority levels
- 58% of instructions executed in 1 μs; multiply and divide in 4 μs
- Enhanced architecture with:
  - non-page-oriented instructions
  - direct addressing
  - four 8-bit register banks
  - stack depth up to 128-bytes
  - multiply, divide, substract and compare
- Upward compatible with MAB8031AH/8051AH
- Extended temperature range with frequency from 3,5 to 10 MHz:
  –40 to + 85 °C MAF8052AH
  –40 to + 100 °C MAF80A52AH

PACKAGE OUTLINES

MAB8032/52AHP: 40-lead DIL, plastic (SOT-129).
MAF8032AH/52AH/A32AH/A52AHP: 40-lead DIL, plastic (SOT-129).

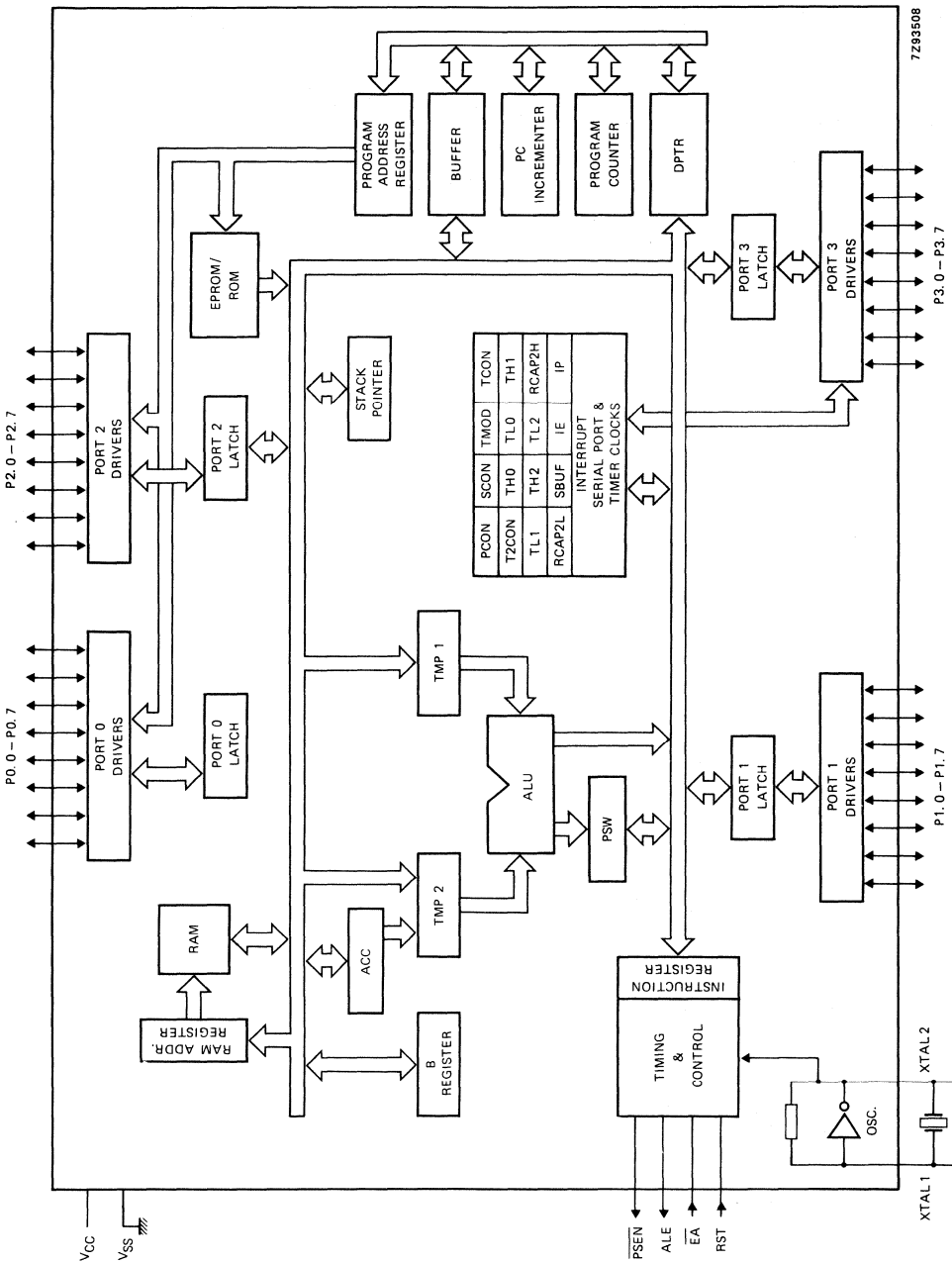


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The MAB80XXH family of single-chip 8-bit microcontrollers is fabricated in NMOS.
Three interchangeable (pin compatible) versions are available:

- MAB8048H: 1 K bytes mask-programmed ROM, 64 bytes RAM
- MAB8035HL: ROM-less version of the MAB8048H
- MAB8049H: 2 K bytes mask-programmed ROM, 128 bytes RAM
- MAB8039HL: ROM-less version of the MAB8049H
- MAB8050H: 4 K bytes mask-programmed ROM, 256 bytes RAM
- MAB8040HL: ROM-less version of the MAB8050H

These microcontrollers are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O lines as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.

An on-chip 8-bit counter is provided, which can count either machine cycles (÷32) or external events. The counter can be used to generate an interrupt to the processor.
Program and data memories plus input/output capabilities can be expanded using standard TTL compatible memories and logic. For more detailed information see the 'single-chip 8-bit micro-controllers' user manual.

Features

- 8-bit CPU, ROM, RAM and I/O
- 8-bit counter/timer
- On-chip oscillator and clock driver circuits
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions 1 or 2 cycles
- Easily expandable memory and 27 I/O lines
- TTL compatible inputs and outputs
- Single 5 V supply
- Standard and extended temperature ranges (see Table 5): MAB80XX: 0 to +70 °C
  MAF80XX: −40 to +85 °C
  MAF80AXX: −40 to +110 °C

Applications

- Peripheral interfaces and controllers
- Test and measuring instruments
- Sequencers
- Modems and data enciphering
- Environmental control systems
- Audio/video systems

PACKAGE OUTLINES

All versions: with type no. suffix P (see Table 5): 40-lead DIL; plastic (SOT-129).
MAB8035/8048/8039/8049 H/HLWP: 44-lead plastic leaded chip-carrier (PLCC); SOT-187.

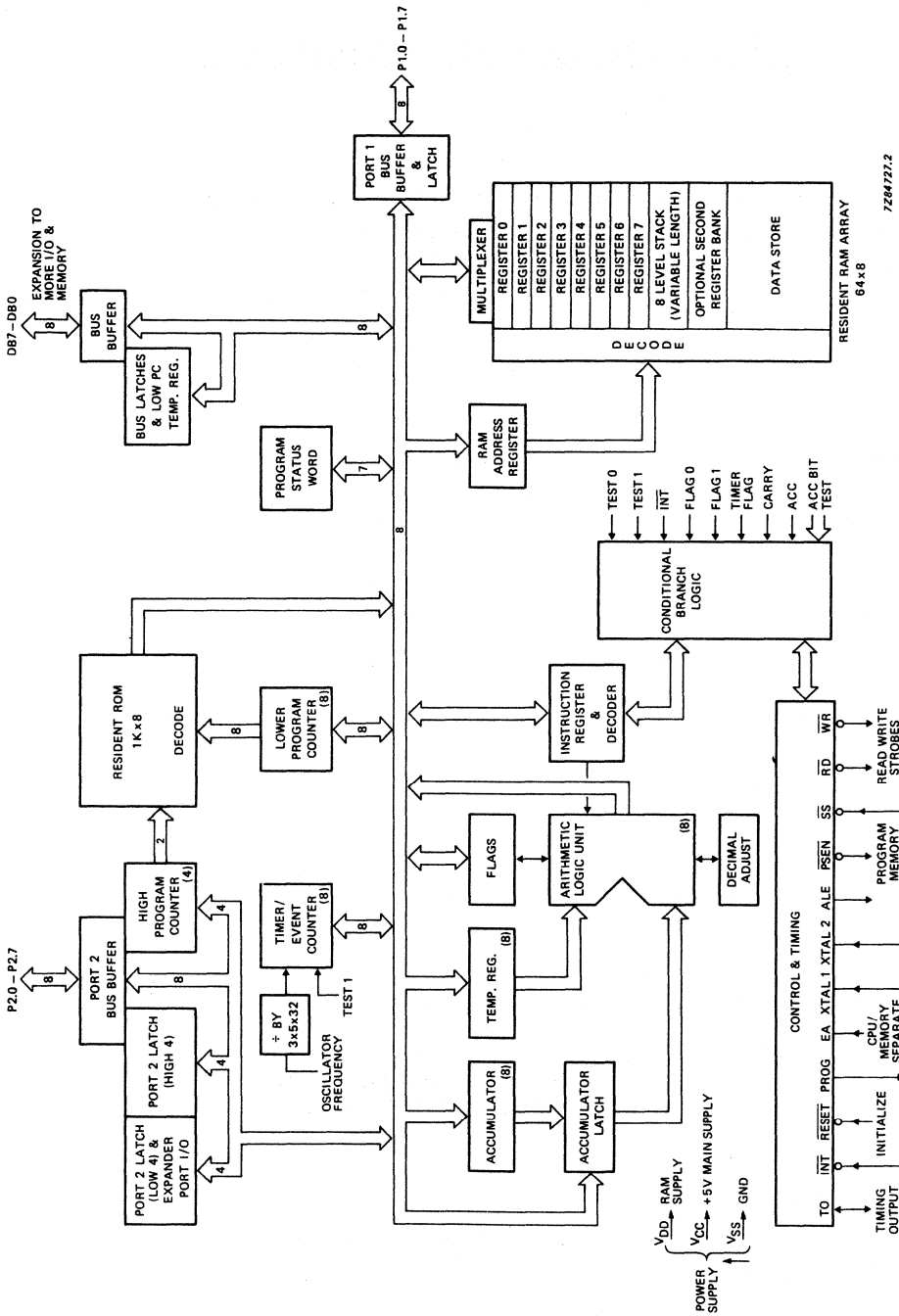


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB84X1 family of microcontrollers is fabricated in NMOS. The family consists of 5 devices:

- MAB8401 — 128 bytes RAM, external program memory, with 8-bit LED-driver (10mA), emulation of MAB/F8422/42* possible
- MAB/MAF8411 — 1K byte ROM/64 bytes RAM plus 8-bit LED-driver
- MAB/MAF8421 — 2K bytes ROM/64 bytes RAM plus 8-bit LED-driver
- MAB/MAF8441 — 4K bytes ROM/128 bytes RAM plus 8-bit LED-driver
- MAB/MAF8461 — 6K bytes ROM/128 bytes RAM plus 8-bit LED-driver

Each version has 20 quasi-bidirectional I/O port lines, one serial I/O line, one single-level vectored interrupt, an 8-bit timer/event counter and on-board clock oscillator and clock circuits. Two 20-pin versions, MAB/F8422 and MAB/F8442* are also available.

This microcontroller family is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048. The microcontrollers have extensive bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the "8-bit Single-chip Microcontrollers user manual".

* See data sheet on MAB/F8422/42.

Features

- 8-bit: CPU, ROM, RAM and I/O in a single 28-lead DIL package
- 1K, 2K, 4K or 6K ROM bytes plus a ROM-less version
- 64 or 128 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two testable inputs: one of which can be used to detect zero cross-over, the other is also the external interrupt input
- Single level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O that can be used in single or multi-master systems (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single 5 V power supply (± 10%)
- Operating temperature ranges:
  - 0 to + 70 °C — MAB84X1 family
  - −40 to + 85 °C — MAF84X1 family only
  - −40 to + 110 °C — MAF84AX1 family only

PACKAGE OUTLINES

MAB8401B: 28-lead 'Piggy-back' package (with up to 28-pin EPROM on top).
MAB8401WP: 68-lead plastic leaded chip-carrier (PLCC) (SOT-188).
MAB/MAF8411/21/41/61P: 28-lead DIL; plastic (SOT-117).
MAF84A11/21/41/61P: 28-lead DIL; plastic (SOT-117).
MAB8411/21/41/61T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

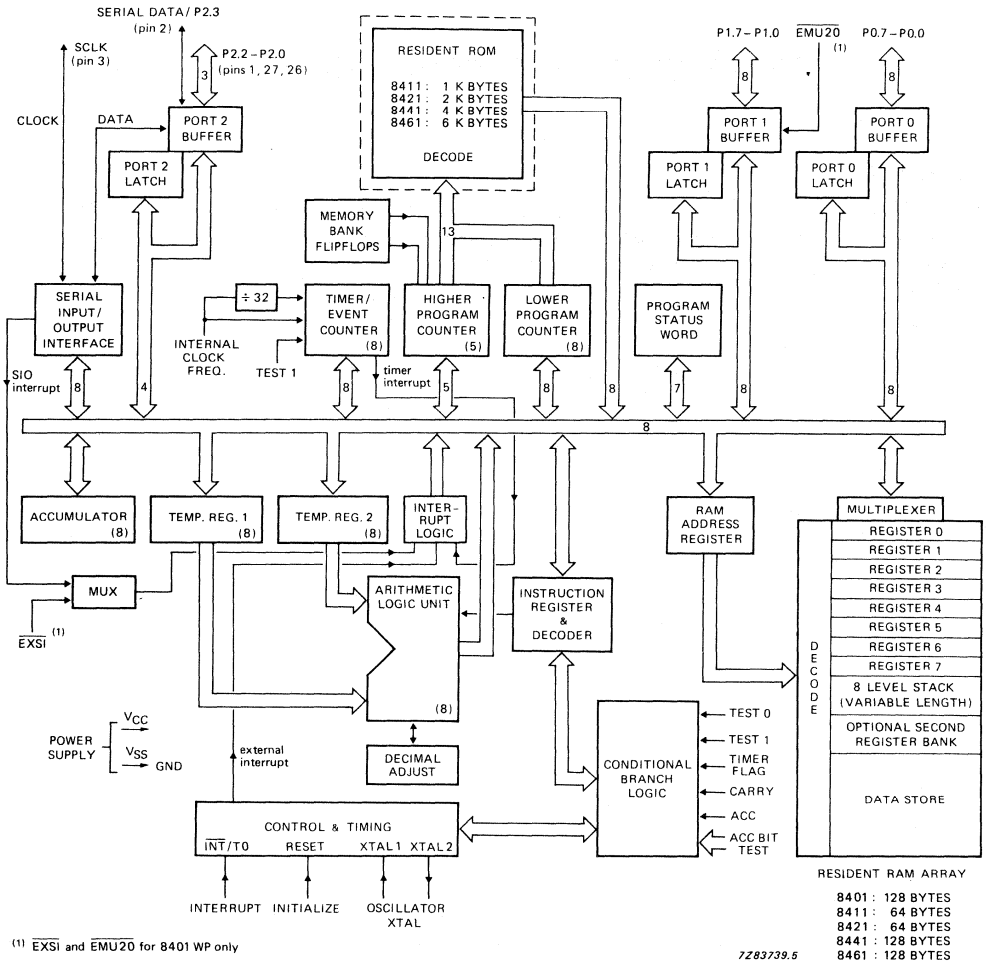


Fig. 4a Block diagram of the MAB84X1 family.

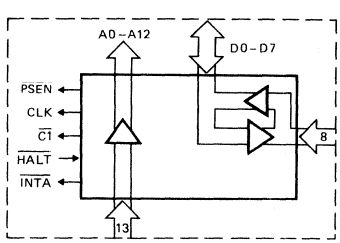


Fig. 4b Replacement for dotted part in Fig. 4a for the MAB8401WP bond-out version.

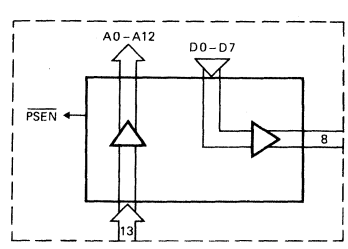


Fig. 4c Replacement of dotted part in Fig. 4a for the MAB8401B 'Piggy-back' version.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8422/8442 is a high-performance microcontroller incorporating dedicated hardware, memory capacity and I/O lines. This dedication means a microcontroller can be economically installed in high-volume products where its main function is control.

The MAB8422/8442 is a 20 pin, single-chip 8-bit microcontroller that has been developed from the 28 pin MAB8421/8441 microcontrollers. The versions are:

- MAB8422 - 2K x 8 ROM/64 bytes RAM
- MAB8442 - 4K x 8 ROM/128 bytes RAM

Each version has 15 I/O port lines comprising one 8-bit parallel port (P0), one 2-bit parallel port (P1.0 and P1.1 that are shared with the serial I/O lines SDA and SCL), one 3-bit parallel port (P2.0 - P2.2) and two input lines ($\overline{INT}$/T0 and T1).

The serial I/O interface is I^2C compatible and therefore the MAB8422/8442 can operate as a slave or a master in single and multi-master systems. Conversion from parallel to serial data when transmitting, and vice versa when receiving, is done mainly in software. There is a minimum of hardware for the serial I/O implemented. This hardware is controlled by the status of the SDA and SCL lines and can be read or written under software control. Standard software for I^2C-bus control is available upon request. For detailed information see the user manual 'Single-chip 8-bit microcontrollers'.

Features

- 8-bit: CPU, ROM, RAM and I/O
- 20 pin package
- MAB8422: 2K x 8 ROM/64 bytes RAM
- MAB8442: 4K x 8 ROM/128 bytes RAM
- 13 quasi-bidirectional I/O port lines
- Two testable inputs T1 and $\overline{INT}$/T0
- High current output on P0 (I_{OL} = 10 mA at V_{OL} = 1 V)
- One interrupt line combined with the testable input line $\overline{INT}$/T0
- Single-level interrupts: external, timer/event counter, serial I/O
- I^2C-compatible serial I/O that can be used in single or multi-master systems (serial I/O data and clock via P1.0 and P1.1 port lines, respectively)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles, cycle time dependent on oscillator frequency
- Single power supply
- Operating temperature ranges: 0 to +70 °C (MAB84X2)
  −40 to +85 °C (MAF84X2)
  −40 to +110 °C (MAF84AX2)

PACKAGE OUTLINES

MAB/MAF84X2, MAF84AX2: 20-lead DIL; plastic (SOT-146).

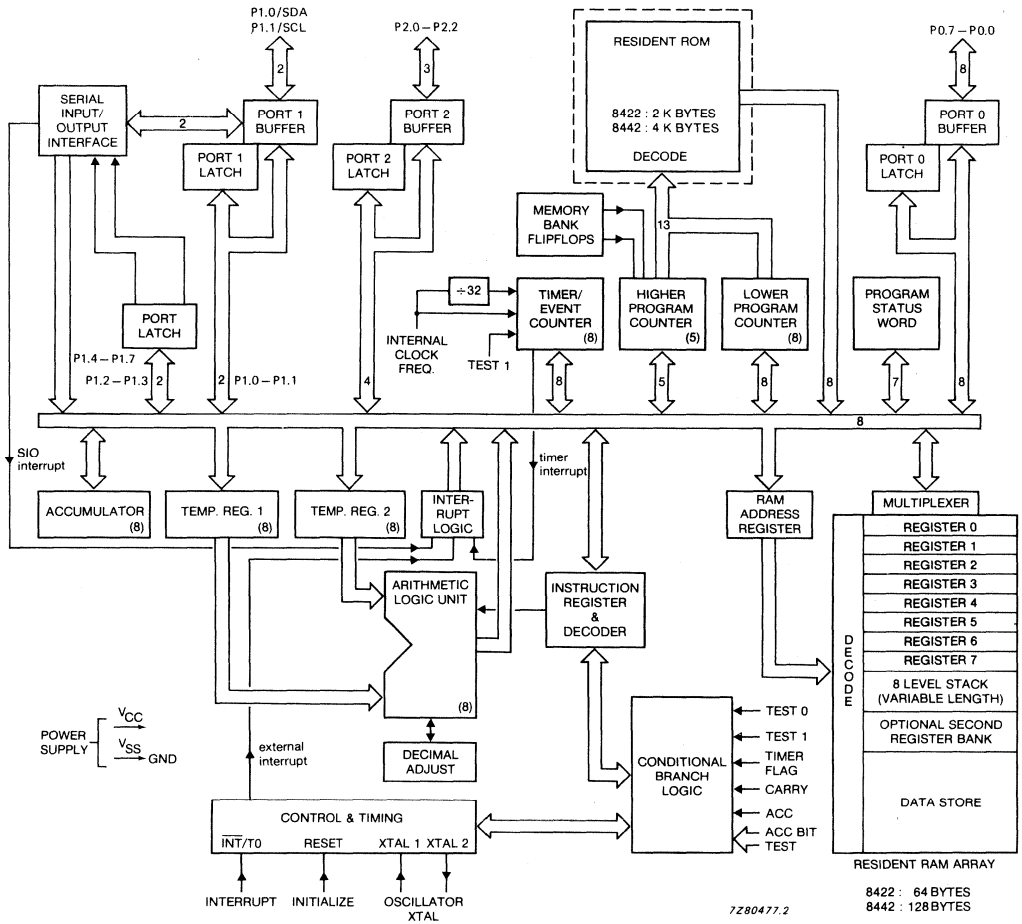


Fig. 1 Block diagram of the MAB8422/8442.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The PCB80C51 family of single-chip 8-bit microcontrollers is manufactured in an advanced CMOS process. The family consists of the following members:

- PCB80C51BH-3: 4 K bytes mask-programmable ROM, 128 bytes RAM
- PCB80C31BH-3: ROM-less version of the PCB80C51BH-3

In the following text, the generic term "PCB80C51BH-3" is used to refer to both family members.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 K bytes of program memory and/or up to 64 K bytes of data memory.

The PCB80C51BH-3 contains a non-volatile 4 K x 8 read-only program memory; a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/event counters; a five-source, two-priority level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB80C51BH-3 can be expanded using standard TTL compatible memories and logic.

The PCB80C51BH-3 has two software selectable modes of reduced activity for further power reduction - Idle and Power-down.
The Idle mode freezes the CPU while allowing the RAM, timers, serial port and interrupt system to continue functioning.
The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

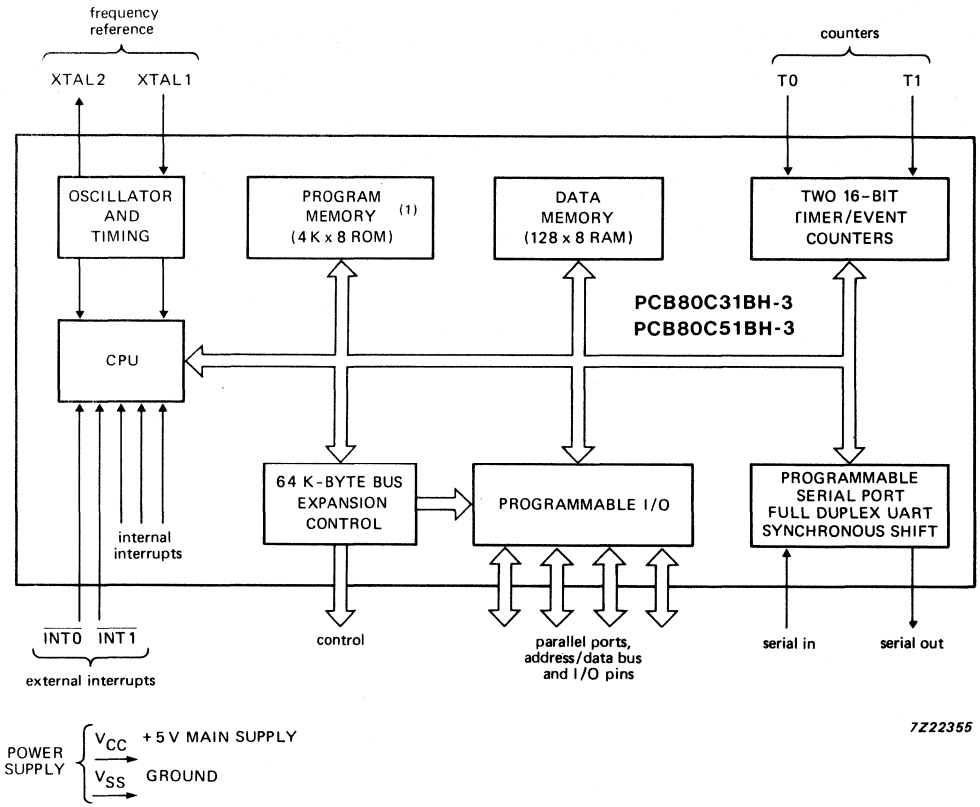
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte and 16 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs. Multiply, divide, subtract and compare are among the many instructions included in the instruction set.
Software development to be announced: PCB85C51 in piggy-back.

Features

- 4 K x 8 ROM (80C51BH-3 only), 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- Full-duplex serial port
- External memory expandable to 128 K, external ROM up to 64 K and/or external RAM up to 64 K
- Boolean processing
- 218 bit-addressable locations
- On-chip oscillator
- Five-source interrupt structure with two priority levels
- With a 12 MHz clock, 58% of the instructions execute in 1 μs; multiply and divide instructions execute in 4 μs; all other instructions execute in 2 μs
- Enhanced architecture with:
  non-page-oriented-instructions
  direct addressing
  four 8-byte + 1-byte register blanks
  stack depth up to 128-bytes
  multiply, divide, subtract and compare instructions
- PCB80C51/C31BH-3
  XTAL frequency range: 1,2 to 16 MHz
  temperature range: 0 °C to + 70 °C
  PCF80C51/C31BH-3
  XTAL frequency range: 1,2 to 12 MHz
  temperature range: −40 °C to + 85 °C
  PCF80CA51/CA31BH-3
  XTAL frequency range: 1,2 to 12 MHz
  temperature range: −40 °C to + 110 °C

PACKAGE OUTLINES

PCB/PCF80C31/51BH-3HP, PCF80CA31/51BH-3P: 40-lead DIL; plastic (SOT-129).
PCB/PCA80C31/51BH-3WP, PCF80CA31/51BH-3WP: 44-lead PLCC; plastic, leaded-chip-carrier (SOT-187).



(1) PCB80C51BH-3 only.

Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT CMOS MICROCONTROLLER

DESCRIPTION

The PC80CXX family of single-chip 8-bit CMOS microcontrollers consists of:

- The PCB80C49 with resident mask programmed 2 K x 8 ROM, 128 x 8 RAM.
- The PCB80C39 without resident program memory for use with external EPROM/ROM, 128 x 8 RAM.

All versions are pin and function compatible to their NMOS counter parts but with additional features and high performance.

The PC80CXX family are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O, and to test individual individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.
An on-chip 8-bit counter is provided, which can count either machine cycles (÷ 32) or external events. The counter can be programmed to cause an interrupt to the processor.
Program and data memories can be expanded using standard devices. Input/output capabilities can be expanded using standard devices.
The family has low power consumption and in addition a power down mode is provided.
For further detailed information see users manual 'single-chip 8-bit microcontrollers'.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 40-pin package
- PCB80C49: 2K x 8 ROM, 128 x 8 RAM
- Internal counter/timer
- Internal oscillator, clock driver
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions: 1 or 2 cycles
- Easily expandable memory and I/O
- TTL compatible inputs and outputs
- Single 5 V supply
- Wide frequency operating range
- Low current consumption
- Also available with extended temperature range; −40 °C to + 85 °C

APPLICATIONS

- Peripheral interfaces and controllers
- Test and measurement instruments
- Sequencers
- Audio/video systems
- Environmental control systems
- Modems and data enciphering

PACKAGE OUTLINES

PCB/F80C39/C49P: 40-lead DIL; plastic (SOT-129).
PCB/F80C39/C49WP: 44-lead plastic leaded chip carrier (PLCC); SOT-187A.

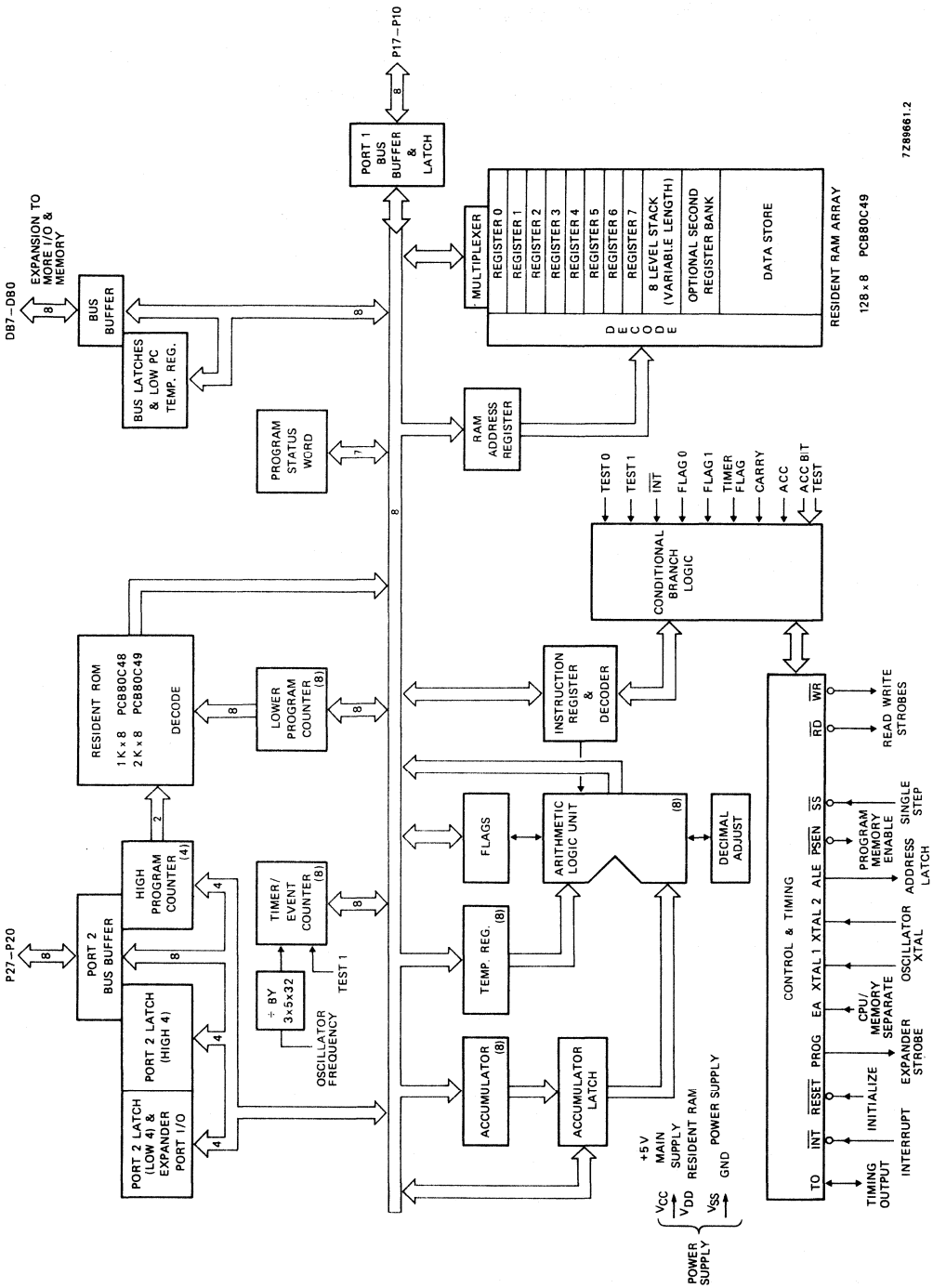


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C552 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C552 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C552" is used to refer to both family members:

- PCB83C552: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C552: ROM-less version of the PCB83C552

This I/O intensive device provides architectural enhancements to function as a controller in the field of automotive electronics, specifically engine management and gear box control.

The PCB83C552 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a fifteen-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I^2C-bus), a 'watchdog' timer and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C552 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

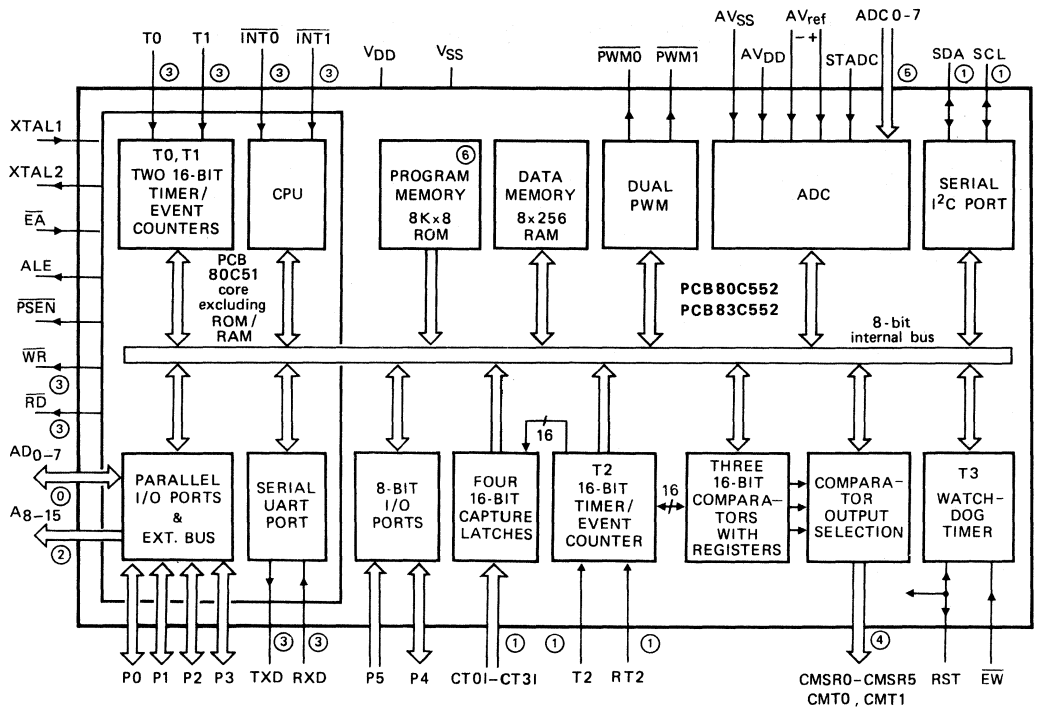
Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- A 10-bit ADC with 8 multiplexed analogue inputs
- Two 8-bit resolution, Pulse Width Modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analogue inputs
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART compatible with the standard PCB80C51
- On-chip watchdog timer

- **A version for extended temperature range is in preparation**

PACKAGE OUTLINE

PCB83C552, PCB80C552: 68-lead PLCC; plastic, leaded-chip-carrier (SOT-188).



0 alternative function of port 0
1 alternative function of port 1
2 alternative function of port 2
3 alternative function of port 3
4 alternative function of port 4
5 alternative function of port 5
6 not present in PCB80C552

7Z97647.3

POWER SUPPLY
V_{DD} + 5 V MAIN SUPPLY
V_{SS} GROUND

Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C652 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C652 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C652" is used to refer to both family members:

- PCB83C652: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C652: ROM-less version of the PCB83C652

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems.

The PCB83C652 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART facilities

- **A version for extended temperature range, extended frequency range (1,2 MHz - 12 MHz) is in preparation**

PACKAGE OUTLINES

PCB83C652P; PCB80C652P: 40-lead DIL; plastic (SOT-129).
PCB83C652WP; PCB80C652WP: 44-lead plastic leaded-chip-carrier (PLCC); (SOT-187).

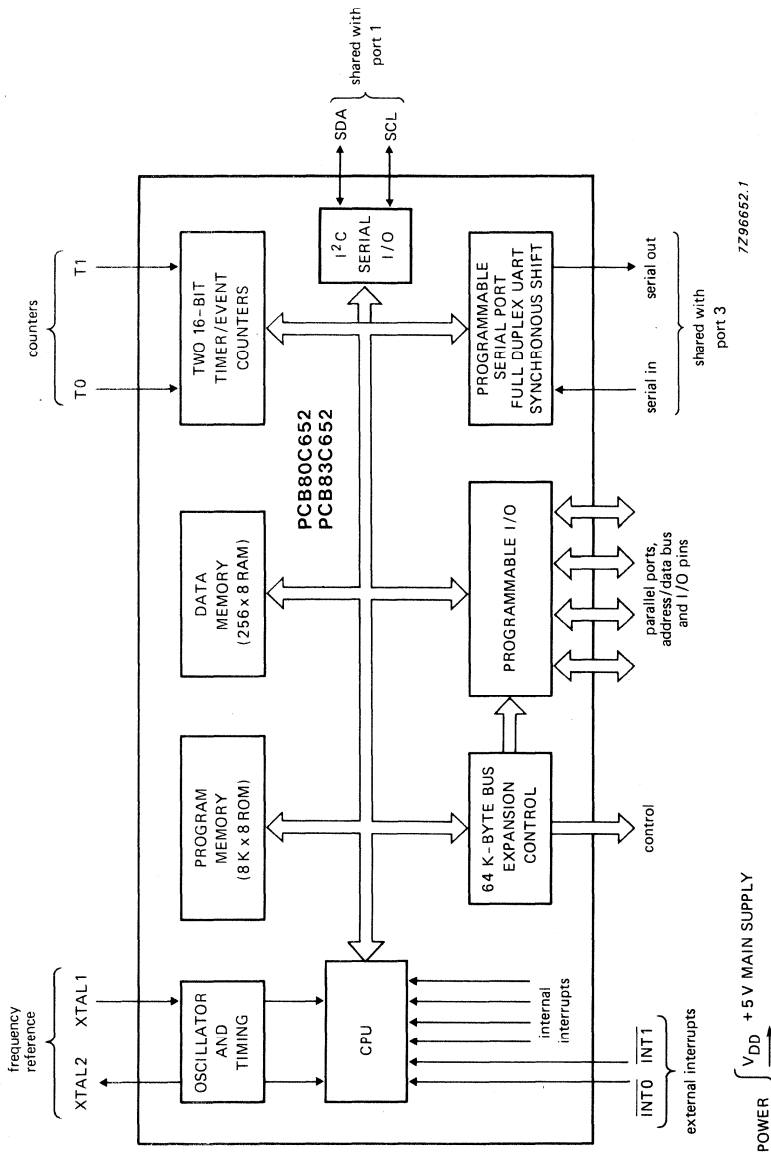


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C654 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C654 has the same instruction set as the PCB80C51.

- PCB83C654: 16 K bytes mask-programmable ROM, 256 bytes RAM

As ROM-less version, the PCB80C652 is available.

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems.

The PCB83C654 contains a non-volatile 16 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C654 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

Features

- 80C51 central processing unit
- 16 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART facilities
- Operating frequency range: 1,2 - 12 MHz

- **A version for extended temperature range is in preparation**

PACKAGE OUTLINES

PCB83C654P; 40-lead DIL; plastic (SOT-129).
PCB83C654WP; 44-lead plastic leaded chip-carrier (PLCC); (SOT-187).
PCB83C654H; 44-lead quad flat-pack; plastic (SOT-205A) in preparation.

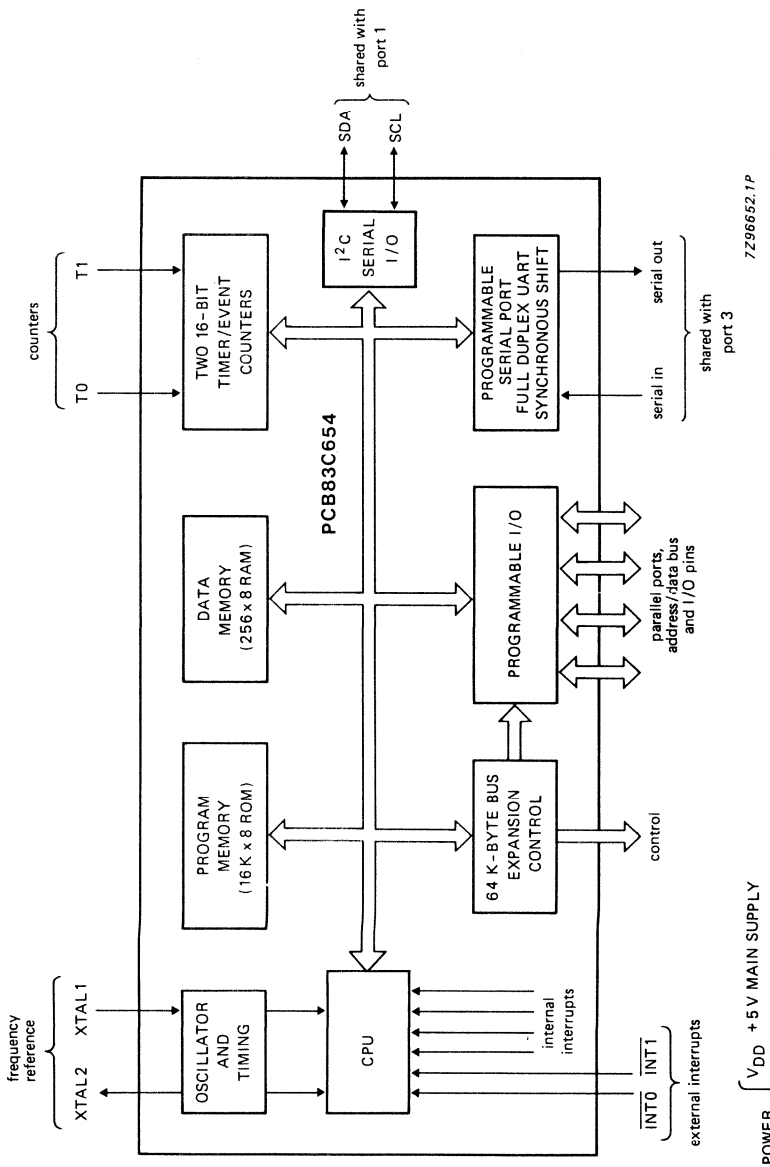


Fig. 1 Block diagram.

STATIC CMOS EEPROM (256 x 8 BIT)

GENERAL DESCRIPTION

The PCB8582 is a 2K-bit 5 V electrically erasable programmable read only memory (EEPROM) organized as 256 by 8 bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I^2C bus, an eight pin DIL package is sufficient. Up to eight PCB8582 devices may be connected to the I^2C bus.

Chip select is accomplished by three address inputs.

Features

- Non-volatile storage of 2K-bit organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- Power on reset
- 10 000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571 and PCD8572

- A version for extended temperature range, −40 to + 85 °C, in preparation: PCF8582.

PACKAGE OUTLINE

PCB8582P: 8-lead DIL; plastic (SOT-97).

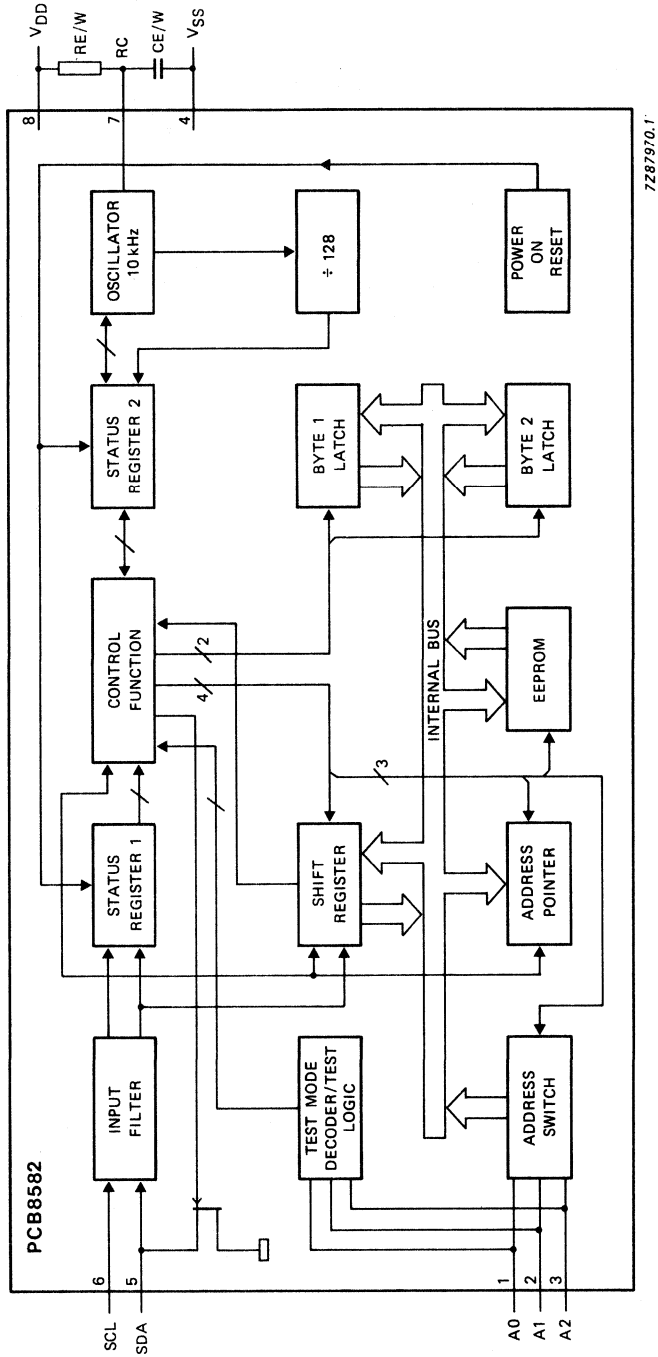


Fig. 1 Block diagram.

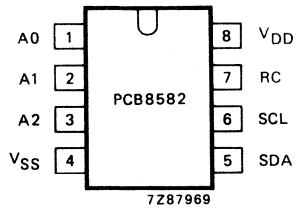


Fig. 2 Pinning diagram.

1 A0
2 A1 address inputs/test
3 A2 mode select
4 V_{SS} ground
5 SDA } I^2C bus lines
6 SCL }
7 RC input for timer constant
8 V_{DD} positive supply

FUNCTIONAL DESCRIPTION

Characteristics of the I^2C bus

The I^2C bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:
Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:
Bus not busy: both data and clock lines remain HIGH.
Start data transfer: a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition.
Stop data transfer: a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transfered between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I^2C bus specifications a low-speed mode (2 kHz clock rate) and a high-speed mode (100 kHz clock rate) are defined. The PCB8582 operates in both modes.
By definition a device that gives out a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.
A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse.
Set-up-and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVELOPMENT DATA

Note

The general characteristics and detailed specification of the I²C bus is available on request.

I²C bus protocol

The I²C bus configuration for different READ and WRITE cycles of the PCB8582 are shown in Fig. 3.

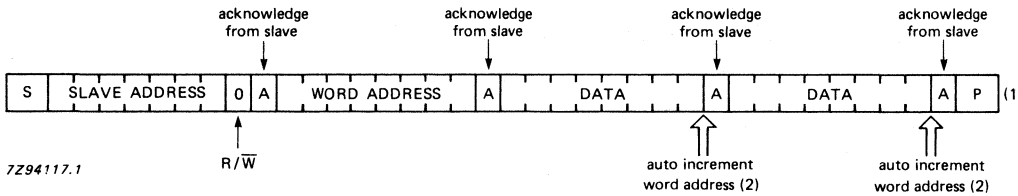


Fig. 3(a) Slave receiver ERASE/WRITE mode.

(1.)After this stop condition the erase/write cycle starts and the bus is free for another transmission; the duration of the erase/write cycle is approximatly 20 ms if only one byte is written, and 40 ms, if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via I²C bus.

(2.)The second data byte is voluntary. It is not allowed to erase/write more than two bytes.

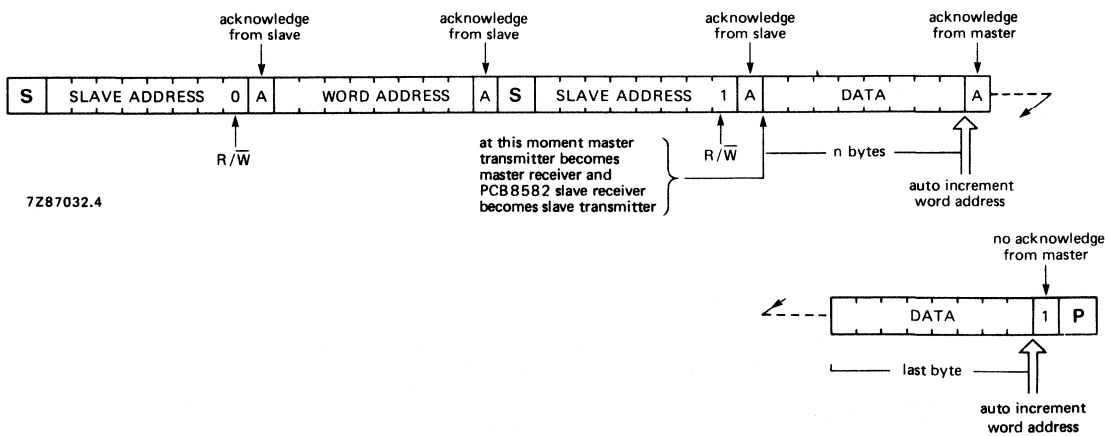


Fig. 3(b) Master reads PCB8582 slave after setting word address. (WRITE word address; READ data).

Note: The slave address is defined in accordance with the I²C bus specification as:

1	0	1	0	A2	A1	A0	R/$\overline{W}$

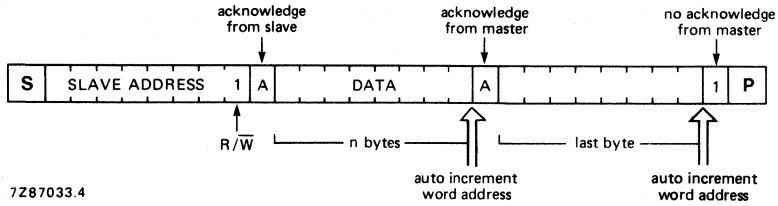


Fig. 3(c) Master reads PCB8582 slave immediately after first byte (READ mode).

I²C bus timing

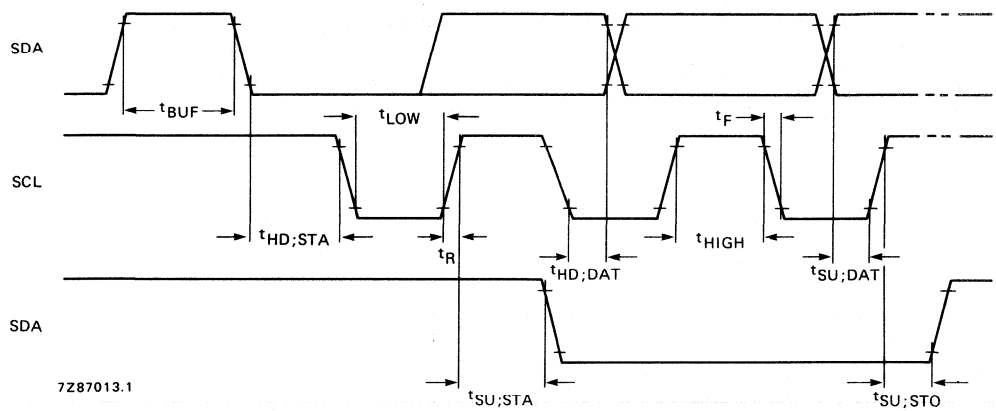


Fig. 4 I²C bus, timing.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 7 V
Voltage, on any input pin (input impedance 500 Ω)	V_I	V_{SS}−0,8 to V_{DD} +0,8 V
Operating temperature range	T_{amb}	0 to +70 °C
Storage temperature range	T_{stg}	−65 to +150 °C
Current into any input pin	I_I	1 mA
Output current	I_O	10 mA

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 0 to + 70 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5	5,5	V
Operating supply current, READ (f_{SLC} = 100 kHz)	I_{DDR}	–	0,1	0,2	mA
Operating supply current, WRITE/ERASE	I_{DDW}	–	1	2	mA
Standby supply current (V_{DD} = 5 V)	I_{DDO}	–	5	10	μA
Input SCL and input/output SDA					
Input/output SDA:					
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input voltage HIGH	V_{IH}	3	–	V_{DD}+0,8	V
Output voltage LOW (I_{OL} = 3 mA, V_{DD} = 4,5 V)	V_{OL}	–	–	0,4	V
Output leakage current HIGH (V_{OH} = V_{DD})	I_{OH}	–	–	1	μA
Input leakage current (A0,A1,A2, SCL), (note 1)	$\pm I_{IN}$	–	–	1	μA
Clock frequency	f_{SCL}	0	–	100	kHz
Input capacity (SCL,SDA)	C_I	–	–	7	pF
Noise suppression time constant at SCL and SDA input	t_I	0,25	0,5	1	μs
Time the bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Hold time start condition. After this period the first clock pulse is generated	$t_{HD;STA}$	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
Set-up time for start condition (only relevent for a repeated start condition)	$t_{SU;STA}$	4,7	–	–	μs
Hold time DATA for:					
CBUS compatible masters	$t_{HD;DAT}$	5	–	–	μs
I^2C devices (note 2)	$t_{HD;DAT}$	0	–	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	–	ns
Rise time for both SDA and SCL lines	t_R	–	–	1	μs
Fall time for both SDA and SCL lines	t_F	–	–	300	ns
Set-up time for stop condition	$t_{SU\cdot STO}$	4,7	–	–	μs
Erase/write timer constant (note 3)					
Erase/write cycle time	$t_{E/W}$	20	–	100	ms
Erase/write timing capacitor for erase/write cycle of 30 ms	$C_{E/W}$	–	3,3	–	nF
Erase/write timing resistor for erase/write cycle of 30 ms	$R_{E/W}$	–	56	–	kΩ
Data retention time	t_S	10	–	–	years

Notes to the characteristics

1. Selection of the chip address is done by connecting the A0, A1, and A2 inputs either to V_{SS} or V_{DD}.
2. A transmitter must internally provide a hold time to bridge the undefined region (maximum 300 ns) of the falling edge of SCL.
3. Endurance (number of erase/write cycles), NE/W, is 10^4 E/W cycles.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

DEVELOPMENT DATA

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84CXX family of microcontrollers. The family consists of the following devices:

- PCF84C00 – 256 x 8 RAM, external program memory
- PCF84C21 – 2 K x 8 ROM, 64 x 8 RAM
- PCF84C41 – 4 K x 8 ROM, 128 x 8 RAM
- PCF84C81 – 8 K x 8 ROM, 256 x 8 RAM

Each version has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits.

Each member of this microcontroller family is an efficient controller as well as an arithmetic processor. The instruction set is similar to that of the MAB8048 and the PCF84CXX family is pin- and instruction set compatible with the MAB8400 family.
The microcontrollers have facilities for both binary and BCD arithmetic plus bit-handling capabilities.

For detailed information see the user manual "Single-chip 8-bit microcontrollers".

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2 K, 4 K or 8 K x 8 ROM; also a ROM-less version
- 64, 128 or 256 x 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 V to 5,5 V)
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C
- High current output on Port 1: I_{OL} = 10 mA at V_{OL} = 1,2 V (all versions except the PCF84C00)

PACKAGE OUTLINES

PCF84C21/41/81P : 28-lead DIL; plastic (SOT-117).
PCF84C21/41/81T : 28-lead mini-pack; plastic (SO-28; SOT-136A).
PCF84C00B : 28-lead 'piggy-back' package (with up to 28-pin EPROM on top).
PCF84C00T : 56-lead mini-pack; plastic (VSO-56; SOT-190).

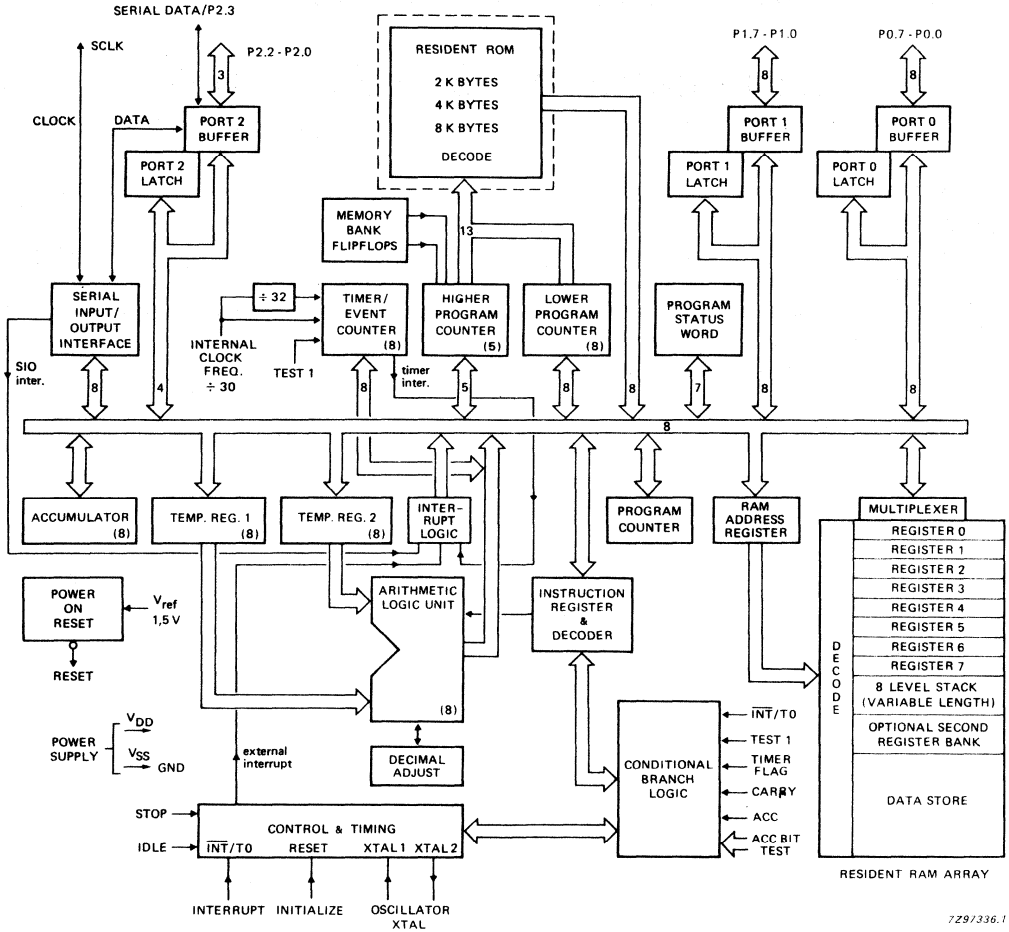


Fig. 1 PCF84CXX block diagram.

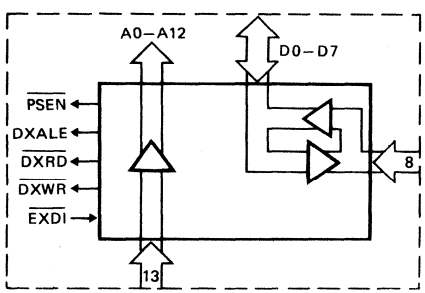


Fig. 1a Replacement of dotted section in Fig. 1, for the PCF84C00T ROM-less version.

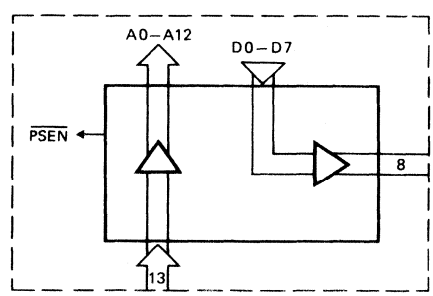


Fig. 1b Replacement of dotted section in Fig. 1, for the PCF84C00B 'piggy-back' version.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The PCF84C12 microcontroller is manufactured in CMOS technology.
It has 13 quasi-bidirectional I/O port lines, one single-level vectored interrupt, an 8-bit timer event counter and on-board clock oscillator and clock circuits.

This microcontroller is an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048 and is pin- and instruction set compatible with the MAB8400 family. The PCF84C12 has bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the user manual "Single-chip 8-bit microcontrollers".

Features

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead DIL or SO package
- 1 K ROM bytes
- 64 RAM bytes
- 13 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external and timer/event counter
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINES

PCF84C12P: 20-lead DIL; plastic (SOT-146).
PCF84C12T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

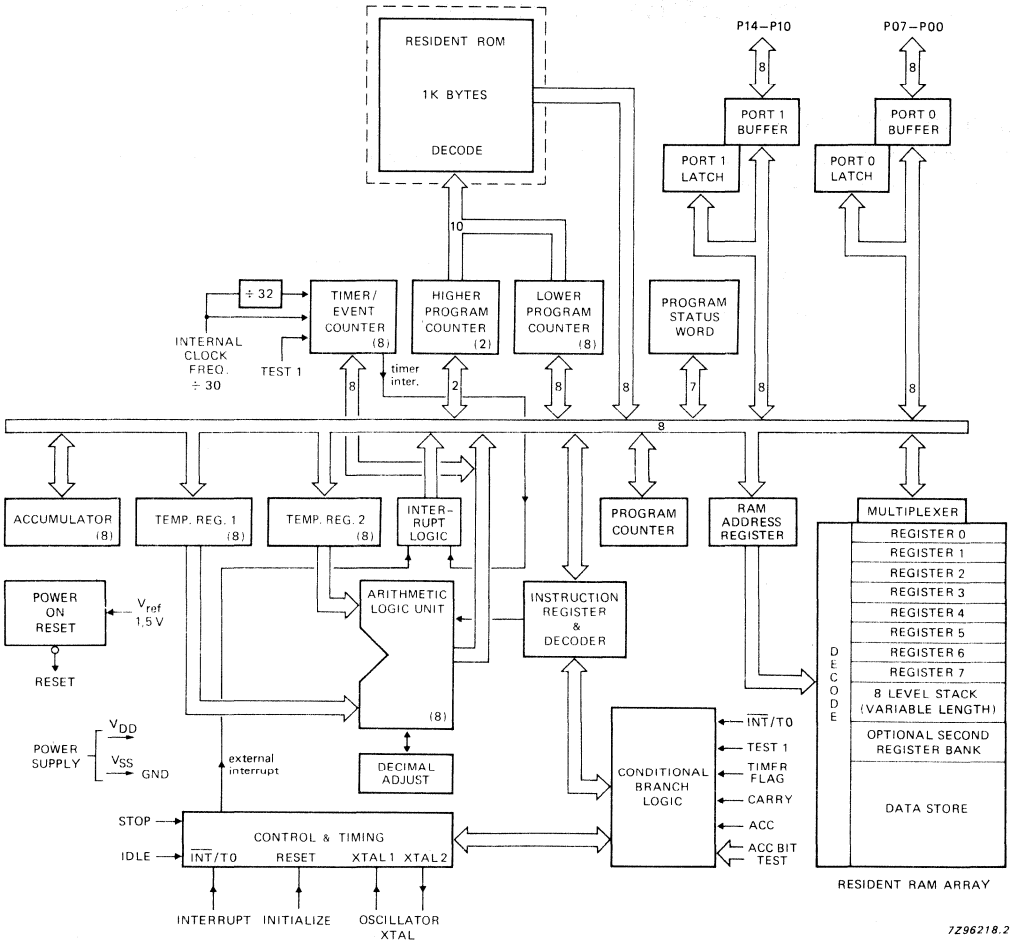


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

18-ELEMENT BAR GRAPH LCD DRIVER

GENERAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to control voltage (V_C) when in pointer or thermometer mode.

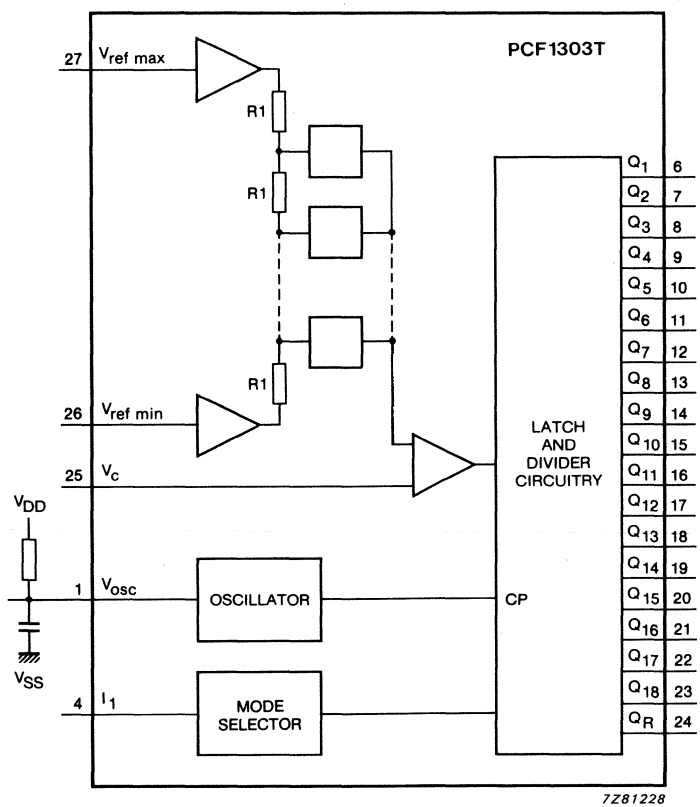
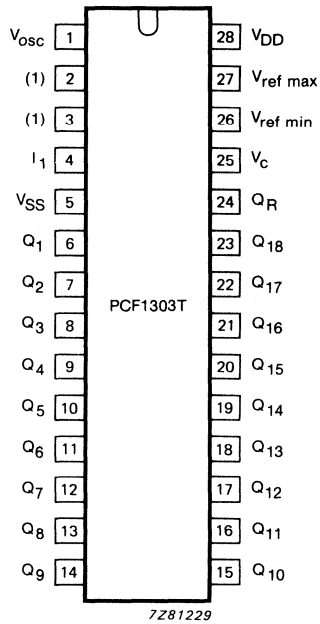


Fig. 1 Block diagram.

PACKAGE OUTLINE

PCF1303T: 28-lead mini-pack; plastic (SO-28; SOT-136A).



(1) Pins 2 and 3 should be connected to V_{SS}.

Fig. 2 Pin configuration.

PIN DESCRIPTION

pin no.	symbol	name and function
1	V_{osc}	oscillator pin
4	I_1	mode select input
5	V_{SS}	ground (0 V)
6 to 23	Q_1 to Q_{18}	segment outputs
24	Q_R	back-plane output
25	V_c	control voltage
26 27	$V_{ref\,min}$ $V_{ref\,max}$	reference voltage inputs
28	V_{DD}	positive supply voltage

FUNCTION TABLE

I_1	mode
L	pointer
H	thermometer

H = HIGH voltage level
L = LOW voltage level

FUNCTIONAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to the control voltage when in pointer or thermometer mode.

The first segment will energize when the control voltage is less than the trigger voltage ($V_{T(bar)2}$ see equation [3]).

The circuit has analogue and digital sections.

The analogue section consists of a comparator with the inverting input coupled to the input control voltage. The non-inverting input of the comparator is connected via 17 analogue switches to the nodes of an 18-element resistor divider. The extremities of the resistor divider are coupled via high-input impedance amplifiers to the maximum reference voltage input and the minimum reference voltage input.

The control input functions with Schmitt trigger action.

The digital section has one reference output (Q_R) to drive the back-plane and 18 outputs (Q_1 to Q_{18}) to drive the segments.

The segment outputs incorporate two latches and some gates.

The circuit is driven by an on-chip oscillator with external resistors and capacitors. The outputs are driven at typical 100 Hz.

LINEARITY

$$V_{step} = V_{step'} \pm \Delta V_{step} \qquad [1]$$

$V_{step'}$ is the voltage drop (internal) across the resistor-ladder network.
ΔV_{step} is the differential on V_{step}.

$$V_{step'} = \frac{(V_{ref\,max} \pm \Delta V_{2'}) - (V_{ref\,min} \pm \Delta V_2)}{18} \qquad [2]$$

ΔV_2 and $\Delta V_{2'}$ are the maximum offset voltage spread of the on-chip voltage followers.

ABSOLUTE VOLTAGE TRIGGER LEVEL

The absolute voltage trigger level at the V_c pin is $V_{T(bar)n}$;

$$V_{T(bar)n} = (V_{ref\,min} \pm \Delta V_{2}{}^{*}) + \{ (n - 1)V_{step'} \pm \Delta V_R \} \pm \Delta V_1 \pm V_H \qquad [3]$$

n = number of segments; $2 \leqslant n \leqslant 18$.

ΔV_R is the voltage deviation at step n of the resistor-ladder network (for n = 2 or 18, $\Delta V_R = \Delta V_{step}$).

ΔV_1 is the offset voltage for the on-chip comparator.

V_H is the hysteresis voltage: $30\%\ V_{step} \geqslant V_H \geqslant 10\%\ V_{step}$.

* For ΔV_2 the same sign (+ or –) should be used as in equation [2].

RATINGS

Limiting values as in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,5 to + 15 V
Voltage on any input	V_I	−0,5 to V_{DD} + 0,5 V
D.C. current into any input or output	$\pm I_I$	max. 10 mA
Storage temperature range	T_{stg}	−25 to + 125 °C
Operating ambient temperature range	T_{amb}	−40 to + 85 °C

D.C. CHARACTERISTICS

V_{SS} = 0 V

parameter	V_{DD} V	symbol	T_{amb} (°C)							unit	notes
			−40		+ 25			+ 85			
			min.	max.	min.	typ.	max.	min.	max.		
Quiescent device current	10,0	I_{DD}		1200			1200		1200	μA	1
Operating supply current	8,2	I_{DD}		2,0			2,0		2,0	mA	2
Input leakage current	6,0 8,2 10,0	$\pm I_I$ $\pm I_I$ $\pm I_I$		300 300 300			300 300 300		1000 1000 1000	nA nA nA	3
HIGH level input voltage select input I_1	6,0 8,2 10,0	V_{IH} V_{IH} V_{IH}	4,2 5,8 7,0		4,2 5,8 7,0			4,2 5,8 7,0		V V V	
LOW level input voltage select input I_1	6,0 8,2 10,0	V_{IL} V_{IL} V_{IL}		1,8 2,4 3,0	2,4		1,8 2,4 3,0		1,8 3,0	V V V	
HIGH level output voltage	6,0 8,2 10,0	V_{OH} V_{OH} V_{OH}	5,95 8,15 9,95		5,95 8,15 9,95			5,95 8,15 9,95		V V V	4
LOW level output voltage	6,0 8,2 10,0	V_{OL} V_{OL} V_{OL}		0,05 0,05 0,05			0,05 0,05 0,05		0,05 0,05 0,05	V V V	4
Output current HIGH	6,0 8,2 10,0	$-I_{OH}$ $-I_{OH}$ $-I_{OH}$	0,6 0,85 1,0		0,5 0,7 0,85			0,35 0,45 0,6		mA mA mA	5
Output current LOW	6,0 8,2 10,0	I_{OL} I_{OL} I_{OL}	0,65 1,0 1,3		0,5 0,8 1,0			0,4 0,6 0,8		mA mA mA	6

For notes see page 6.

parameter	V_{DD} V	symbol	T_{amb} (°C)							unit	notes
			−40		+ 25			+ 85			
			min.	max.	min.	typ.	max.	min.	max.		
Input voltage control input V_c	6,0	V_{IC}	0,0	6,0	0,0		6,0	0,0	6,0	V	
	8,2	V_{IC}	0,0	8,2	0,0		8,2	0,0	8,2	V	
	10,0	V_{IC}	0,0	10,0	0,0		10,0	0,0	10,0	V	
Input voltage $V_{ref\ max}$ input	6,0	$V_{IR\ max}$	3,6	5,5	3,6		5,5	3,6	5,5	V	
	8,2	$V_{IR\ max}$	3,6	7,7	3,6		7,7	3,6	7,7	V	
	10,0	$V_{IR\ max}$	3,6	9,5	3,6		9,5	3,6	9,5	V	
Input voltage $V_{ref\ min}$ input	6,0	$V_{IR\ min}$	0,5	1,0	0,5		1,0	0,5	1,0	V	
	8,2	$V_{IR\ min}$	0,5	4,5	0,5		4,5	0,5	4,5	V	
	10,0	$V_{IR\ min}$	0,5	6,0	0,5		6,0	0,5	6,0	V	
$V_{ref\ max}$ − $V_{ref\ min}$	6,0	ΔV_I	3,0		3,0			3,0		V	
	8,2	ΔV_I	3,0		3,0			3,0		V	
	10,0	ΔV_I	3,0		3,0			3,0		V	
DC component bar output to back-plane output	8,2	$\pm V_{BP}$		25		10	25		25	mV	7
Back-plane frequency	8,2	f_{BP}	90	110		100		90	110	Hz	8
Input offset voltage	8,2	$\pm V_{IO}$		120			120		120	mV	9
Step voltage variation	8,2	$\pm \Delta V_{step}$		50			50		50	mV	10
Input voltage slew rate V_c input	6,0	SR		50			50		50	V/s	11
	8,2	SR		50			50		50	V/s	
	10,0	SR		50			50		50	V/s	

For notes see next page.

Notes to D.C. characteristics

1. $V_{ref\,min}$ = 0,5 V, $V_{ref\,max}$ = 9,5 V, $V_c = V_{osc}$ = 0 V, I_1 at V_{SS} or V_{DD}.
2. See Fig. 2.
3. Pin under test at V_{SS} or V_{DD}. All other inputs simultaneously at V_{SS} or V_{DD}.
4. I_O = 0, all inputs at V_{SS} or V_{DD}.
5. $V_{OH} = V_{DD} - 0{,}5$ V, all inputs at V_{SS} or V_{DD}.
6. V_{OL} = 0,4 V, all inputs at V_{SS} or V_{DD}.
7. f_{BP} = 100 Hz, load segment outputs to back-plane output.
   $C_1 - C_{18} \leqslant 0{,}01\ \mu F$, $C_{BP} = C_1 + C_2 + \ldots C_{18} \leqslant 0{,}05\ \mu F$, $R_1 - R_{18} \geqslant 2\ M\Omega$.
8. R_{osc} = 0,1 MΩ, C_{osc} = 390 pF.
9. Number of segments 2 or 18.
   For n = 2:

$$V_{IO} = V_c - V_{ref\,min} - \frac{(V_{ref\,max}) - (V_{ref\,min})}{18} \pm V_H$$

   For n = 18:

$$V_{IO} = V_c - V_{ref\,max} + \frac{(V_{ref\,max}) - (V_{ref\,min})}{18} \pm V_H$$

10. See equation [1].
11. Condition applies with clock oscillator such that f_{BP} = 100 Hz.

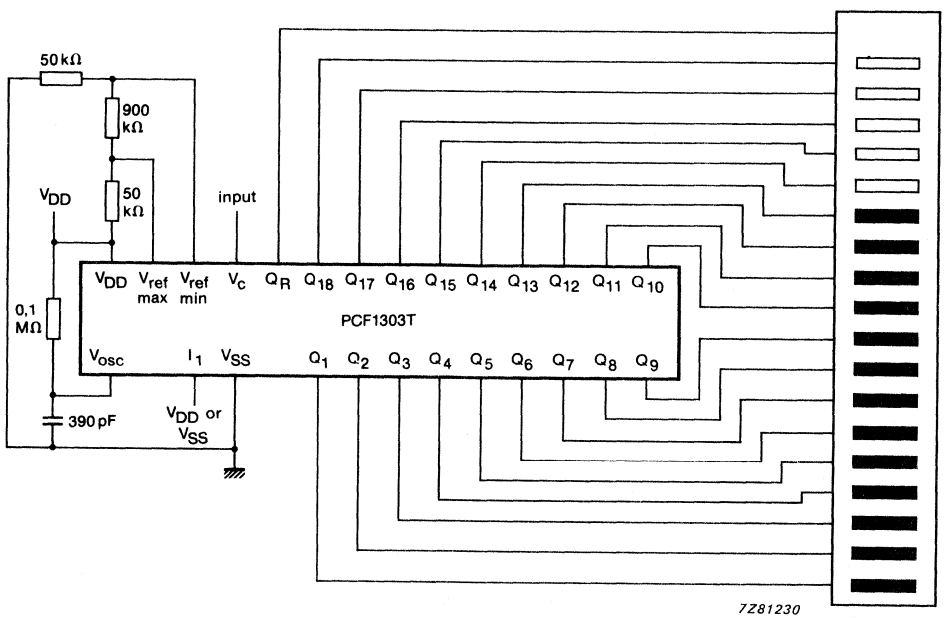


Fig. 3 Typical application.

LCD DRIVER

GENERAL DESCRIPTION

The members of the PCF21XX family are single chip, silicon gate CMOS circuits. A three-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility
- Power-on reset clear

	PCF2100	PCF2110	PCF2111	PCF2112
• LCD segments	40	60	64	32
• LED segments	–	2	–	–
• Multiplex rate	1:2	1:2	1:2	1:1
• Word length	22 bit	34 bit	34 bit	34 bit

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT-117).

PCF2110P:
PCF2111P: 40-lead DIL; plastic (SOT-129).
PCF2112P:

PCF2100T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

PCF2110T:
PCF2111T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).
PCF2112T:

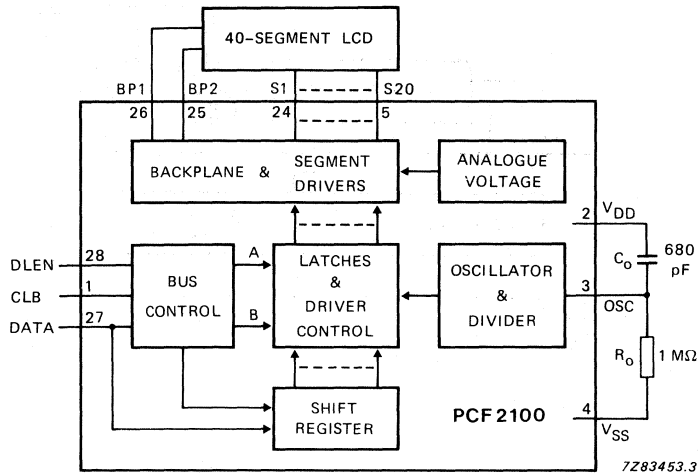


Fig. 1 Block diagram; PCF2100

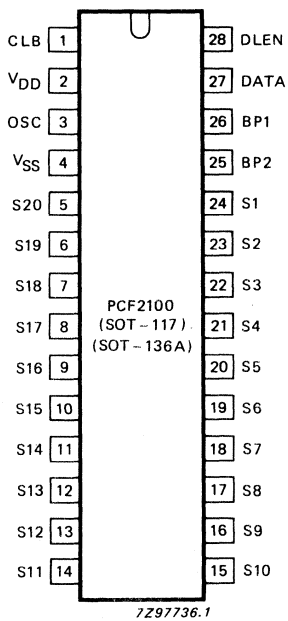


Fig. 2 Pinning diagram; PCF2100

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
27	DATA	data line	CBUS
28	DLEN	data line enable	CBUS

Outputs

5 to 24	S20 to S1	LCD driver outputs
25	BP2	backplane drivers (commons of LCD)
26	BP1	backplane drivers (commons of LCD)

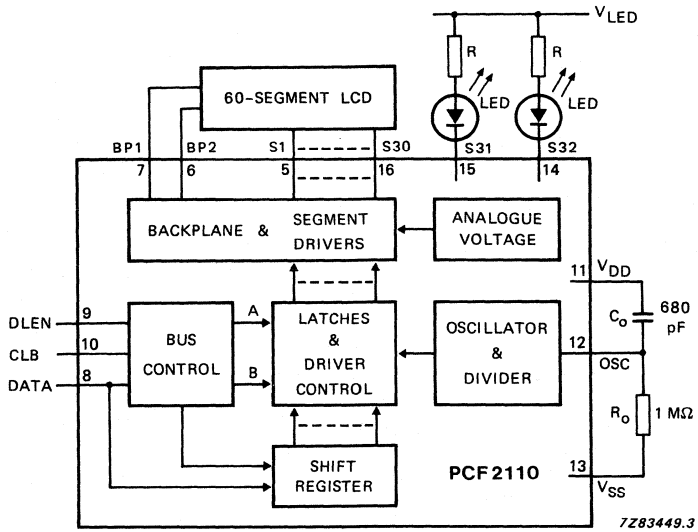


Fig. 3 Block diagram; PCF2110 (SOT-129).

DEVELOPMENT DATA

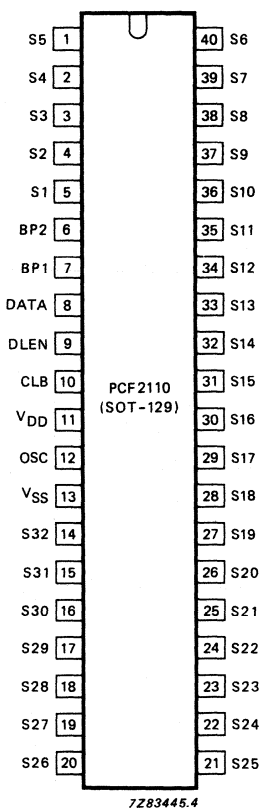


Fig. 4 Pinning diagram; PCF2110

PINNING (SOT-129)

Supply

11	V_{DD}	positive supply
13	V_{SS}	negative supply

Inputs

8	DATA	data line } CBUS
9	DLEN	data line enable } CBUS
10	CLB	clock burst } CBUS
12	OSC	oscillator input

Outputs

1 to 5	S5 to S1	LCD driver outputs
6	BP2	backplane drivers (commons of LCD)
7	BP1	backplane drivers (commons of LCD)
14	S32	LED driver outputs
15	S31	LED driver outputs
16 to 40	S30 to S6	LCD driver outputs

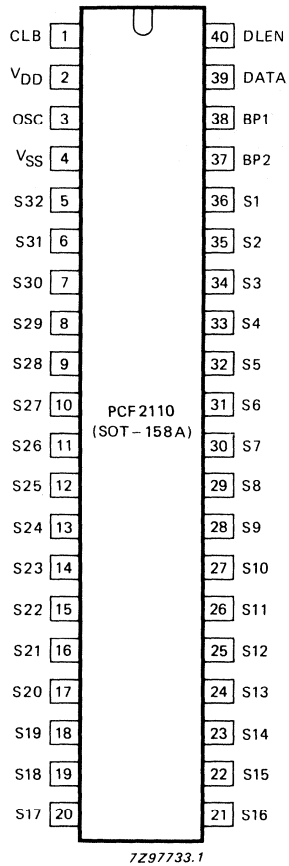


Fig. 5 Pinning diagram; PCF2110

PINNING (SOT-158A)

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5	S32	LED driver outputs
6	S31	LED driver outputs
7 to 36	S30 to S1	LCD driver outputs
37	BP2	backplane drivers (commons of LCD)
38	BP1	backplane drivers (commons of LCD)

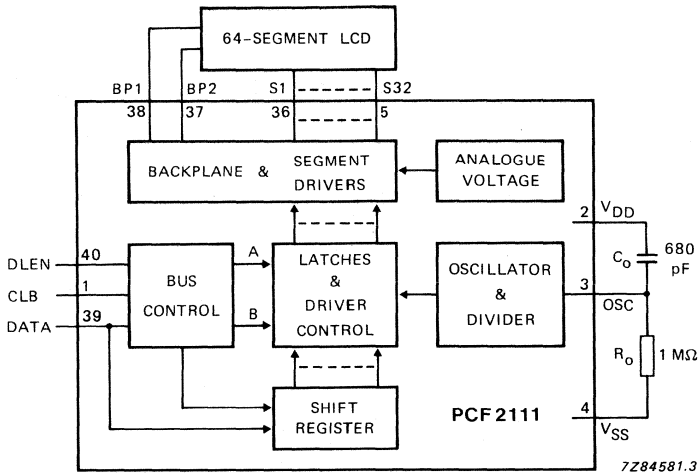


Fig. 6 Block diagram; PCF2111

DEVELOPMENT DATA

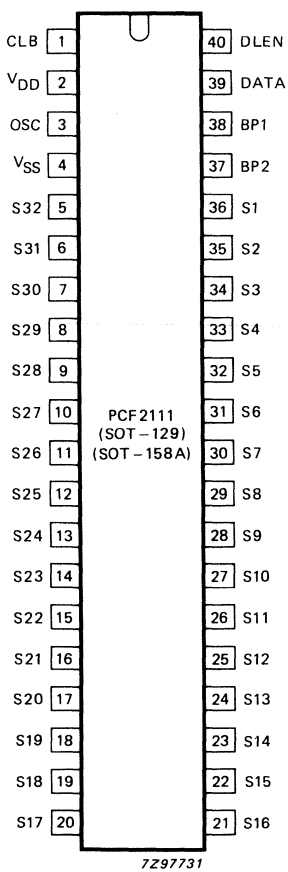


Fig. 7 Pinning diagram; PCF2111

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	} CBUS
40	DLEN	data line enable	} CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP1	} backplane drivers
37	BP2	} (commons of LCD)

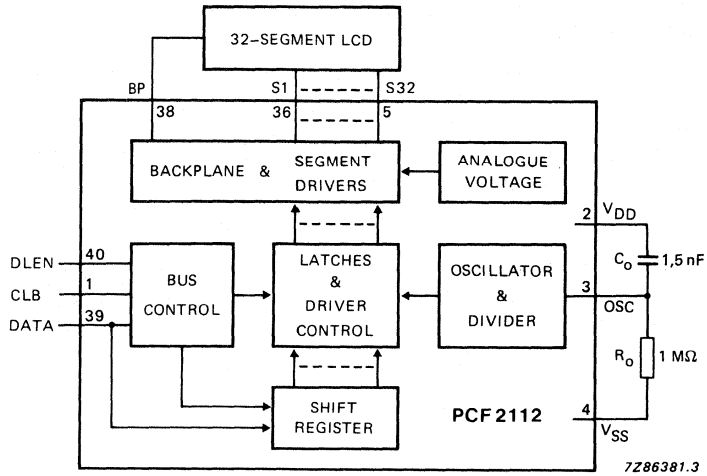


Fig. 8 Block diagram; PCF2112

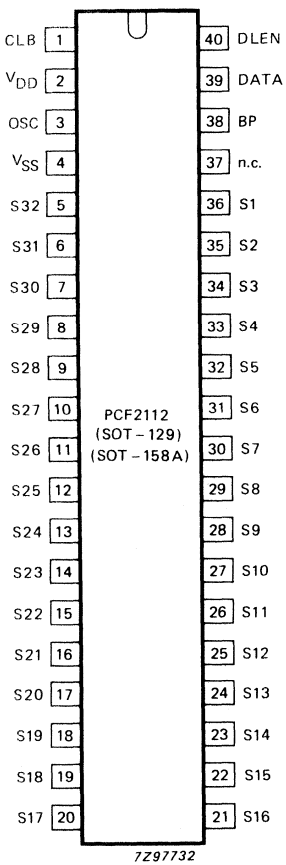


Fig. 9 Pinning diagram; PCF2112

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP	backplane driver (common of LCD)
37	n.c.	not connected

FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA-bit is HIGH.

PCF2100

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded. CLB-pulse 23 transfers data from the shift register to the selected latches.

PCF2110

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. Bits 31 and 32 contain the LED output information. With DATA-bit 33 LOW, the B-latches (BP2) are loaded and bits 31 and 32 are ignored. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2111

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2112

When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

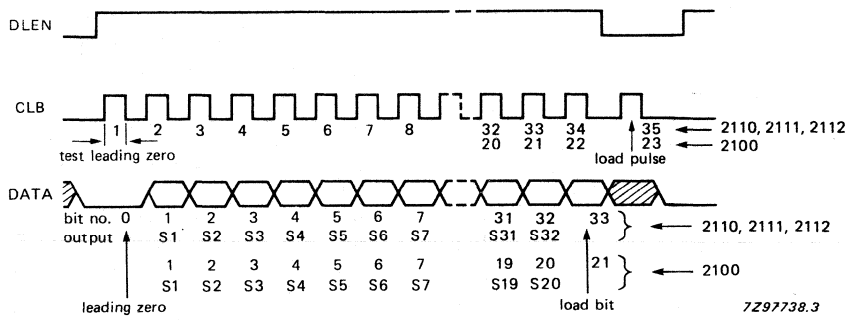


Fig. 10 CBUS data format.

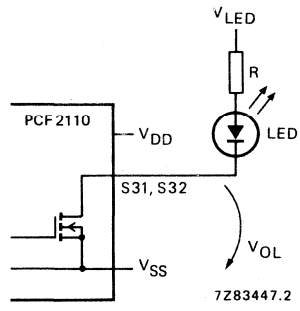


Fig. 11 LED driver circuitry.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

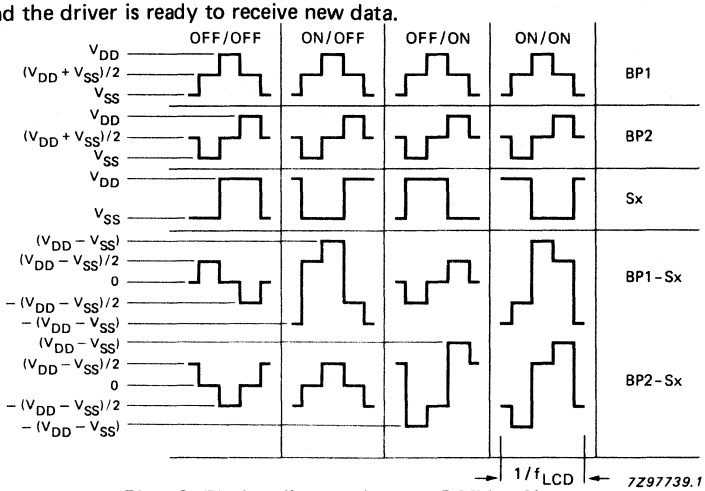


Fig. 12 Timing diagram (except PCF2112).

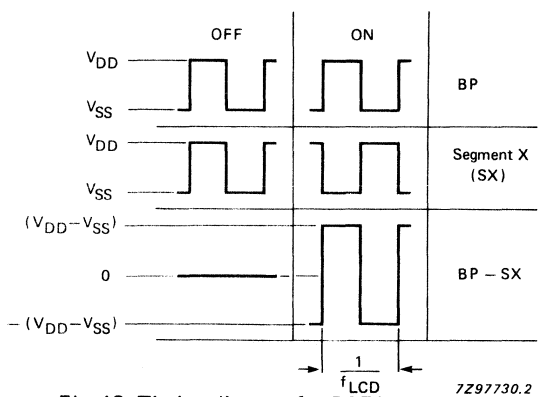


Fig. 13 Timing diagram for PCF2112.

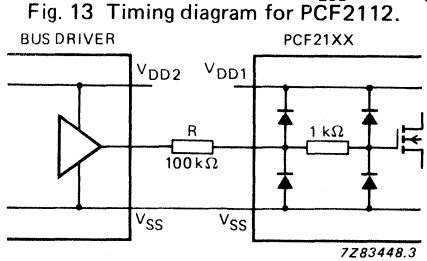
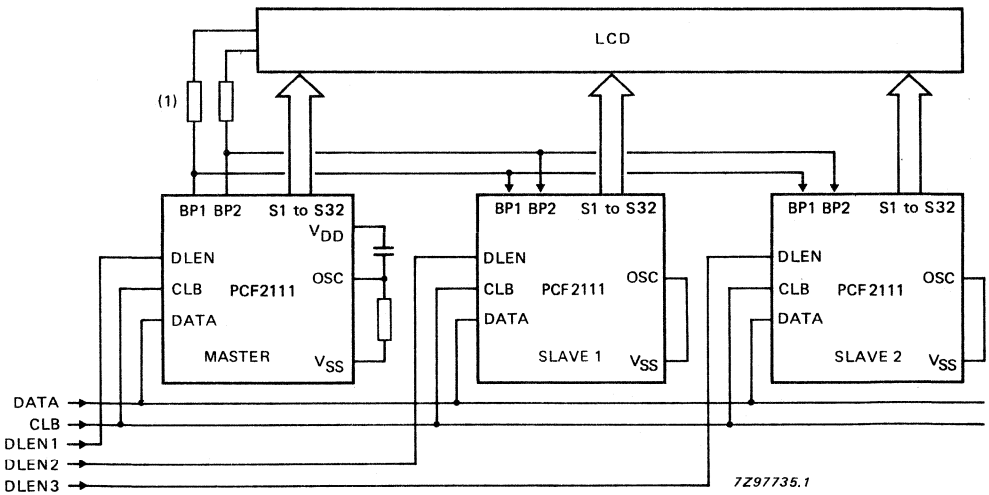


Fig. 14 Input circuitry.

Note to Fig. 14

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current $\leqslant 40\,\mu A$.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be $> 2{,}7\ k\Omega$. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 15 Diagram showing expansion possibility (using PCF2111).

Note to Fig. 15

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21XX family up to the BP drive capability of the master. The PCF2112 can only function as a master for other PCF2112s.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	9,0	V
Input voltage range DLEN, CLB, DATA and OSC		V_I	V_{SS}−0,5	V_{DD}+0,5	V
Output voltage range BP1, BP2 and S1 to S32		V_O	V_{SS}−0,5	V_{DD}+0,5	V
Supply current		$\pm I_{DD}$, $\pm I_{SS}$	−	50	mA
DC input current		$\pm I_I$	−	20	mA
DC output current		$\pm I_O$	−	25	mA
Total power dissipation per package	note 1	P_{tot}	−	500	mW
Power dissipation per output		P_O	−	100	mW
Storage temperature range		T_{stg}	−65	+150	°C

Note to the ratings

1. Derate by 7,7 mW/°C when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2,25	–	6,5	V
Supply current	note 1	I_{DD1}	–	20	50	μA
Supply current	note 1; T_{amb} = −25 to + 85 °C	I_{DD2}	–	20	30	μA
Power-on reset level	note 2	V_{POR}	–	1,0	1,4	V
Inputs CLB, DATA DLEN						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,0	–	–	V
Leakage current	$V_I = V_{SS}$ or V_{DD}	$\pm I_I$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	10	pF
Input OSC						
Oscillator start-up current	$V_I = V_{SS}$	I_{OSC}	0,5	1,2	5,0	μA
LCD outputs						
DC component of backplane drivers		$\pm V_{BP}$	–	20	–	mV
Backplane driver output impedance	note 4; V_{DD} = 5 V	R_{BP}	–	0,5	5	kΩ
Segment driver output impedance	note 4; V_{DD} = 5 V	R_S	–	1	7	kΩ
LED outputs (S31 and S32 in PCF2110)						
Output current LOW	V_{OL}=0,4 V; V_{DD}=5 V	I_{OL}	8	14	–	mA
Output leakage current	$V_O = V_{DD}$	$\pm I_O$	–	–	1	μA
Load current		I_{LED}	–	–	20	mA

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs CLB, DATA DLEN						
Data set-up time		t_{SUDA}	3	–	–	μs
Data hold time		t_{HDDA}	3	–	–	μs
Leading zero set-up time		t_{SULZ}	3	–	–	μs
Enable set-up time		t_{SUEN}	1	–	–	μs
Disable set-up time		t_{SUDI}	2	–	–	μs
Load pulse set-up time		t_{SULD}	2,5	–	–	μs
Busy time		t_{BUSY}	3	–	–	μs
CLB HIGH time		t_{WH}	1	–	–	μs
CLB LOW time		t_{WL}	5	–	–	μs
CLB period		t_{CLB}	10	–	–	μs
Rise and fall times		t_r, t_f	–	–	10	μs
LCD timing						
LCD frame frequency		f_{LCD}	60	75	100	Hz
LCD frame frequency for PCF2112	C_O = 1,5 nF	f_{LCD}	30	35	50	Hz
Transfer time with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
Driver delay with test loads	V_{DD} = 5 V	t_{PLCD}	–	20	100	μs

Notes to the characteristics

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

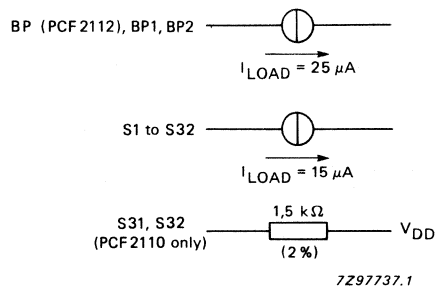


Fig. 16 Test loads.

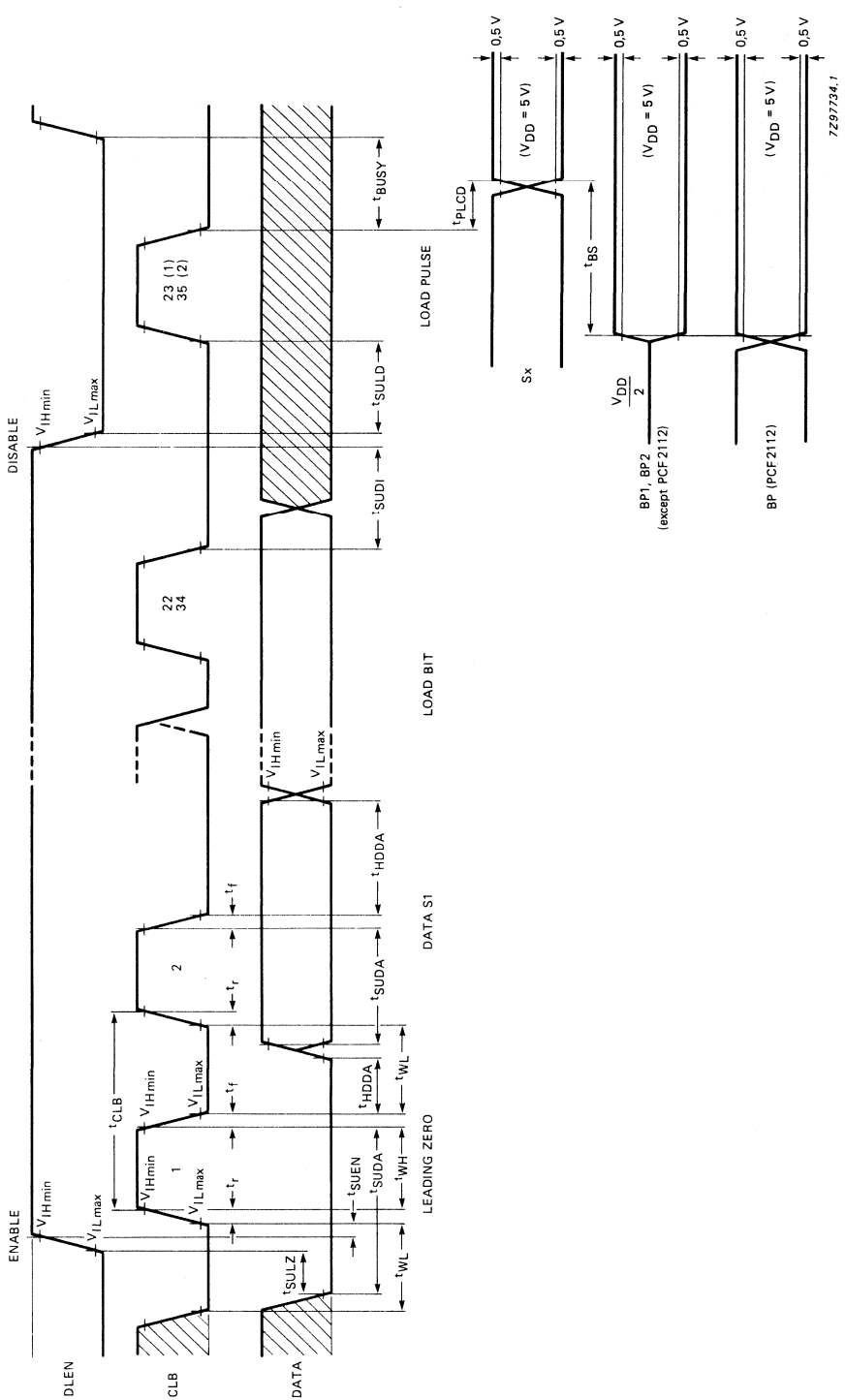


Fig. 17 CBUS timing.

(1) Load pulse 23 (for PCF2100).
(2) Load pulse 35 (for PCF2110, PCD2111 and PCF2112; see Fig. 10).

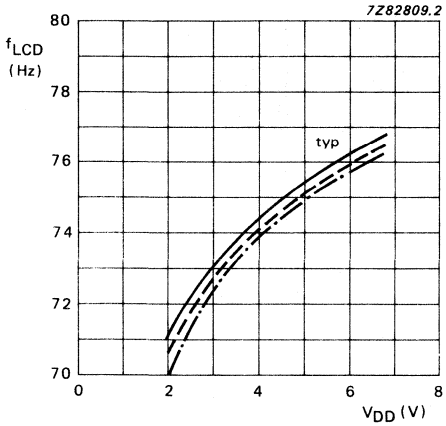


Fig. 18 Displays frequency as a function of supply voltage; C_O = 680 pF (except PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

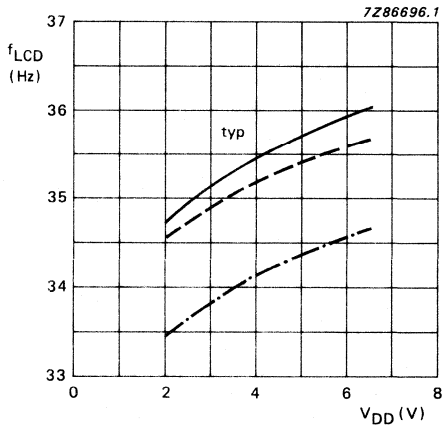


Fig. 19 Display frequency as a function of supply voltage; C_O = 1,5 nF (except PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

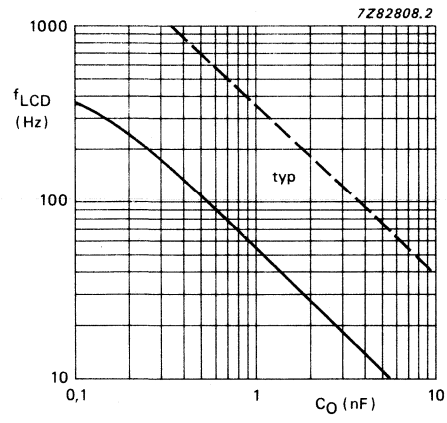


Fig. 20 Display frequency as a function of R_O and C_O; T_{amb} = + 25 °C; V_{DD} = 5 V.
——— R_O = 1 MΩ;
– – – – R_O = 100 kΩ.

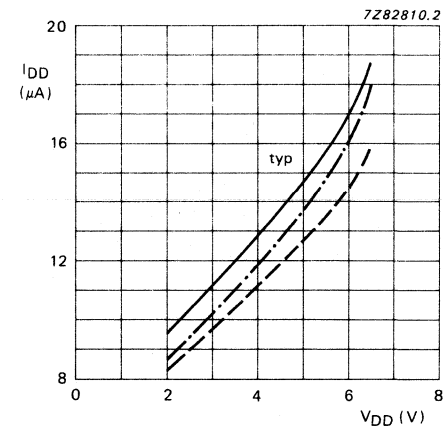


Fig. 21 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

DEVELOPMENT DATA

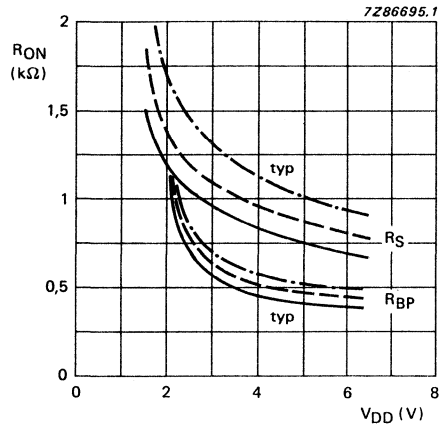


Fig. 22 Output resistance of backplane and segments.
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

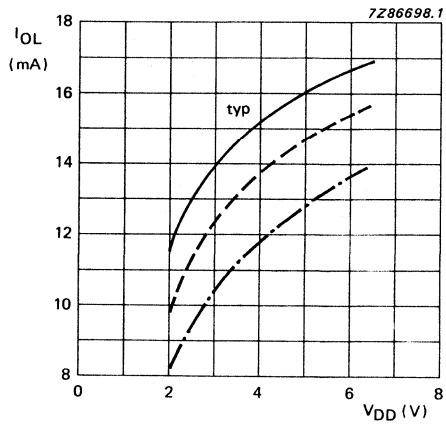


Fig. 23 Output current as a function of supply voltage (only PCF2112).
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

LCD FLAT-PANEL ROW/COLUMN DRIVER

GENERAL DESCRIPTION

The PCF2201 is a row or column LCD driver, designed to drive LCD flat-panels at multiplex rates of up to 1 : 256. The PCF2201 converts serial or parallel 4-bit display data into parallel LCD drive waveforms, capable of driving up to 81 rows or 80 columns of an LCD matrix. The PCF2201 is cascadable, enabling it to drive any LCD flat-panel matrix. The PCF2201 is controlled by an alphanumeric/graphic controller.

Features

- Row or column drive capability
- 80 data latches
- 81 stage bidirectional shift register
- 81 LCD drive outputs
- Proprietary margin control drive output
- Low drive impedance
- LCD drive voltage of up to 25 V
- 5 V logic compatibility
- High speed operation (4 MHz)
- Multiplex rates of up to 1 : 256
- Externally adjusted bias voltages
- Maximum LCD voltage and V_{DD} may be separated
- 64/65 pin programmable output operation mode
- Low power consumption
- Overall flat-panel power consumption minimized
- Pin programmable right/left orientation for convenience of flat-panel construction
- Optimized pinning for single plane wiring
- Space-saving 120-lead Tape-Automated Bonding package
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINE

PCF2201V: 120-lead Tape-Automated Bonding package.

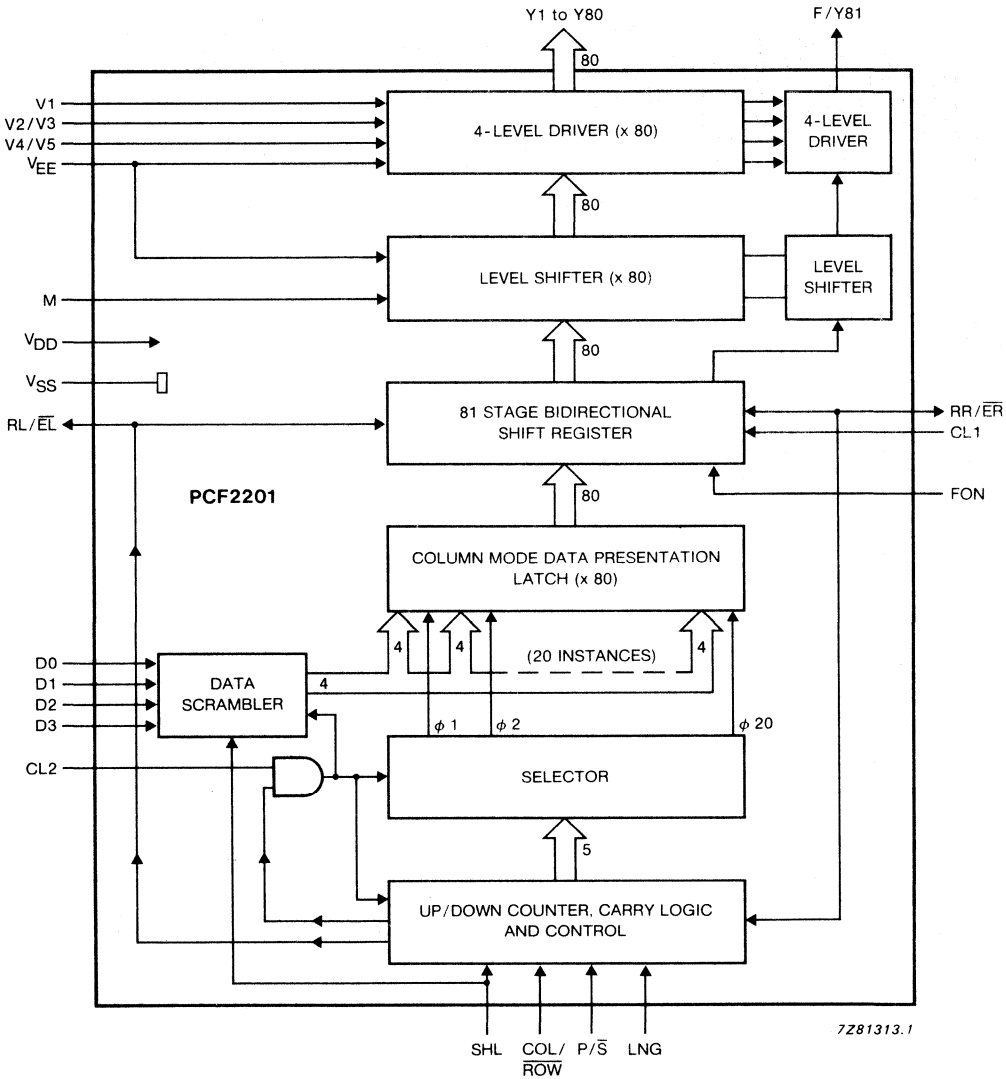


Fig. 1 Block diagram.

DEVELOPMENT DATA

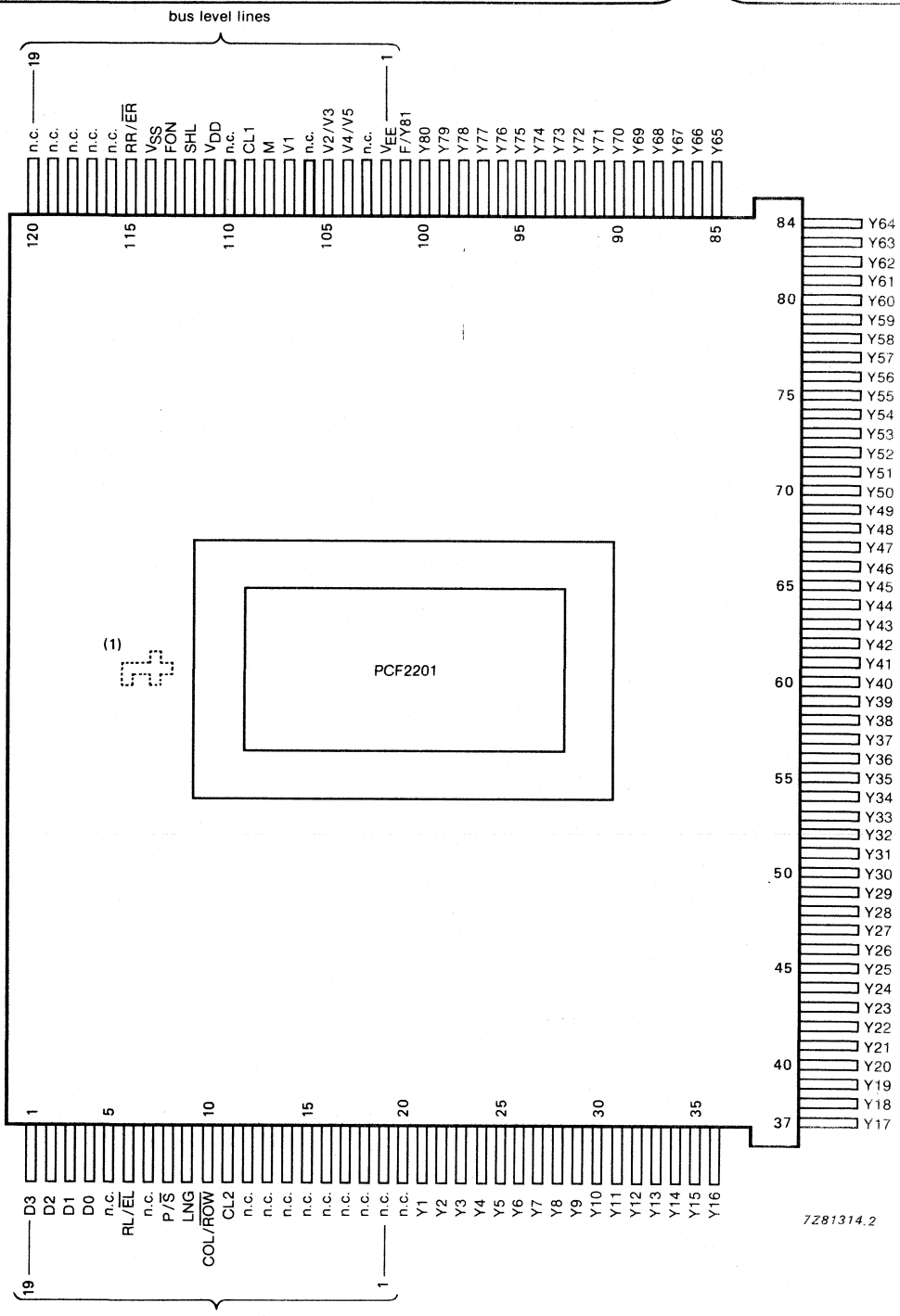


Fig. 2 Pinning diagram.

(1) mark orientation

PINNING FUNCTIONS

mnemonic	I/O	function
V_{DD}	P	Positive supply voltage (5 V)
V_{SS}	P	Logic ground (0 V)
V_1	P	Most positive LCD supply voltage ($\leqslant V_{DD}$), selection level
V_2/V_3	P	Upper non-selection level for row (V2) or column (V3) driver
V_4/V_5	P	Lower non-selection level for row (V5) or column (V4) driver
V_{EE}	P	Most negative LCD supply voltage (−20 V), selection level
Y1 to Y80	O	Liquid crystal driver outputs
CL1	I	Clock for 81 stage bidirectional shift register Loads parallel data from the data presentation latch and frame control in column driver mode Shifts data in row driver mode Negative edge triggered
CL2	I	Data transfer clock in column driver modes Data must be valid on the negative edge of CL2 Unused in row driver mode (may be left open)
COL/$\overline{\text{ROW}}$	I	Column/row driver mode select
P/$\overline{\text{S}}$	I	Parallel/serial mode select for column drivers Tie to V_{SS} in row driver mode
SHL	I	Shift direction select
D0 to D3	I	Data inputs in column driver modes Unused in row driver mode (may be left open) Filling order:

COL/$\overline{\text{ROW}}$	P/$\overline{\text{S}}$	SHL	D0	D1	D2	D3
H	L	L	Y1, Y2, Y3,.	unused	unused	unused
H	L	H	Y80, Y79,...	(may be left open)	(may be left open)	(may be left open)
H	H	L	Y1, Y5, Y9,.	Y2, Y6, Y10,.	Y3, Y7, Y11,.	Y4, Y8, Y12,..
H	H	H	Y80, Y76,...	Y79, Y75,....	Y78, Y74,....	Y77, Y73,.....

Also in the **serial** column driver mode, a multiple of 4 data bits must always be transferred. Add dummy bits if necessary

DEVELOPMENT DATA

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>RL/$\overline{EL}$
RR/$\overline{ER}$</td><td>I/O</td><td>Left/right serial input/outputs in row driver mode, left/right enable input/outputs in column driver modes
<table>
<tr><th>COL/$\overline{ROW}$</th><th>P/$\overline{S}$</th><th>SHL</th><th>RL/$\overline{EL}$</th><th>RR/$\overline{ER}$</th><th>comments</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>I</td><td>O</td><td>shift direction:
RL/$\overline{EL}$ –> RR/$\overline{ER}$ (Y1 –> F/Y81)</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>O</td><td>I</td><td>shift direction:
RR/$\overline{ER}$ –> RL/$\overline{EL}$ (F/Y81 –> Y1)</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>I</td><td>O</td><td>RR/$\overline{ER}$ goes LOW 80 CL2 pulses after RL/$\overline{EL}$</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>O</td><td>I</td><td>RL/$\overline{EL}$ goes LOW 80 CL2 pulses after RR/$\overline{ER}$</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>I</td><td>O</td><td>RR/$\overline{ER}$ goes LOW 20 CL2 pulses after RL/$\overline{EL}$</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>O</td><td>I</td><td>RL/$\overline{EL}$ goes LOW 20 CL2 pulses after RR/$\overline{ER}$</td></tr>
</table>
In the serial column mode, the device accepts one bit of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 80 bits of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data
The sequence is reset when CL1 is HIGH and CL2 is LOW

In the parallel column mode, the device accepts one nibble of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 20 nibbles of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data.
The sequence is reset when CL1 is HIGH and CL2 is LOW</td></tr>
<tr><td>LNG</td><td>I</td><td>Length control
<table>
<tr><th>COL/$\overline{ROW}$</th><th>LNG</th><th>SHL</th><th>description</th><th>valid Yi</th><th>undefined Yi</th></tr>
<tr><td>L
L</td><td>L
L</td><td>L
H</td><td>65-bit row mode
operation</td><td>Y1...Y65
Y17...Y80, F/Y81</td><td>Y66...Y80, F/Y81
Y1...Y16</td></tr>
<tr><td>L
L</td><td>H
H</td><td>L
H</td><td>81-bit row mode
operation</td><td>Y1...Y80, F/Y81
Y1...Y80, F/Y81</td><td>–
–</td></tr>
<tr><td>H
H</td><td>L
L</td><td>L
H</td><td>64-bit column
mode operation</td><td>Y1...Y64
Y17...Y80</td><td>Y65...Y80
Y1...Y16</td></tr>
<tr><td>H
H</td><td>H
H</td><td>L
H</td><td>80-bit column
mode operation</td><td>Y1...Y80
Y1...Y80</td><td>–
–</td></tr>
</table>
In 80/81-bit operation, the device behaves as previously described
In 64/65-bit operation, the device behaves as if all resources have been reduced to 64/65 instances; i.e. 16 outputs (determined by SHL) can no longer be accessed and should be left open circuit.</td></tr>
</table>

PINNING FUNCTIONS (continued)

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>F/Y81*</td><td>O</td><td>Frame output in column driver mode
It continuously delivers the select or non-select column driver LCD voltages depending on the state of the frame control
The frame output is used to blank the flat-panel display margin outside the actual LCD matrix
Liquid crystal driver output, number 81 in row driver mode</td></tr>
<tr><td>FON</td><td>I</td><td>Frame control
Defines the contents of the shift register cell corresponding to F/Y81 in column driver mode
Tie to V_{DD} or V_{SS} in row driver mode</td></tr>
<tr><td>M</td><td>I</td><td>Signal to convert LCD drive waveform into a.c.:
<table>
<tr><th>COL/$\overline{\text{ROW}}$</th><th>SR data</th><th>M</th><th>output level (Y_i or F/Y81)</th><th>note</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">row driver</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>V_{EE}</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V_1</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">column driver</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>V_1</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V_{EE}</td></tr>
</table></td></tr>
<tr><td>n.c.</td><td>–</td><td>not connected</td></tr>
</table>

* Patent application pending.

FUNCTIONAL DESCRIPTION

4-level driver

One of the liquid crystal driver levels (V_1, V_2/V_3, V_4/V_5 and V_{EE}) is output onto lines Y1 to Y80 and F/Y81 depending on the state of the relevant level shifter.

Level shifter

The level shifter converts logic level driver information into LCD level selection signals. The LCD level selection signals are dependent on the contents of the 81 stage bidirectional shift register and the state of signals M and COL/$\overline{\text{ROW}}$.

81 stage bidirectional shift register

In row driver mode the bidirectional shift register is used for the row line scan. In column driver mode the bidirectional shift register is used to hold column data until the next line is assembled in the data presentation latch.

Column mode data presentation latch

The column mode data presentation latch provides temporary storage during transfer of column data required for the next row.

Data scrambler

In serial column data transfer, the data scrambler converts 1-bit data to parallel 4-bit nibbles. Data is rearranged by the data scrambler according to the orientation (left or right) of the chip, as defined by pin SHL.

Selector

The selector generates latch clocks $\phi 1$ to $\phi 20$ for the presentation latch. Selection is determined by the state of the up/down counter and the carry logic.

Up/down counter, carry logic and control

Incoming column data storage locations are determined by the up/down counter making use of enable lines (RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$) and the length control select (LNG). The carry logic inhibits the data transfer clock (CL2) in inactive column drivers, thereby reducing power dissipation. When data transfer to one column driver is completed, the subsequent column driver is enabled by the carry logic. The control part co-ordinates the up/down counter and carry logic, depending upon the condition of the device (SHL, COL/$\overline{\text{ROW}}$, P/$\overline{\text{S}}$, LNG, RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	V_{SS} −0,3 to V_{SS} + 7	V
LCD supply voltage range	V_{EE}	V_{DD} −30 to V_{DD}	V
V_1, V_2/V_3 voltage range (note 1)	V_U	$\frac{V_{DD} + V_{EE}}{2}$ −1 to V_{DD}	V
V_4/V_5 voltage range (note 1)	V_L	V_{EE} to $\frac{V_{DD} + V_{EE}}{2}$ − 1	V
Input voltage range (CL1, CL2, COL/$\overline{\text{ROW}}$, P/$\overline{\text{S}}$, SHL, D0, D1, D2, D3, RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$, LNG, FON, M)	V_I	V_{SS} −0,3 to V_{DD} + 0,3	V
Output voltage range (RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$)	V_O	V_{SS} −0,3 to V_{DD} + 0,3	V
Driver output voltage range (F/Y81, Y1 to Y80)	V_Y	V_{EE} −0,3 to V_{DD} + 0,3	V
DC input current	$\pm I_I$	max. 20	mA
DC output current	$\pm I_O$	max. 25	mA
V_{DD}, V_{SS}, V_1, V_2/V_3, V_4/V_5 or V_{EE} current	$\pm I_{SUP}$	max. 20	mA
Power dissipation per package	P_{tot}	max. 400	mW
Power dissipation per output	P_o	max. 100	mW
Storage temperature range	T_{stg}	−65 to + 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 4,5 to 5,5 V;

V_{EE} = 0 to −20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\ V \geqslant V_4/V_5 \geqslant V_{EE}$; f_M = 100 Hz

T_{amb} = −40 to + 85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Positive supply voltage		V_{DD}	4,5	–	5,5	V
Negative LCD supply voltage		V_{EE}	V_{DD}−25	–	V_{DD}−5	V
Static supply current	$f_{CL1} = f_{CL2}$ = 0 Hz; COL/$\overline{\text{ROW}}$ = H; M = L; note 2	I_{DD1}	–	15	40	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; f_{CL1} = 25 kHz; f_{CL2} = 4 MHz; note 2	I_{DD2}	–	0,4	1	mA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; RL/$\overline{\text{EL}}$ = H (SHL = L) or RR/$\overline{\text{ER}}$ = H (SHL = H); f_{CL1} = 25 kHz; note 2	I_{DD3}	–	50	150	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = L; f_{CL1} = 100 kHz; note 2	I_{DD4}	–	75	200	μA
Logic						
Input voltage LOW		V_{IL}	0	–	0,3 V_{DD}	V
HIGH		V_{IH}	0,7 V_{DD}	–	V_{DD}	
Output voltage LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OH}	V_{DD}−0,05	–	–	V
Output current LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	V_{OL} = 1 V	I_{OL}	1	–	–	mA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output current HIGH RL/$\overline{EL}$ and RR/$\overline{ER}$	$V_{OH} = V_{DD}-1$ V	I_{OH}	–	–	1	mA
Leakage current at CL1, CL2, COL/$\overline{ROW}$, P/$\overline{S}$, SHL, D0 to D3, RL/$\overline{EL}$, RR/$\overline{ER}$, LNG, FON and M		$\pm I_{L1}$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	7	pF
LCD outputs						
Leakage current at V_1, V_2/V_3, V_4/V_5		$\pm I_{L2}$	–	–	2	μA
Resistance ON between V_1, V_2/V_3, V_4/V_5, V_{EE} and Y1 to Y80, F/Y81	$I_O = 100$ μA; $V_{EE} = V_{DD}-25$ V note 4	R_{ON}	–	–	2	kΩ

AC CHARACTERISTICS (note 5)

$V_{SS} = 0$ V; $V_{DD} = 4{,}5$ to $5{,}5$ V;
$V_{EE} = 0$ to -20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\text{ V} \geqslant V_4/V_5 \geqslant V_{EE}$;
$f_M = 100$ Hz; see Figs 4 and 5; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Column driver data transfer rate		f_{CL2}	–	–	4	MHz
CL2 HIGH time		t_{CL2H}	100	–	–	ns
CL2 LOW time		t_{CL2L}	100	–	–	ns
CL2 rise time		t_{CL2r}	–	–	25	ns
CL2 fall time		t_{CL2f}	–	–	25	ns
Row driver clock rate		f_{CL1}	–	–	100	kHz
CL1 HIGH time		t_{CL1H}	275	–	–	ns
CL1 LOW time		t_{CL1L}	5	–	–	μs
CL1 rise time		t_{CL1r}	–	–	50	ns
CL1 fall time		t_{CL1f}	–	–	50	ns

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Column data set-up time	COL/$\overline{\text{ROW}}$ = H	t_{SUC}	50	–	–	ns
Column data hold time	COL/$\overline{\text{ROW}}$ = H	t_{HDC}	30	–	–	ns
Row data set-up time	COL/$\overline{\text{ROW}}$ = L	t_{SUR}	200	–	–	ns
Row data hold time	COL/$\overline{\text{ROW}}$ = L	t_{HDR}	0	–	–	ns
Enable HIGH to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECH}	90	–	–	ns
Enable LOW to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECL}	85	–	–	ns
Propagation delay to enable HIGH	COL/$\overline{\text{ROW}}$ = H	t_{PEH}	–	–	185	ns
Propagation delay to enable LOW	COL/$\overline{\text{ROW}}$ = H	t_{PEL}	–	–	140	ns
CL2 to CL1 time	COL/$\overline{\text{ROW}}$ = H	t_{CL21}	50	–	–	ns
CL1 to CL2 time	COL/$\overline{\text{ROW}}$ = H	t_{CL12}	50	–	–	ns
Overlap time of CL2 = LOW and CL1 = HIGH	COL/$\overline{\text{ROW}}$ = H	t_{ov}	275	–	–	ns
Propagation delay HIGH to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PLH}	20	–	200	ns
Propagation delay LOW to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PHL}	20	–	200	ns
Propagation delay to Y1 . . . Y80, F/Y81	$V_{EE} = V_{DD}$ −20 V	t_{PY}	–	–	3	μs

Notes to characteristics

1. Maintain $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\ V \geqslant V_4/V_5 \geqslant V_{EE}$.
2. Outputs open, inputs at V_{SS} or V_{DD}.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

Fig. 3 Test loads.

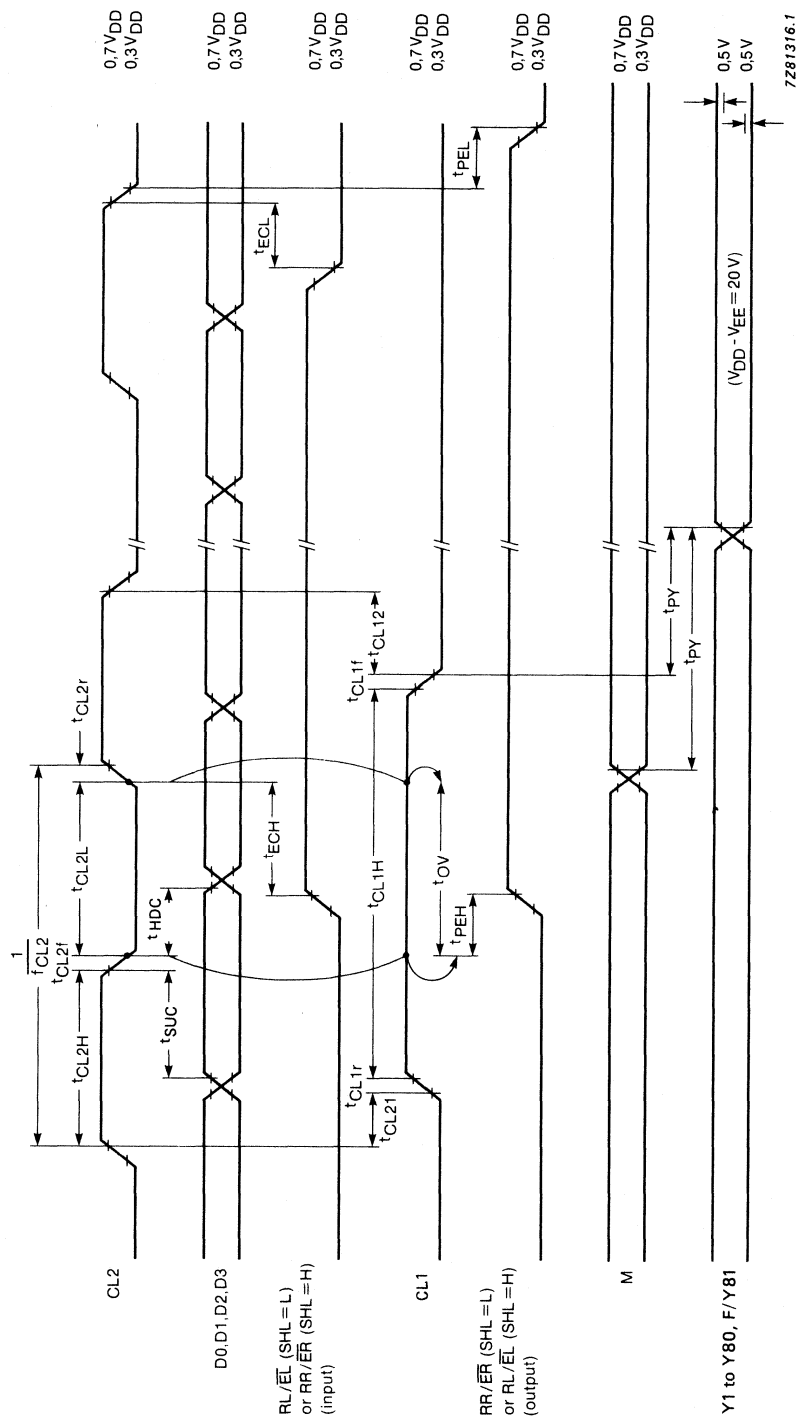


Fig. 4 Column driver timing waveforms.

DEVELOPMENT DATA

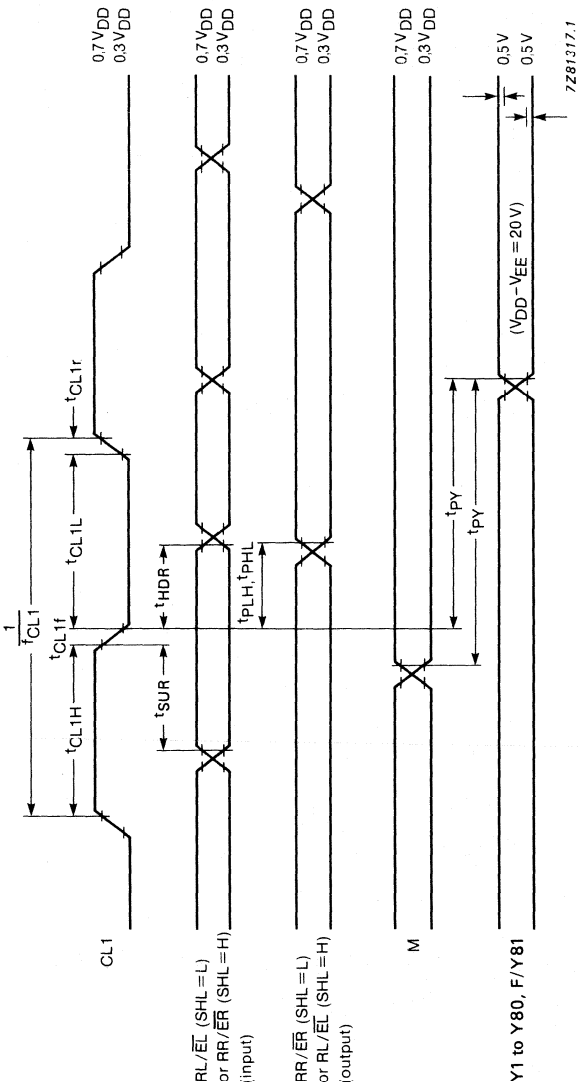


Fig. 5 Row driver timing waveforms.

APPLICATION INFORMATION

Generation of LCD bias levels

Optimum contrast for LCD flat-panels is achieved when the bias levels are selected using the formulae in Table 1. The multiplex rate is denoted by the variable n ($n \geqslant 9$). V_{th} is defined as the LCD threshold voltage, typically where the LCD exhibits approximately 10% contrast. The ratio of the 'ON' voltage to the 'OFF' voltage is discrimination (D) and is a measure of the flat-panel contrast at a given multiplex rate.

Table 1 LCD flat-panel bias levels for optimum contrast ($V_{op} = V1 - V_{EE}$)

$\frac{V_2}{V_{op}} = \frac{\sqrt{n}}{\sqrt{n}+1}$	$\frac{V_3}{V_{op}} = \frac{\sqrt{n}-1}{\sqrt{n}+1}$	$\frac{V_4}{V_{op}} = \frac{2}{\sqrt{n}+1}$	$\frac{V_5}{V_{op}} = \frac{1}{\sqrt{n}+1}$
$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$		$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n}+\frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$	
$D = \frac{V_{on(rms)}}{V_{off(rms)}} = \frac{\sqrt{n-1}}{\sqrt{n}-1}$		$\frac{V_{op}}{V_{th}} = \frac{\sqrt{n}+1}{\sqrt{2(1-1/\sqrt{n}}}$	

The intermediate bias levels are generated by a resistive divider (see Fig. 6). Capacitors (C) are used to smooth out switching transients. Considerable power consumption may result by using this arrangement when driving a large LCD flat-panel, because of the low impedance of the resistive divider.

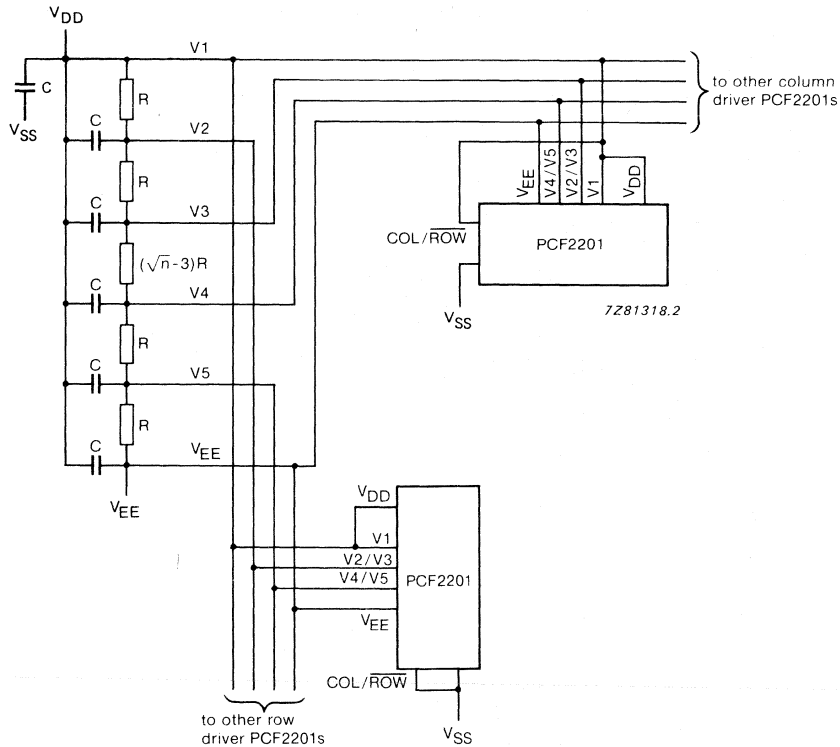


Fig. 6 Unbuffered LCD biasing level generation.

DEVELOPMENT DATA

A better solution for LCD flat-panel biasing is presented in Fig. 7. The operational amplifiers provide low impedance biasing with a low power consumption. The fairly high impedance which can be implemented at the resistive divider, helps maintain low power consumption. One diode voltage drop seperates V1 from V_{DD} to compensate for the limited common mode voltage range (V+ −1,5 V) when the operational amplifiers are powered between V_{DD} and V_{EE}.

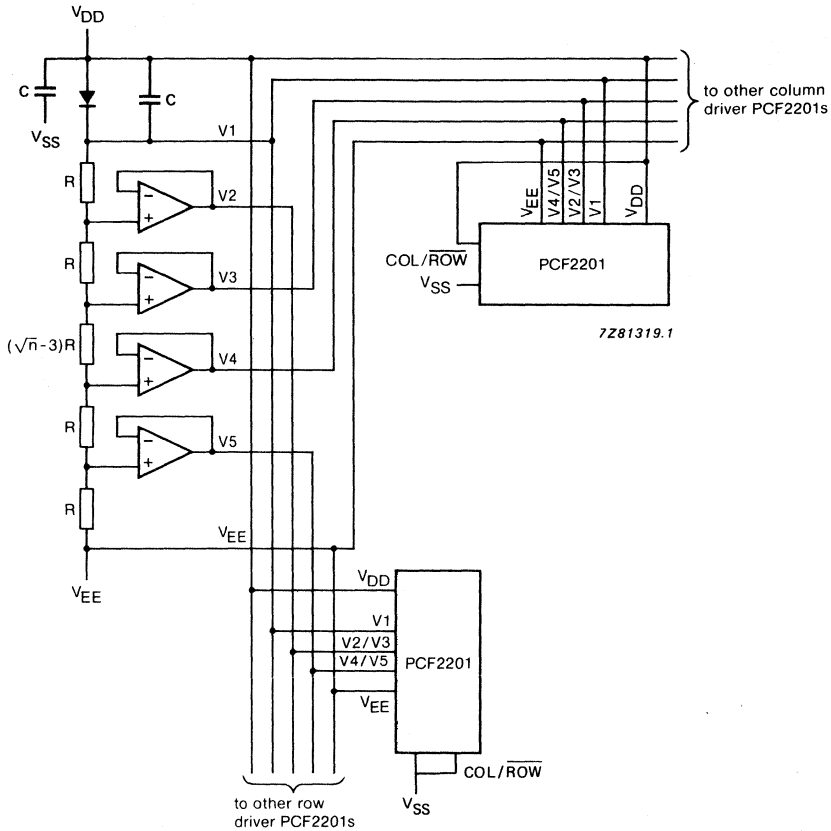


Fig. 7 Buffered LCD bias level generation.

Typical LCD flat-panel application

Alphanumeric/graphic computer terminals with LCD flat-panel screens using 200 x 640 dots are very popular. The format of 200 x 640 is compatible with the standard 25 lines by 80 characters at 8 x 8 dot character fonts. Fig. 8 gives a possible circuit using 19 PCF2201's, with upper and lower half screens used for good contrast. The use of half screens reduces the multiplex rate to 1:100 (Fig. 9 gives the timing information).

DEVELOPMENT DATA

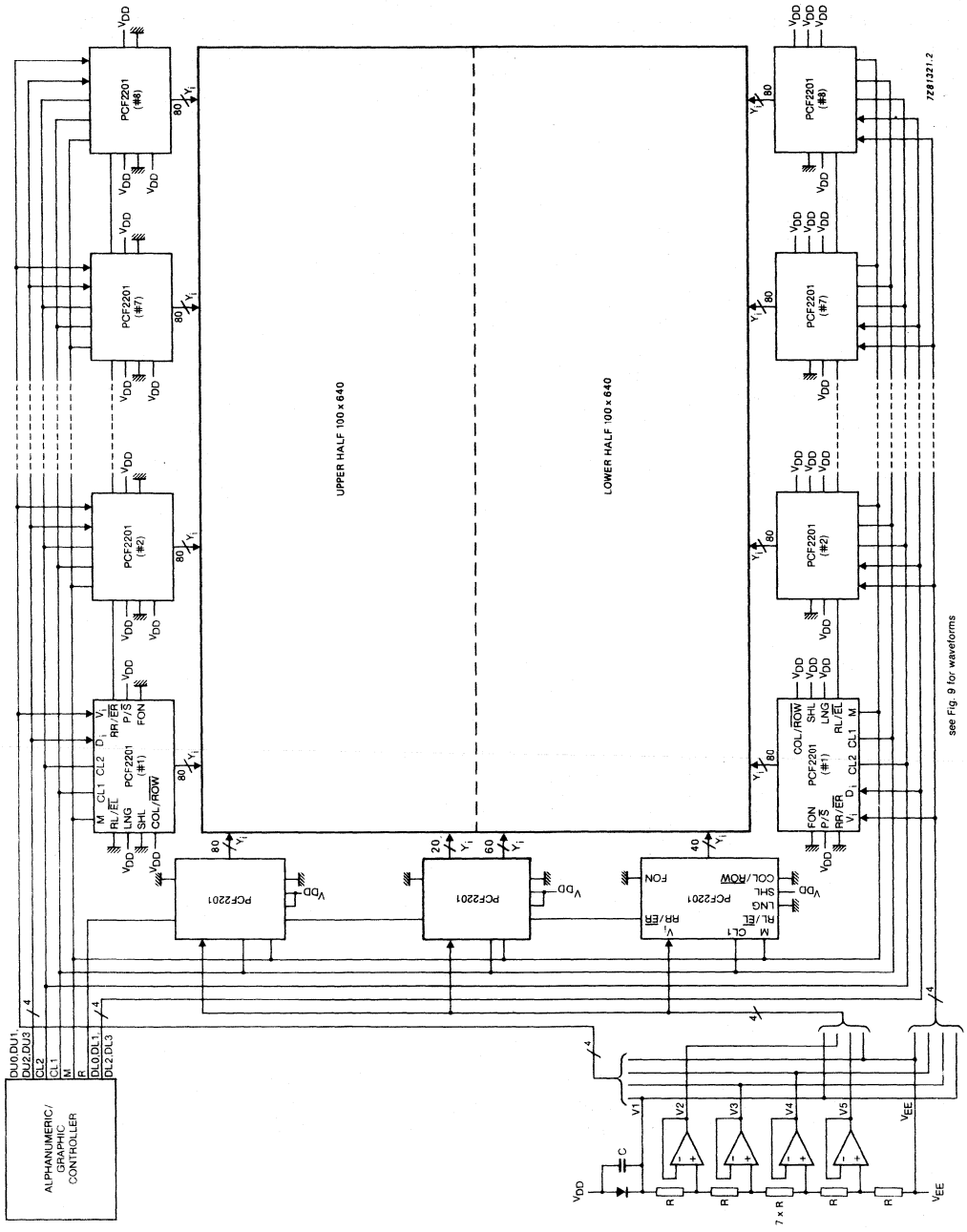


Fig. 8 LCD flat-panel with 1:100 multiplex rate in upper and lower half screens.

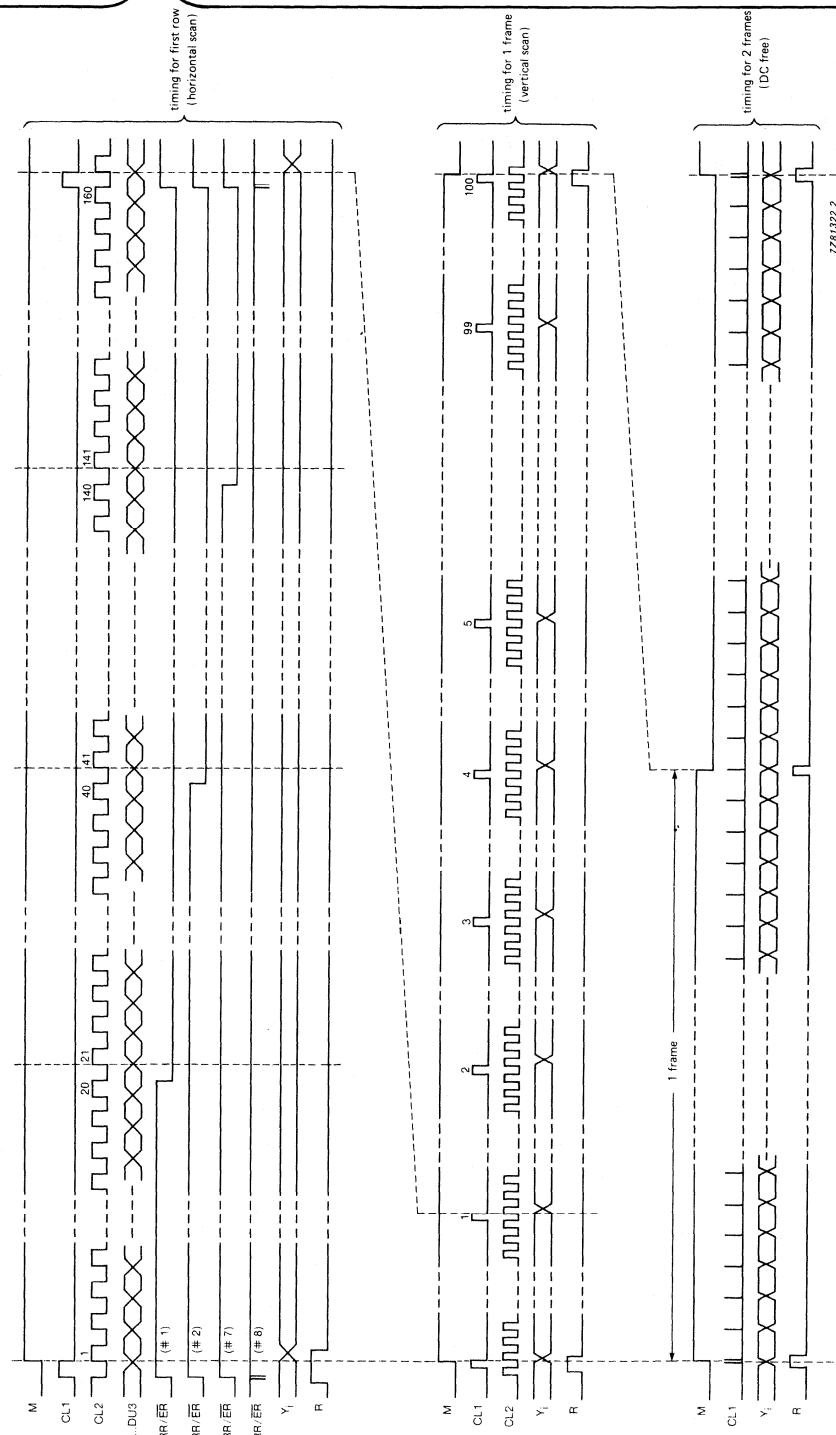
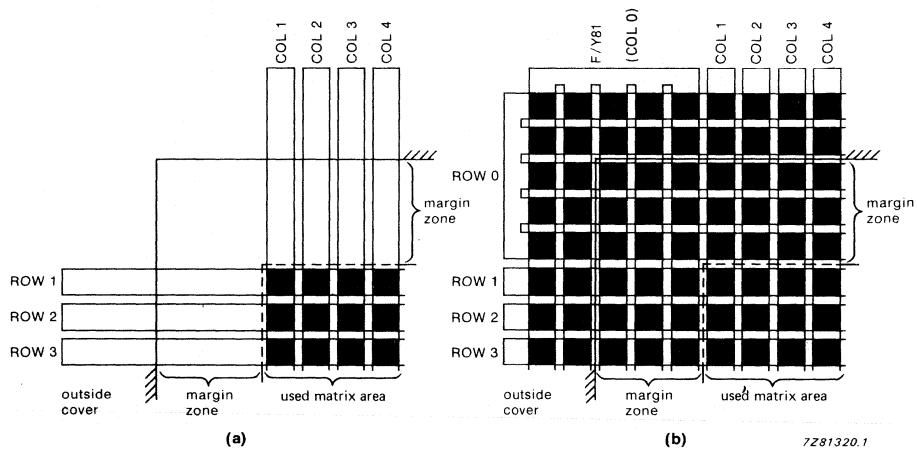


Fig. 9 Timing for the upper half screen of the LCD flat-panel (Fig. 8). For the lower half screen, replace RR/$\overline{ER}$, DU0, DU1, DU2 and DU3 with RL/$\overline{EL}$, DL0, DL1, DL2, DL3.

Margin control

The used area of the flat-panel matrix is normally smaller than the LCD glass surface. Connection lines outside of the used area of the matrix carry row or column LCD signals (see Fig. 10A). This 'null' state differs slightly in colour from the 'OFF' state pixel for twisted nematic LCD. The structural change in the margin zone is noticeable.

When a high contrast Philips LCD flat-panel of the supertwisted birefringence effect (SBE) type is employed, the situation becomes critital. The colour of the 'OFF' state appears blue and the colour of the 'ON' state appears grey or white. Therefore inverted information is sent to the display, generating dark (blue) characters on a light (grey) background. The margin zone is treated as an extension of the used matrix area (see Fig. 10B), to avoid the margin zone appearing as a dark blue frame. This is extended out to a region where the LCD glass can be covered up. The additional row requires an increase in the multiplex rate from n to n + 1, the additional column is realized by the frame output of the furthest left and right column drivers of the flat-panel. This removes the requirement for additional column drivers packages to provide margin control.



(A) without margin control

(B) with margin control

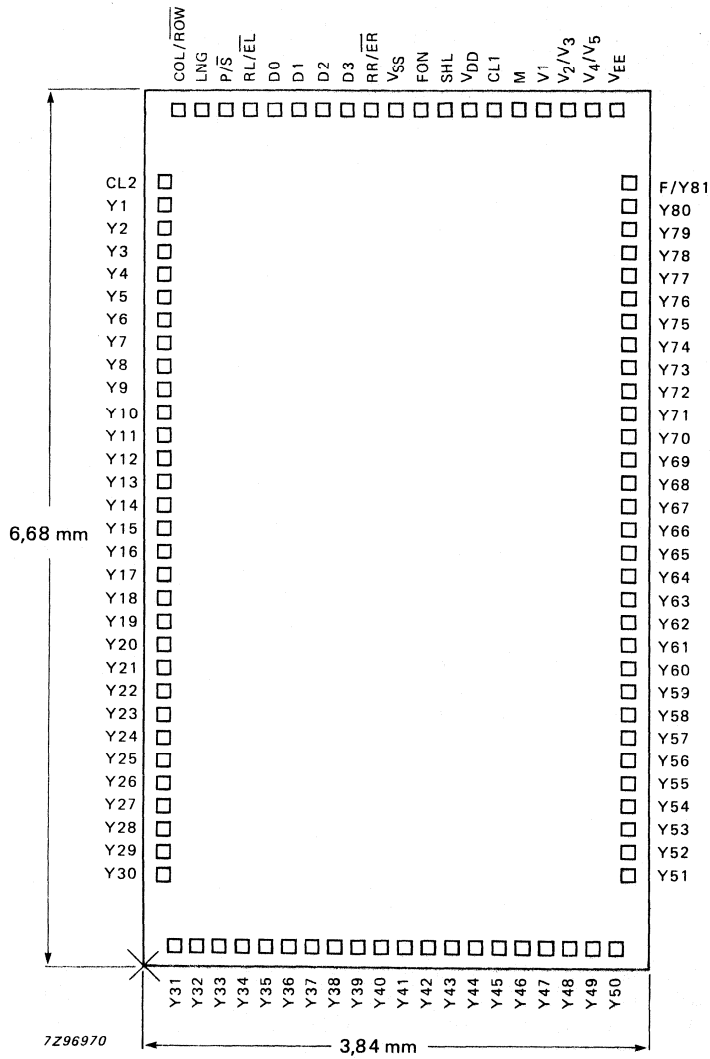
Fig. 10 Upper left corner of the LCD flat-panel.

Single plane wiring

The pinning of the PCF2201 tape-automated bonding package has been selected for ease of wiring. One side of this package contains no pins. The adjacent logic level lines are arranged so that they can be bussed in a single plane on the printed circuit board, which allows single sided substrates to be used.

For ease of wiring layout it is suggested to use the bus-level numbers (see Fig. 2) since most supply lines can be run through at the same level. On the actual package there are 120 pins, of which 19 pins are not internally connected. These extra pins are due to single plane wiring gaps and enhance stability in surface mounting.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 25,65 mm^2

Bonding pad dimensions: 104 μm x 104 μm

Fig. 11 Bonding pad locations.

Table 2 Bonding pad centre locations (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left corner, see Fig. 11.

pad	X	Y	pad	X	Y
D3	1556	6526	Y43	2364	154
D2	1372	6526	Y44	2540	154
D1	1188	6526	Y45	2716	154
D0	1004	6526	Y46	2892	154
RL/$\overline{EL}$	820	6526	Y47	3068	154
P/$\overline{S}$	636	6526	Y48	3244	154
LNG	452	6526	Y49	3420	154
COL/$\overline{ROW}$	268	6526	Y50	3596	154
CL2	156	5982	Y51	3684	702
Y1	156	5806	Y52	3684	878
Y2	156	5630	Y53	3684	1054
Y3	156	5454	Y54	3684	1230
Y4	156	5278	Y55	3684	1406
Y5	156	5102	Y56	3684	1582
Y6	156	4926	Y57	3684	1758
Y7	156	4750	Y58	3684	1934
Y8	156	4574	Y59	3684	2110
Y9	156	4398	Y60	3684	2286
Y10	156	4222	Y61	3684	2462
Y11	156	4046	Y62	3684	2638
Y12	156	3870	Y63	3684	2814
Y13	156	3694	Y64	3684	2990
Y14	156	3518	Y65	3684	3166
Y15	156	3342	Y66	3684	3342
Y16	156	3166	Y67	3684	3518
Y17	156	2990	Y68	3684	3694
Y18	156	2814	Y69	3684	3870
Y19	156	2638	Y70	3684	4046
Y20	156	2462	Y71	3684	4222
Y21	156	2286	Y72	3684	4398
Y22	156	2110	Y73	3684	4574
Y23	156	1934	Y74	3684	4750
Y24	156	1758	Y75	3684	4926
Y25	156	1582	Y76	3684	5102
Y26	156	1406	Y77	3684	5278
Y27	156	1230	Y78	3684	5454
Y28	156	1054	Y79	3684	5630
Y29	156	878	Y80	3684	5806
Y30	156	702	F/Y81	3684	5982
Y31	252	154	V_{EE}	3580	6526
Y32	428	154	V_4/V_5	3396	6526
Y33	604	154	V_2/V_3	3212	6526
Y34	780	154	V1	3028	6526
Y35	956	154	M	2844	6526
Y36	1132	154	CL1	2660	6526
Y37	1308	154	V_{DD}	2476	6526
Y38	1484	154	SHL	2292	6526
Y39	1660	154	FON	2108	6526
Y40	1836	154	V_{SS}	1924	6526
Y41	2012	154	RR/$\overline{ER}$	1740	6526
Y42	2188	154			

DEVELOPMENT DATA

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 3 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PFC8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specification defined by Philips.

PACKAGE OUTLINES

PCF8566T: 40-lead mini-pack; (VSO-40; SOT-158A).
PCF8566P: 40-lead DIL; plastic (SOT-129).

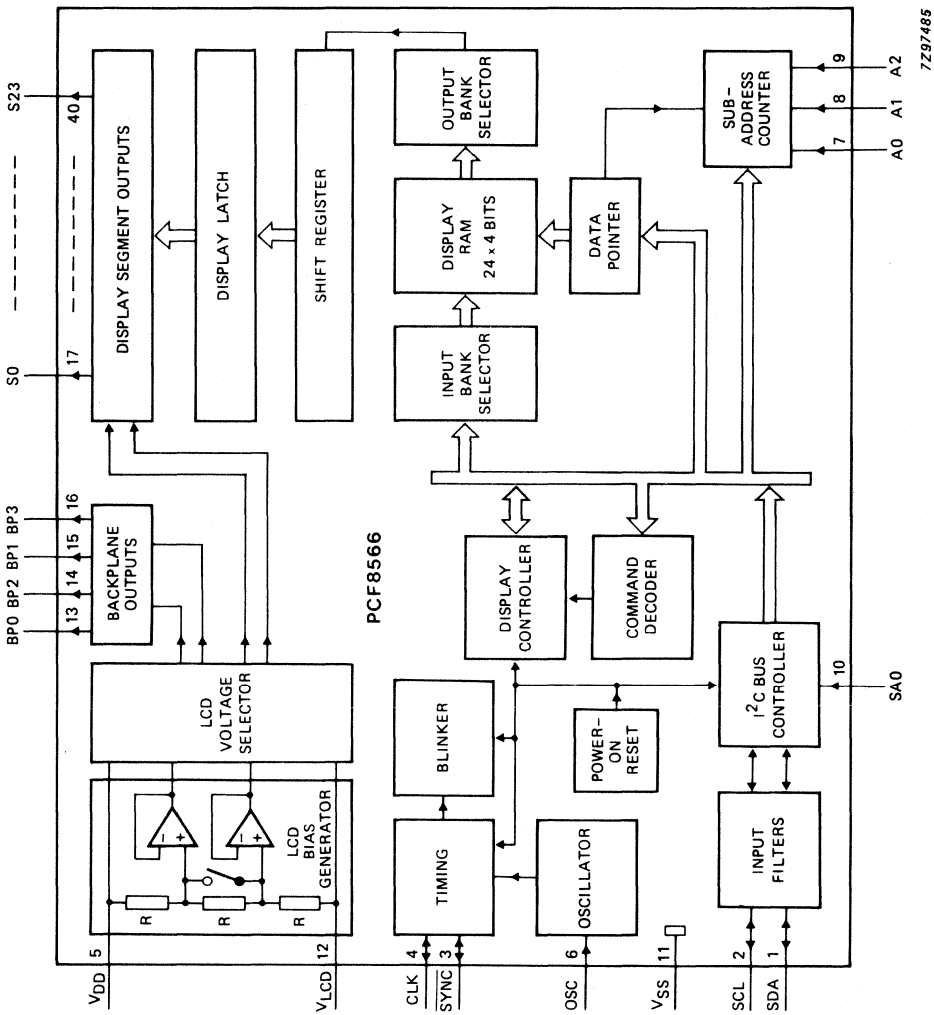


Fig. 1 Block diagram.

DEVELOPMENT DATA

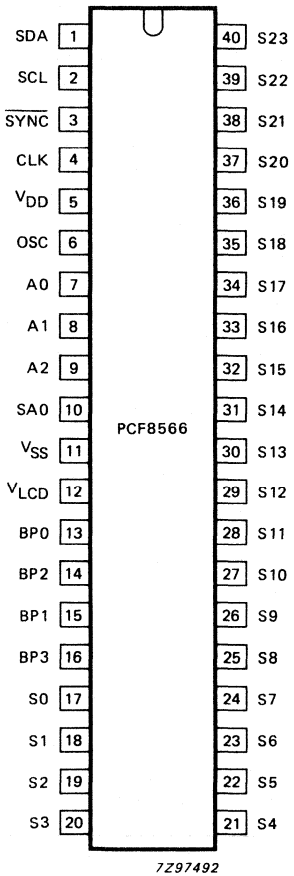


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	I^2C bus subaddress inputs
9	A2	I^2C bus subaddress inputs
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	LCD backplane outputs
15	BP1	LCD backplane outputs
16	BP3	LCD backplane outputs
17 to 40	S0 to S23	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 characters + 10 indicator symbols	24 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the two-line I^2C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

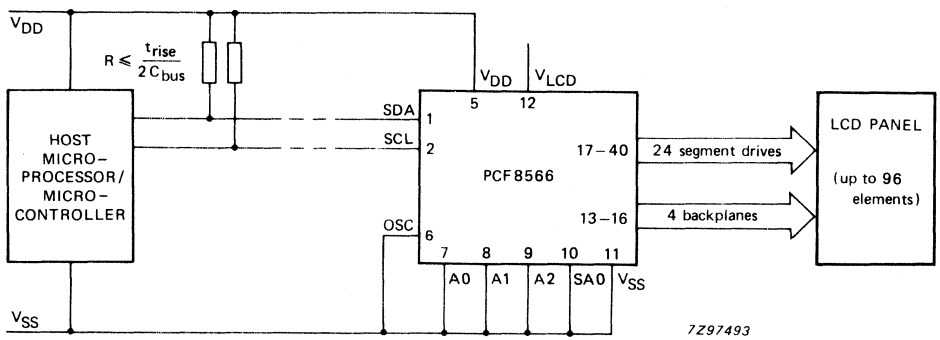


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generation

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

DEVELOPMENT DATA

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.

Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex). The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off(rms)} = 2{,}449\ V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off(rms)} = 2{,}309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

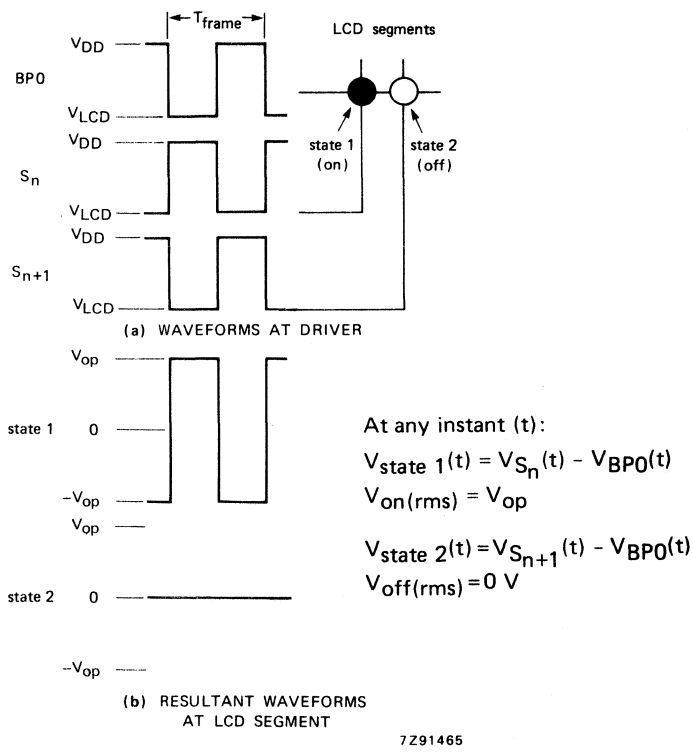


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

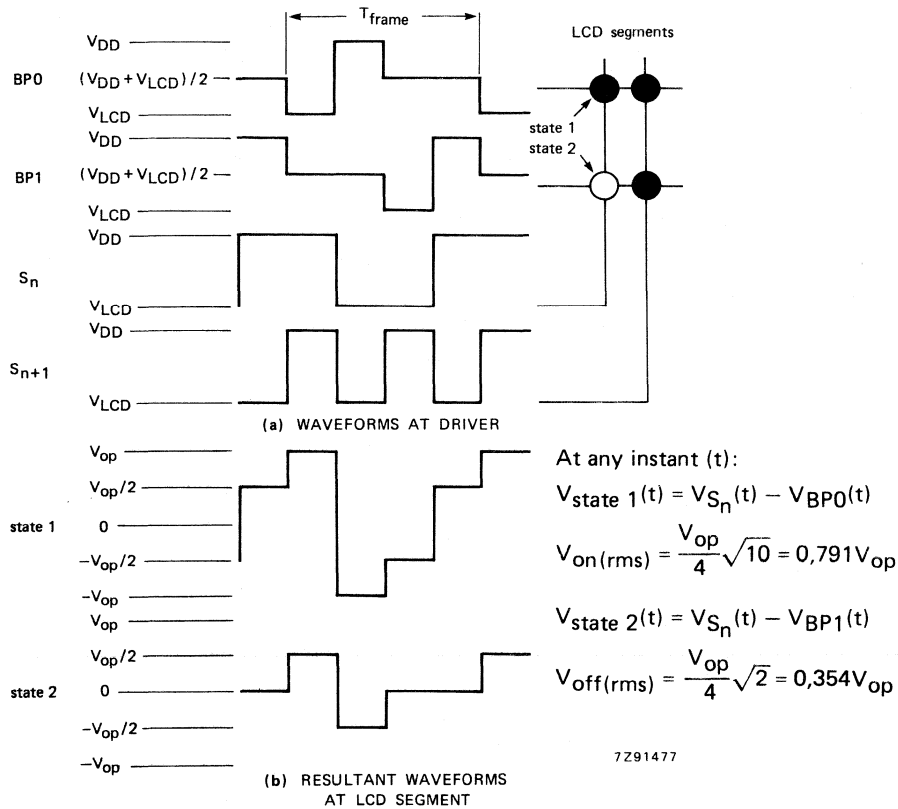


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

DEVELOPMENT DATA

LCD drive mode waveforms (continued)

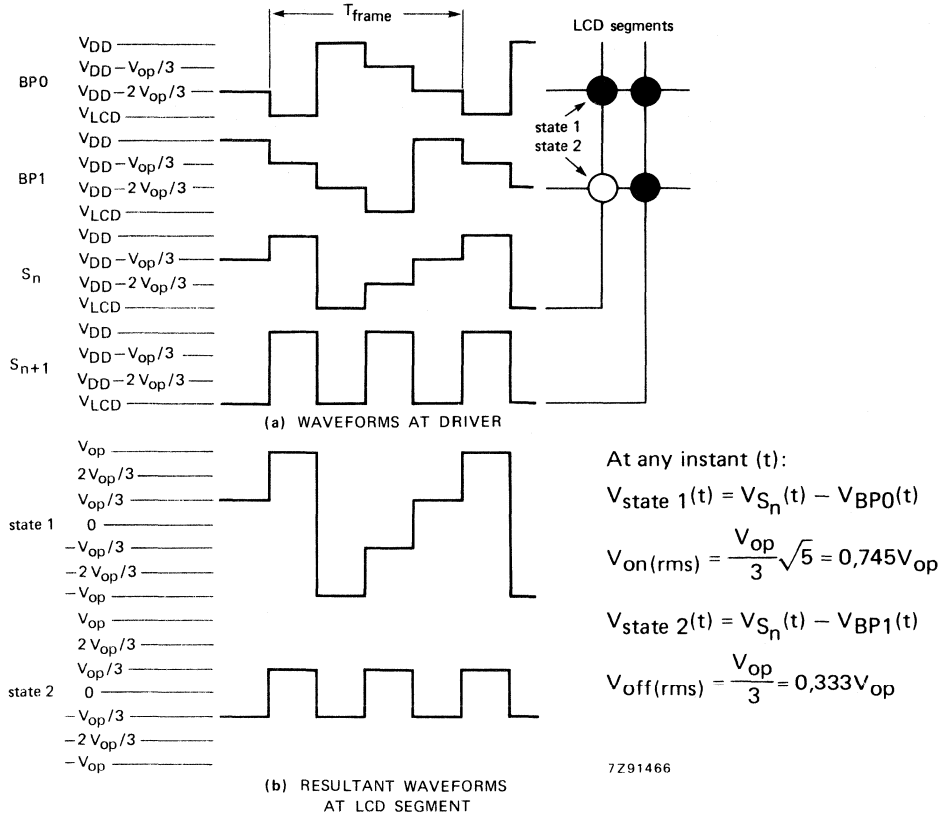


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

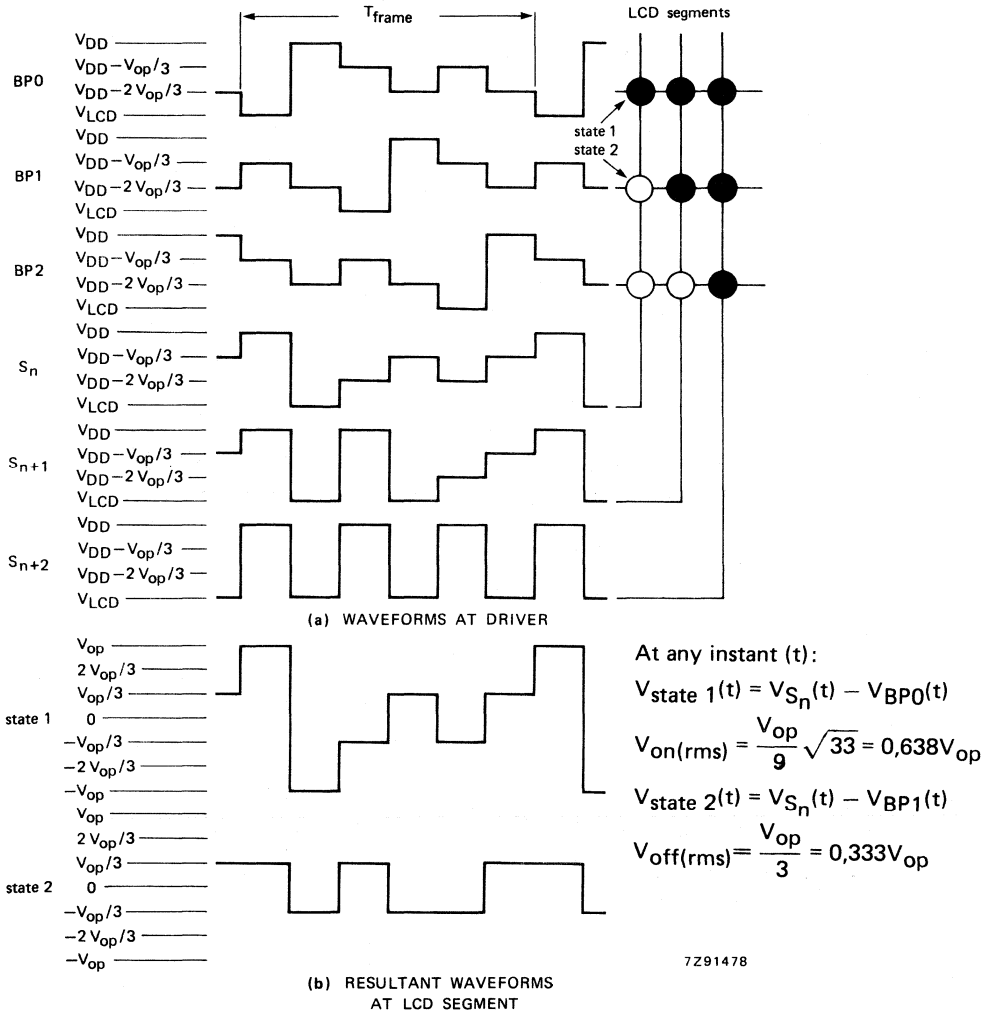


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

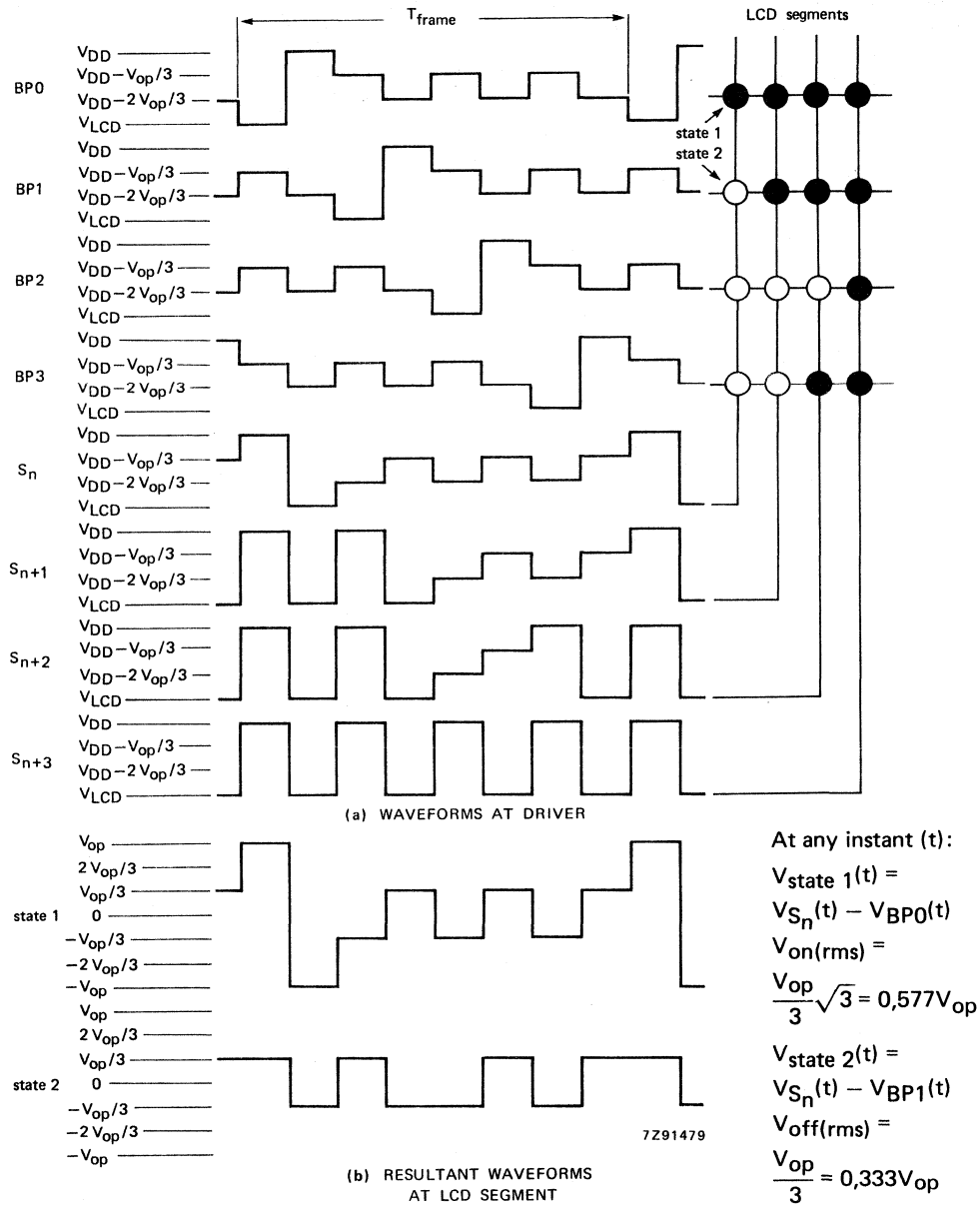


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8566 mode	f_{frame}	nominal f_{frame} (Hz)
normal mode	$f_{CLK}/2880$	64
power-saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller, this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Fig. 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

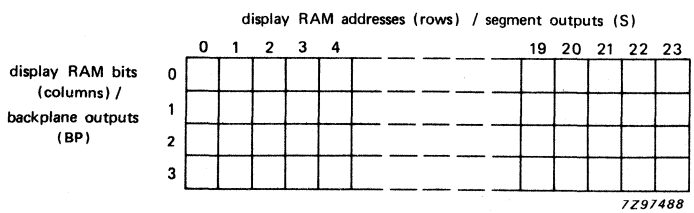


Fig. 9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

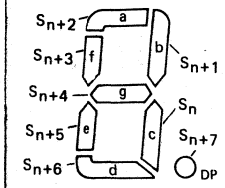
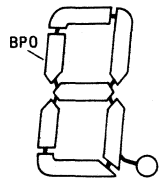
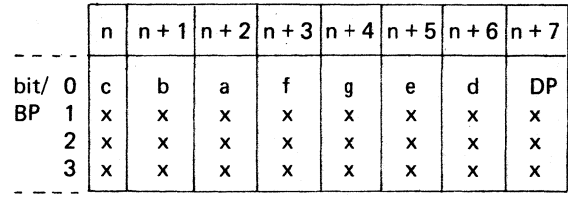
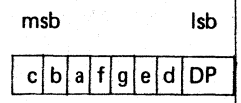
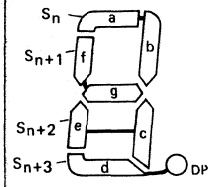
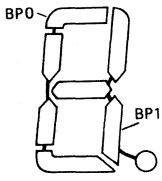
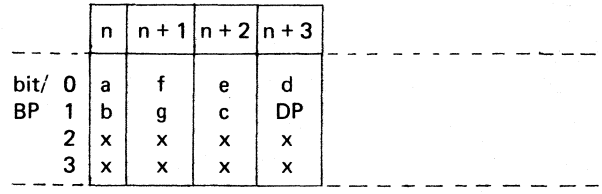
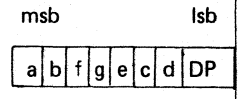
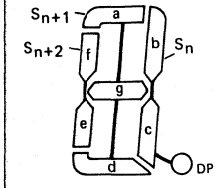
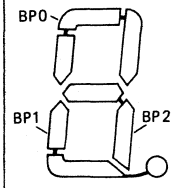
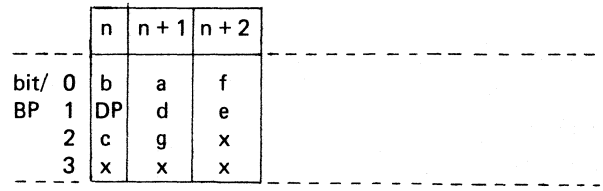
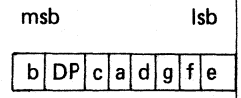
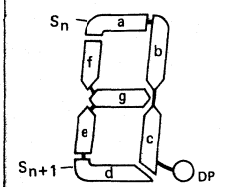
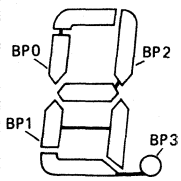
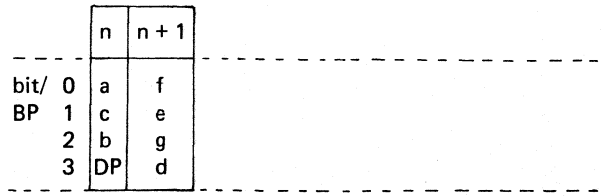
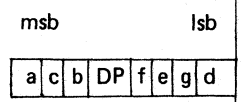
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

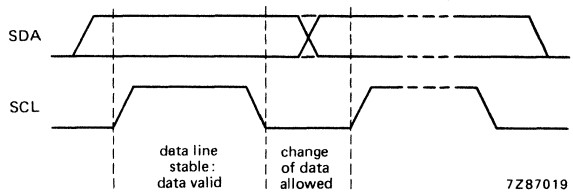


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

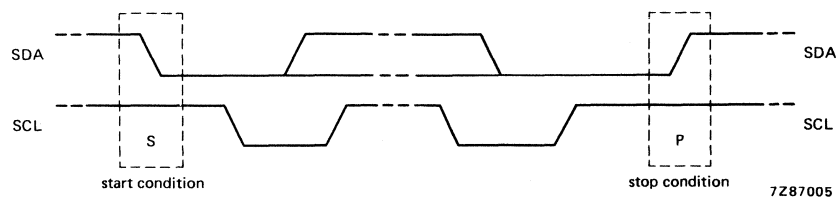


Fig. 12 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

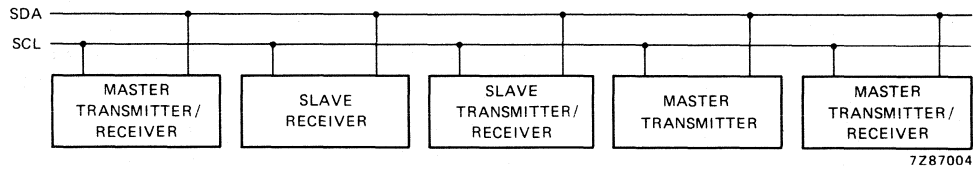


Fig. 13 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

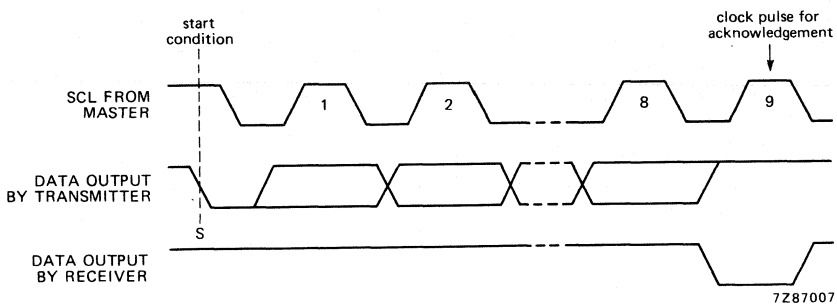


Fig. 14 Acknowledgement on the I²C bus.

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8566 I²C bus controller

The PCF8566 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open or tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8566s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 15. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C bus master issues a stop condition (P).

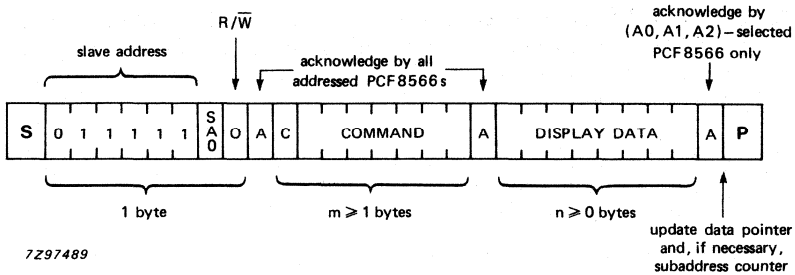


Fig. 15 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

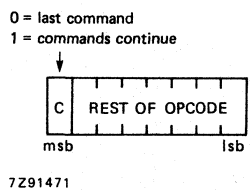


Fig. 16 General format of command byte.

The five commands available to the PCF8566 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8566 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 0 P4 P3 P2 P1 P0	bits P4 P3 P2 P1 P0 5-bit binary value of 0 to 23	Five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

DEVELOPMENT DATA

command/opcode	options	description
BANK SELECT C 1 1 1 1 0 I O	static / 1 : 2 MUX / bit I RAM bit 0 / RAM bits 0, 1 / 0 RAM bit 2 / RAM bits 2, 3 / 1 static / 1 : 2 MUX / bit O RAM bit 0 / RAM bits 0, 1 / 0 RAM bit 2 / RAM bits 2, 3 / 1	Defines input bank selection (storage of arriving display data) Defines output bank selection (retrieval of LCD display data) The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
BLINK C 1 1 1 0 A BF1 BF0	blink frequency / bits BF1 / BF0 off / 0 / 0 2 Hz / 0 / 1 1 Hz / 1 / 0 0,5 Hz / 1 / 1 blink mode / bit A normal blinking / 0 alternation blinking / 1	Defines the blinking frequency Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 17).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Casadability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

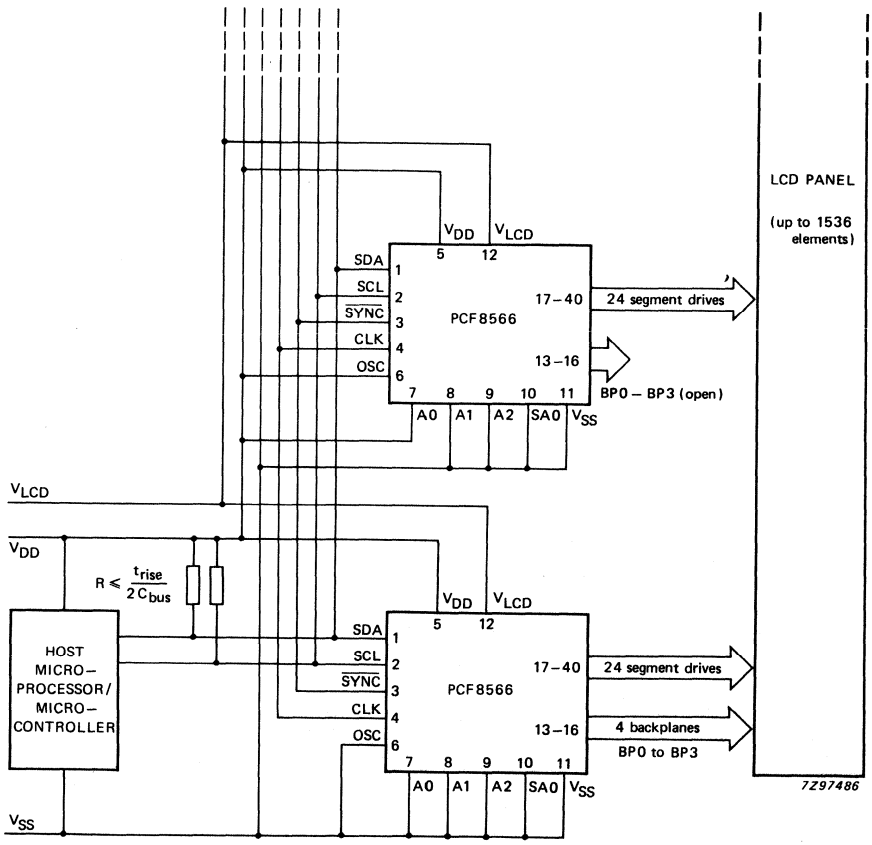


Fig. 17 Cascaded PCF8566 configuration.

DEVELOPMENT DATA

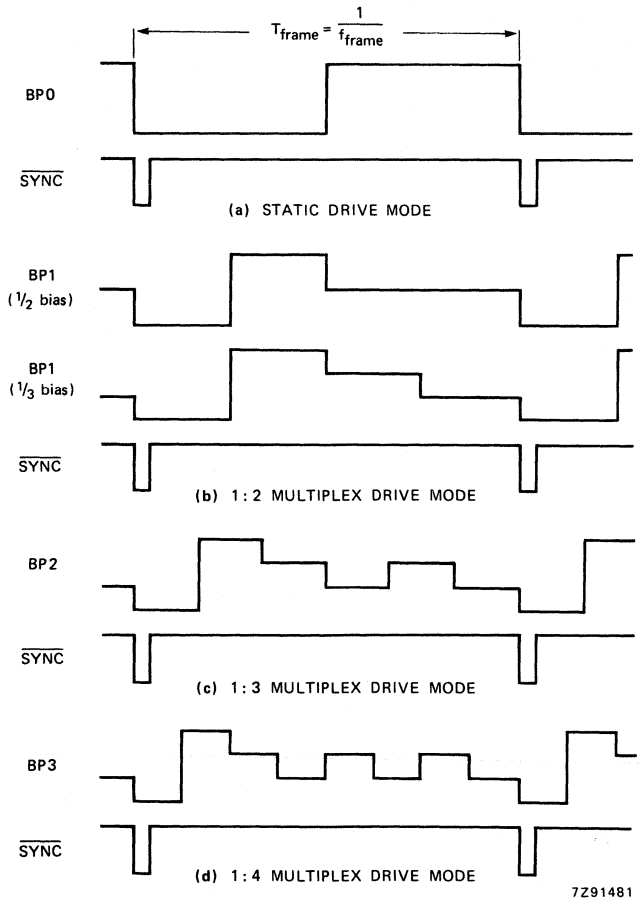


Fig. 18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see section "APPLICATION INFORMATION".

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}		−0,5 to + 7 V
LCD supply voltage range	V_{LCD}		V_{DD} −7 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S23; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5 V
D.C. input current	$\pm I_I$	max.	20 mA
D.C. output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 3 to 6 V; V_{LCD} = V_{DD} −3 to V_{DD} −6 V;

T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	3	–	6	V
LCD supply voltage	V_{LCD}	V_{DD} −6	–	V_{DD} −3	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	–	180	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	–	60	μA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} –0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	–1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SAO, CLK, OSC, A0, A1, A2, SCL, SDA) at $V_I = V_{SS}$ or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	1,8	V
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 3 to 6 V; V_{LCD} = V_{DD} −3 to V_{DD} −6 V;

T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

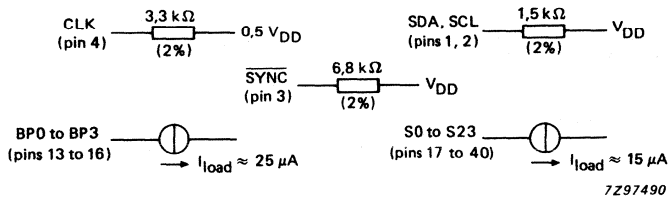


Fig. 19 Test loads.

DEVELOPMENT DATA

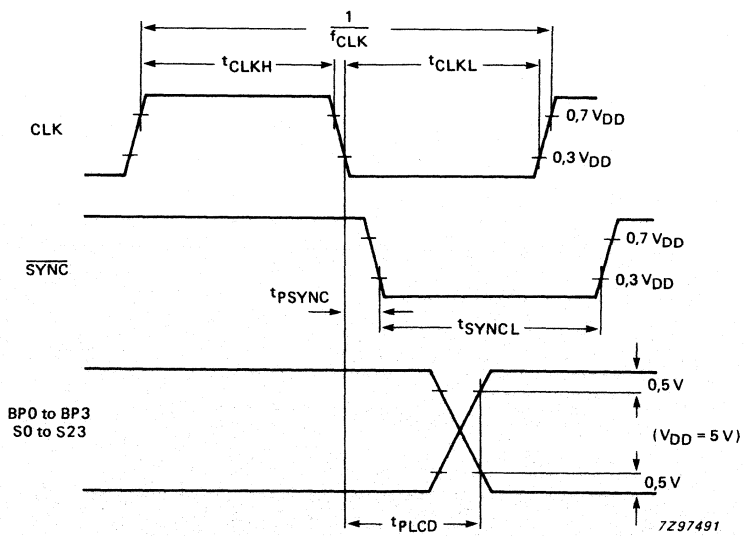


Fig. 20 Driver timing waveforms.

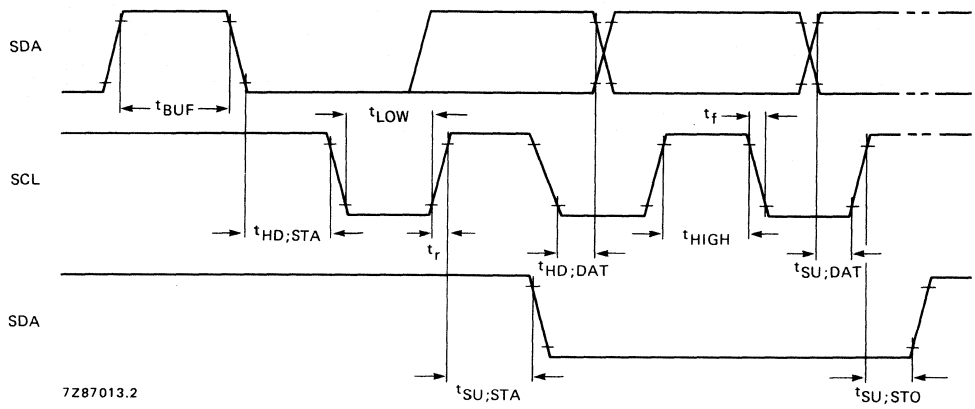
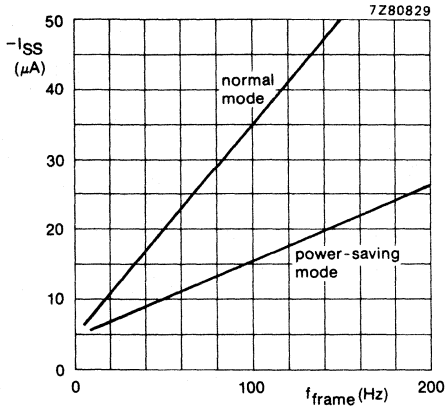
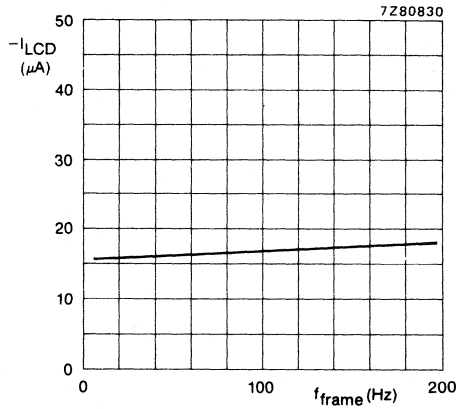


Fig. 21 I^2C bus timing waveforms.

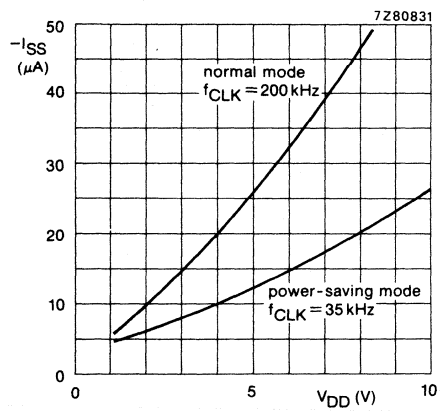
DEVELOPMENT DATA



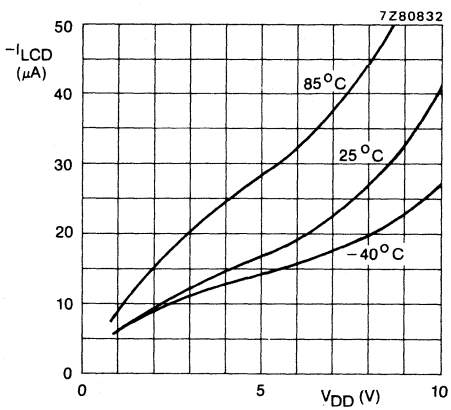
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

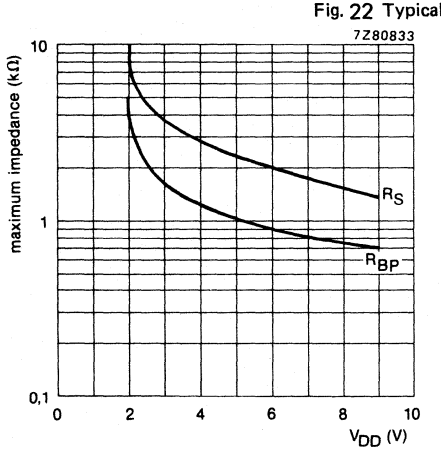


(c) V_{LCD} = 0 V; external clock; T_{amb} = −40 to + 85 °C.

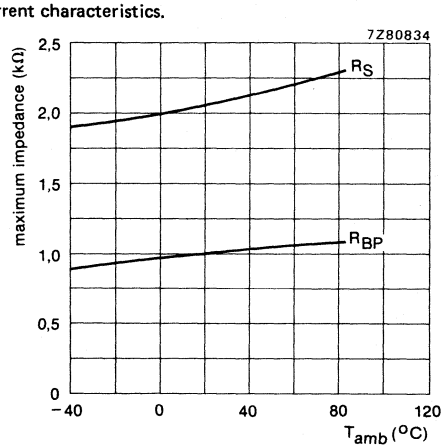


(d) V_{LCD} = 0 V; external clock; f_{CLK} = nominal frequency.

Fig. 22 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig. 23 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

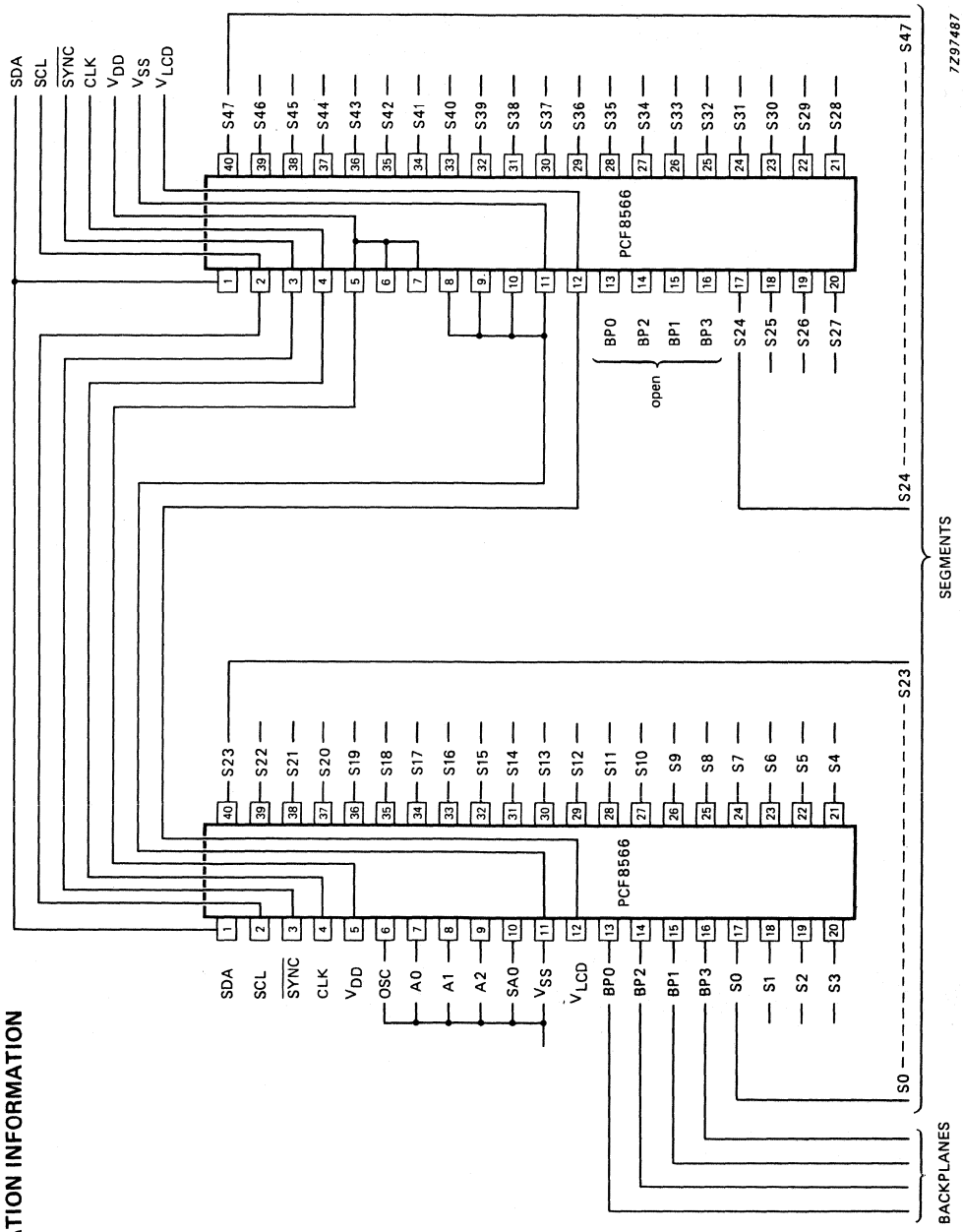


Fig. 24 Single plane wiring of packaged PCF8566s.

128 x 8 BIT/256 x 8 BIT STATIC RAMs WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

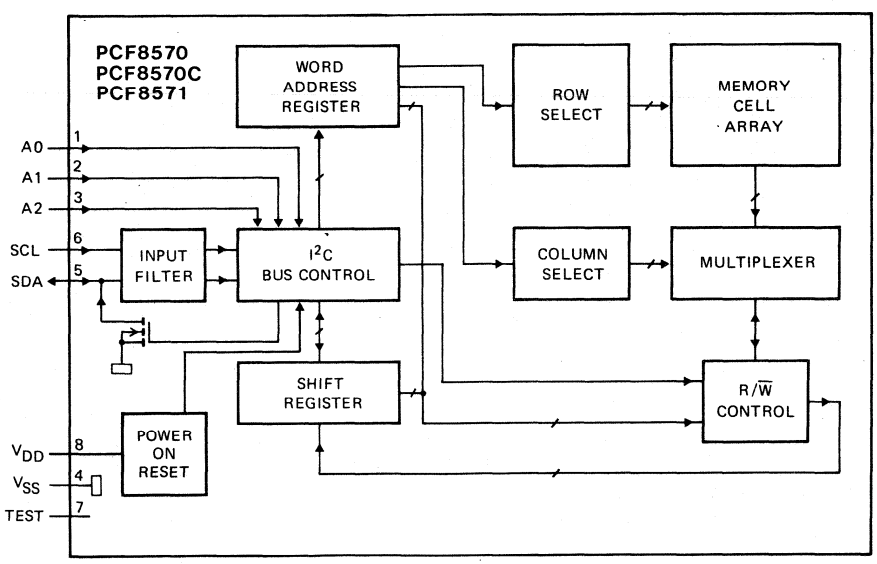


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT-97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line } I^2C bus
6	SCL	serial clock line } I^2C bus
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

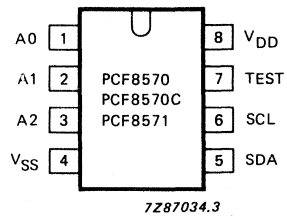


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}	−0,8 to + 8,0	V
Voltage range on any input	V_I	−0,8 to V_{DD} + 0,8	V
DC input current (any input)	$\pm I_I$	max. 10	mA
DC output current (any output)	$\pm I_O$	max. 10	mA
Supply current (pin 8 or pin 4)	$\pm I_{DD}$; I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 300	mW
Power dissipation per output	P	max. 50	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at $V_I = V_{SS}$ or V_{DD};					
operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level*	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Fig. 12 and 13)					
Supply current at T_{amb} = 25 °C; TEST = V_{DD};					
PCF8570/8570C	I_{DDR}	–	50	400	nA
PCF8571	I_{DDR}	–	50	200	nA
Recovery time	t_{HD2}	–	50	–	μs

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

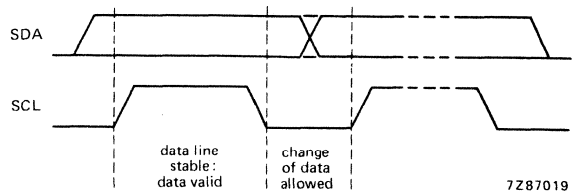


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

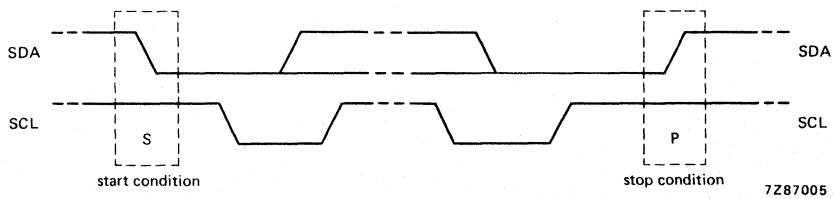


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

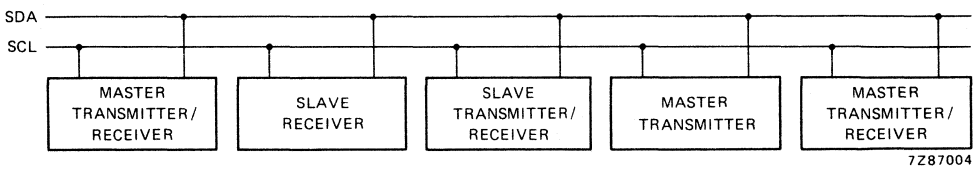


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

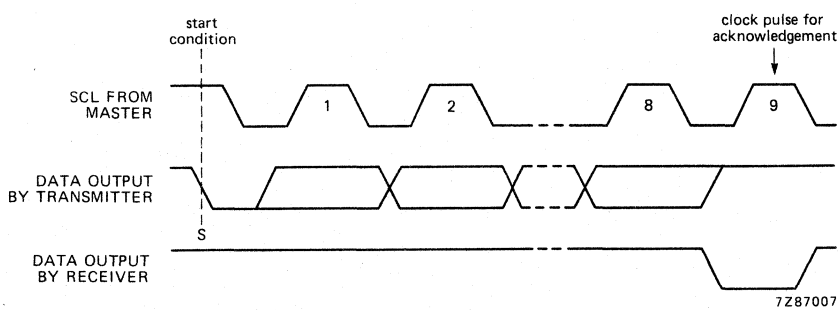


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_r	–	–	1,0	μs
SCL and SDA fall time	t_f	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

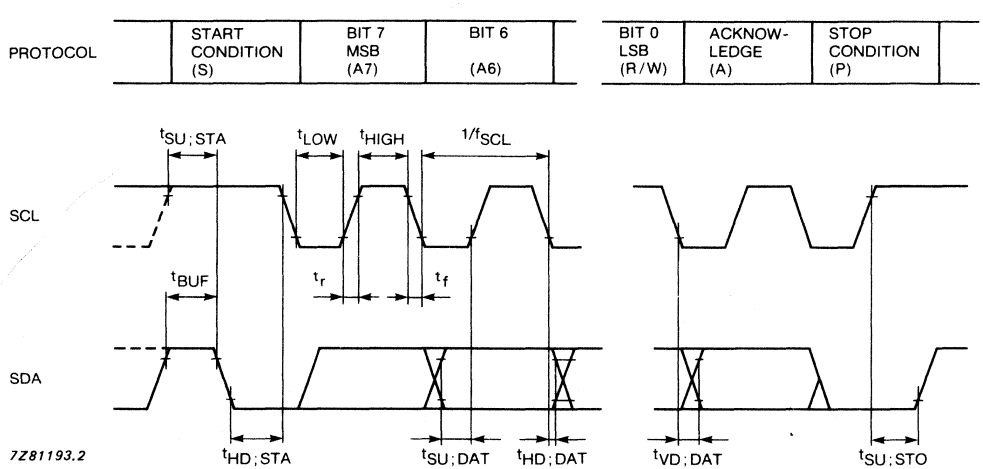


Fig. 7 I^2C bus timing diagram.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570/PCF8570C/PCF8571 READ and WRITE cycles is shown in Fig. 8.

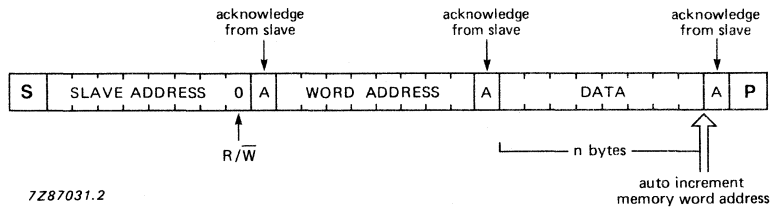


Fig. 8(a) Master transmits to slave receiver (WRITE mode).

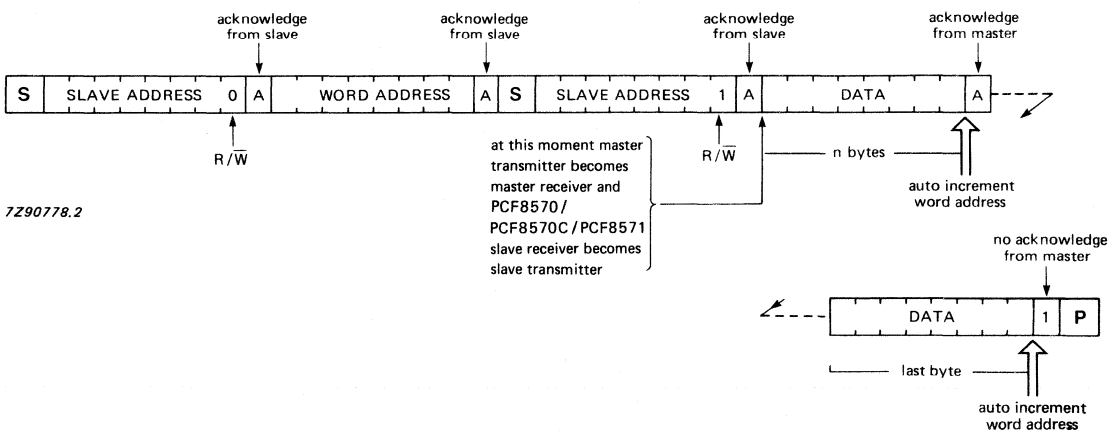


Fig. 8(b) Master reads after setting word address (WRITE word address; READ data).

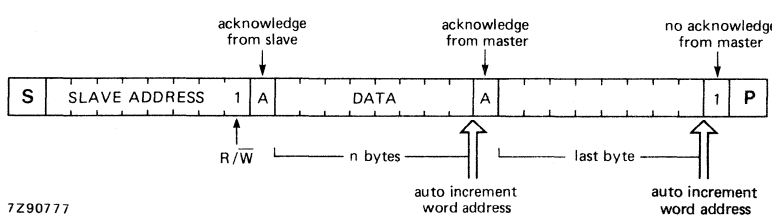


Fig. 8(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570/PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 9). The PCF8570C has slave address 1011 as group 1, while group 2 is fully programmable (see Fig. 10).

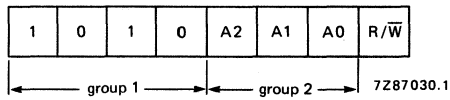


Fig. 9 PCF8570 and PCF8571 address.

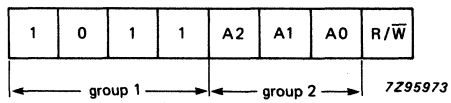


Fig. 10 PCF8570C address.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.

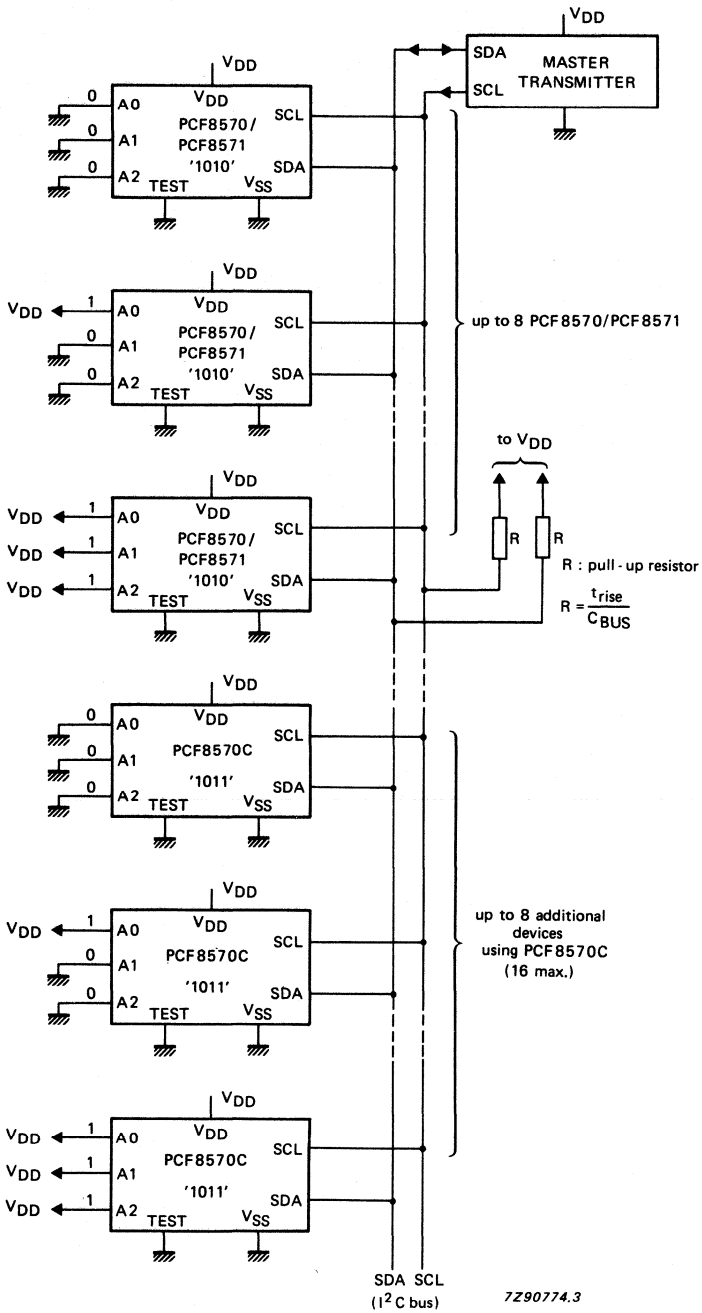
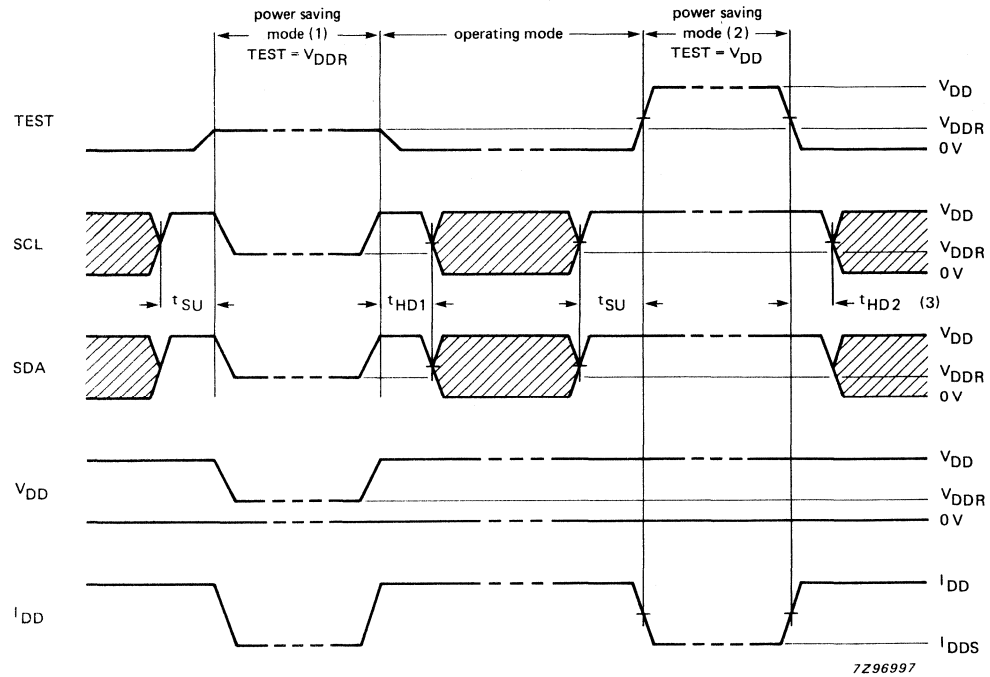


Fig. 11 Application diagram.

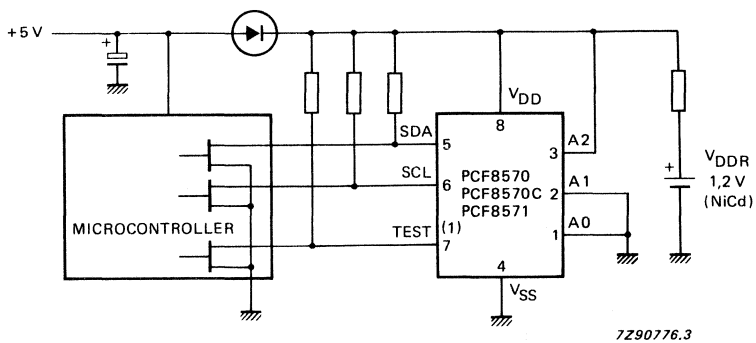
POWER SAVING MODE

With the condition **TEST** = V_{DD} or V_{DDR} the PCF8570/PCF8570C/PCF8571 goes into the power saving mode and I^2C bus logic is reset.



(1) Power saving mode without 5 V supply voltage.
(2) Power saving mode with 5 V supply voltage.
(3) t_{SU} and $t_{HD1} \geqslant 4\ \mu s$ and $t_{HD2} \geqslant 50\ \mu s$.

Fig. 12 Timing for power saving mode.



(1) In the operating mode TEST = 0; In the power saving mode TEST = V_{DDR}.

Fig. 13 Application example for power saving mode.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS peripheral circuit that functions as a real time clock/calendar with an Inter IC (I^2C) bus interface.
The device incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA are also available. Information is transferred via a serial, two-line bidirectional bus (I^2C). Back-up for the clock during supply interruption is provided by a 1.2 V nickel cadmium battery. The time base is generated from a 32,768 kHz crystal controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (clock)		$V_{DD}-V_{SS1}$	1,1	–	6,0	V
Supply voltage (I^2C interface)		$V_{DD}-V_{SS2}$	2,5	–	6,0	V
Crystal oscillator		f_{osc}	–	32,768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT-38).
PCF8573T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

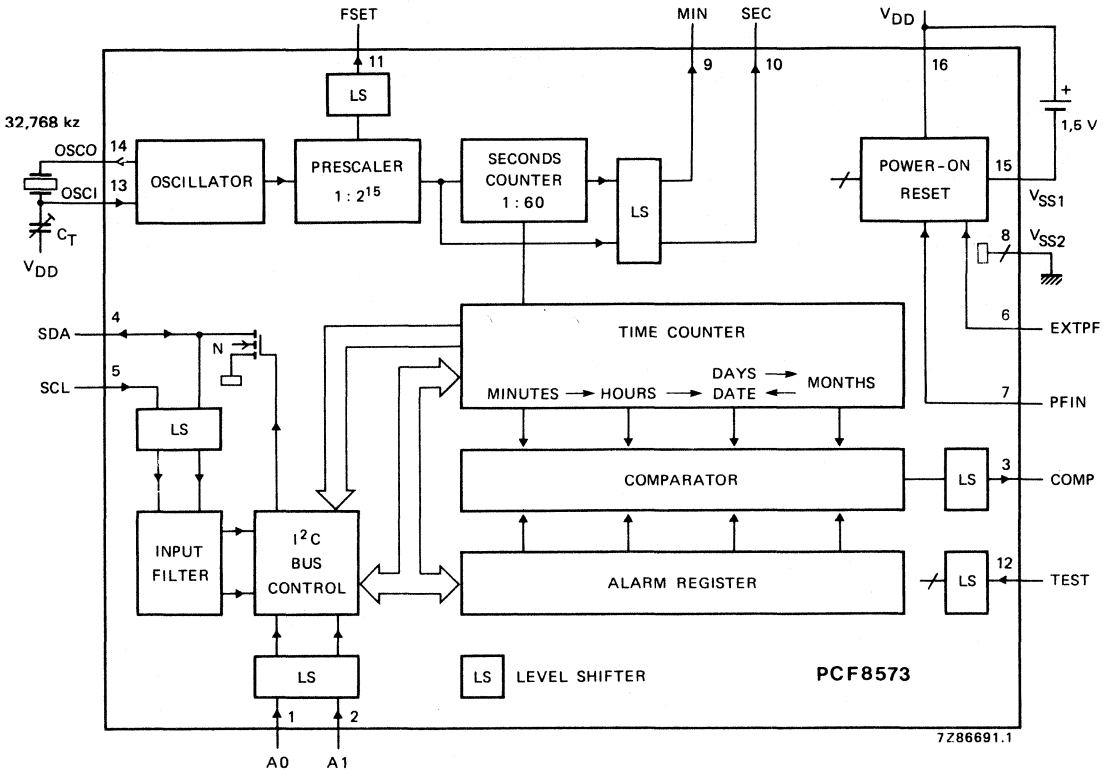


Fig. 1 Block diagram.

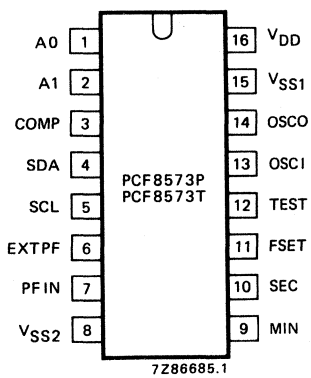


Fig. 2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C bus
5	SCL	serial clock line	I^2C bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

1. Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

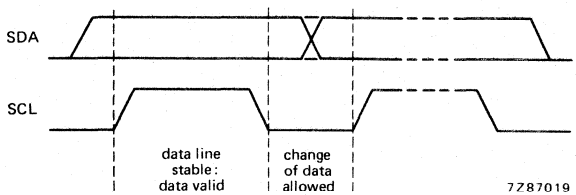


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

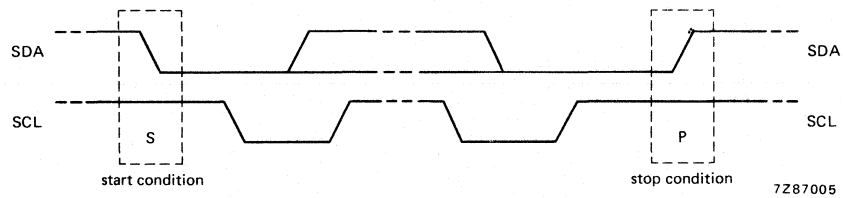


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

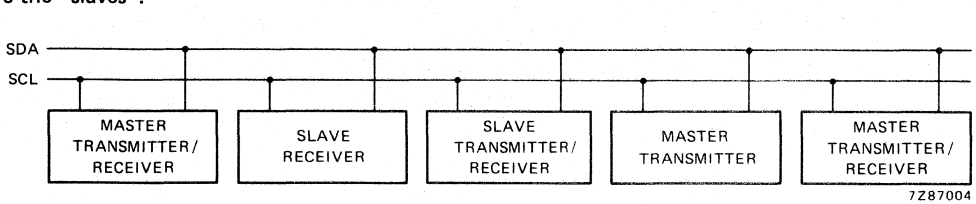


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 11 and Fig. 12.)

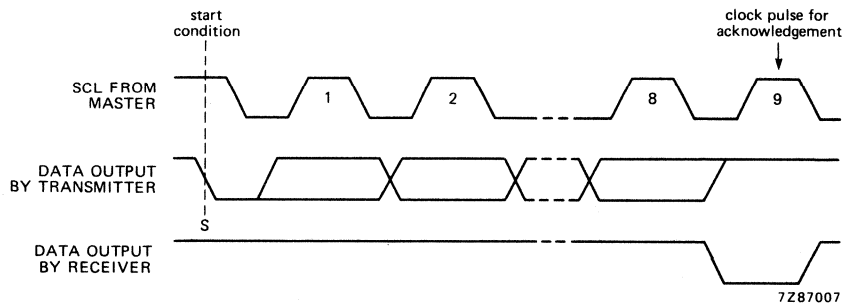


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

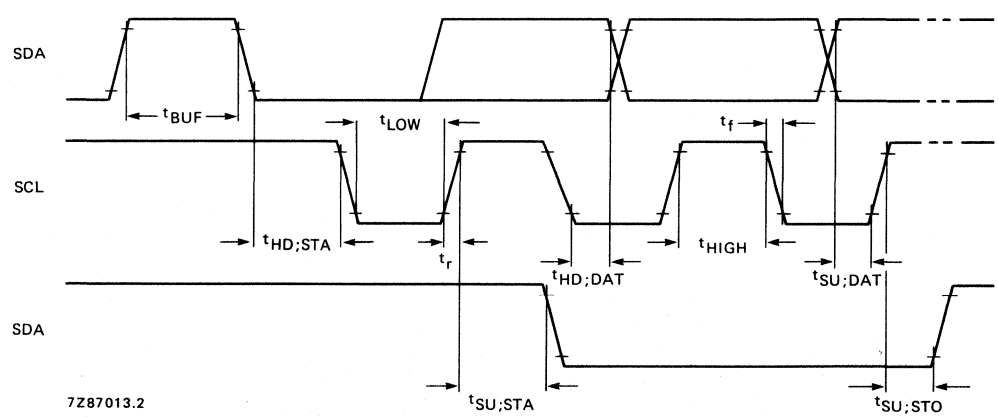


Fig. 7 Timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

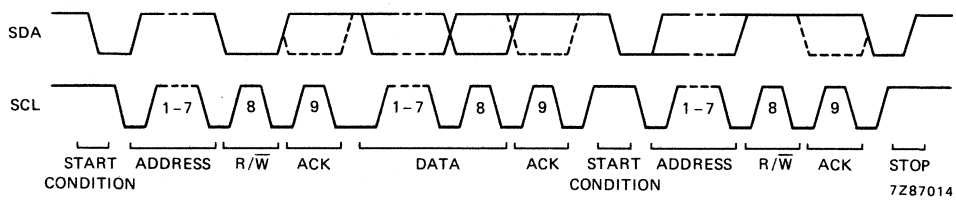


Fig. 8 Complete data transfer.

Where:

Clock t_{LOWmin} 4,7 μs

$t_{HIGHmin}$ 4 μs

The dashed line is the acknowledgement of the receiver

Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 9.

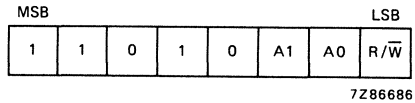


Fig. 9 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 10 and Fig. 11.

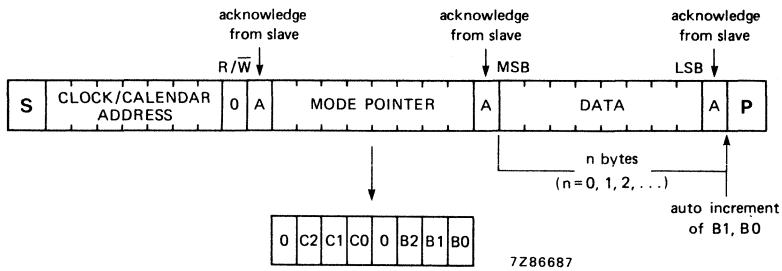


Fig. 10 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nible is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

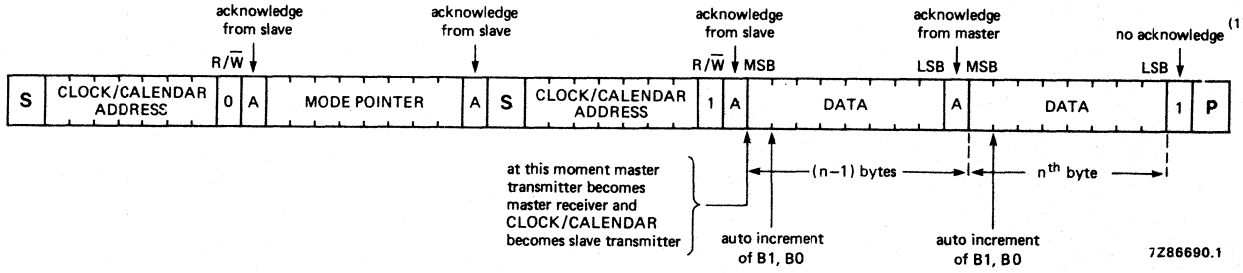
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

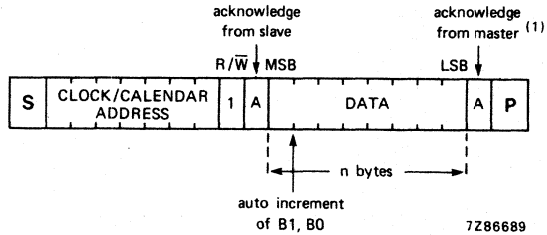
"X" is the don't care bit
"D" is the data bit
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 11 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 12 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where:

"D" is the data bit.

* = minutes.

** = seconds.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage ranges		$V_{DD}-V_{SS1}$	−0,3	8	V
		$V_{DD}-V_{SS2}$	−0,3	8	V
Voltage input (pins 4; 5)		V_I	$V_{SS2}-0,8$	$V_{DD}+0,8$	V*
Voltage input (pins 6; 7; 13, 14)		V_I	$V_{SS1}-0,6$	$V_{DD}+0,6$	V
Voltage on any other pin		V_I	$V_{SS2}-0,6$	$V_{DD}+0,6$	V
Input current		I_I	–	10	mA
Output current		I_O	–	10	mA
Power dissipation per output		P_O	–	100	mW
Total power dissipation		P_{tot}	–	200	mW
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

* Impedance min. 500 Ω.

CHARACTERISTICS

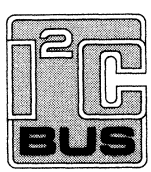
V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = + 25 °C.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage I^2C interface		$V_{DD}-V_{SS2}$	2,5	5,0	6,0	V
Supply voltage (clock)		$V_{DD}-V_{SS1}$	1,1	1,5	$V_{DD}-V_{SS2}$	V
Supply current V_{SS1}	$V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	3	10	μA
	$V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
Supply current V_{SS2}	$V_{DD}-V_{SS2}$ = 5 V; (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA
Inputs SCL, SDA, A0, A1, TEST						
Input voltage HIGH		V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0,3 x V_{DD}	V
Input leakage current	$V_I = V_{SS2}$ to V_{DD}	$\pm I_I$	–	–	1	μA
Inputs EXTPF, PFIN						
Input voltage HIGH		$V_{IH}-V_{SS1}$	0,7 x $V_{DD}-V_{SS1}$	–	–	V
Input voltage LOW		$V_{IL}-V_{SS1}$	0	–	0,3 x $V_{DD}-V_{SS1}$	V
Input leakage current	$V_I = V_{SS1}$ to V_{DD}	$\pm I_I$	–	–	1,0	μA
	T_{amb} = 25 °C; $V_I = V_{SS1}$ to V_{DD}	$\pm I_I$	–	–	0,1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage HIGH	$V_{DD}-V_{SS2}$ = 2,5 V; $-I_O$ = 0,1 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0,5 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output voltage LOW	$V_{DD}-V_{SS2}$ = 2,5 V; I_O = 0,3 mA	V_{OL}	–	–	0,4	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1,6 mA	V_{OL}	–	–	0,4	V
Output SDA (n channel open drain)						
Output "ON"	I_O = 3 mA; $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current)	$V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	I_O	–	–	1	μA
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1,2	1,4	V
Power "ON" reset	$V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	–	–	1	μs
Input PFIN		t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	–	–	1	μs
fall time		t_f	–	–	0,3	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency at SCL	$V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (Fig. 7)		t_{LOW}	4,7	–	–	μs
Pulse width HIGH (Fig. 7)		t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA input		T_I	0,25	1	2,5	μs
Input capacitance (SDA; SCL)		C_I	–	–	7	pF
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters	f = 32,768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	9	–	pF
Trimmer capacitance		C_T	5	–	25	pF



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

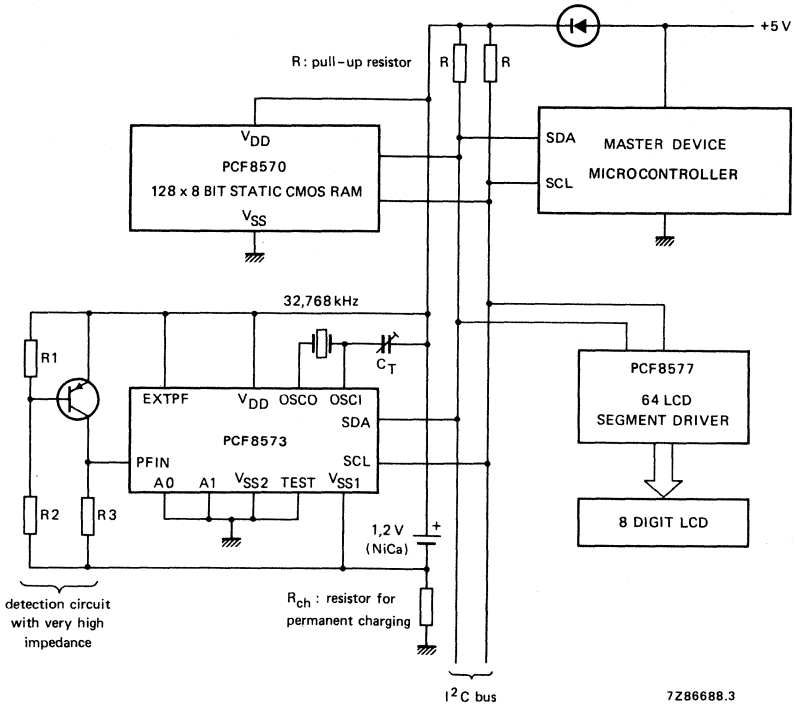


Fig. 13 Application example of the PCF8573 clock/calendar.

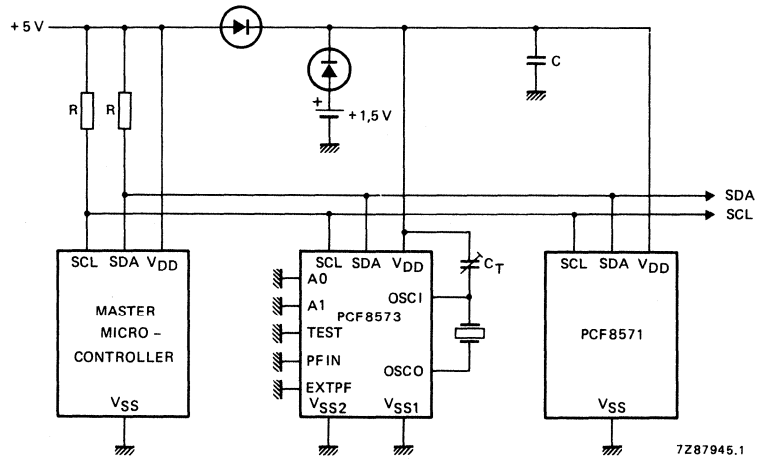


Fig. 14 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

REMOTE 8-BIT I/O EXPANDER FOR I²C BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I²C).
It can also interface microcomputers without a serial interface to the I²C bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig. 10.

Features

- Operating supply voltage 2,5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

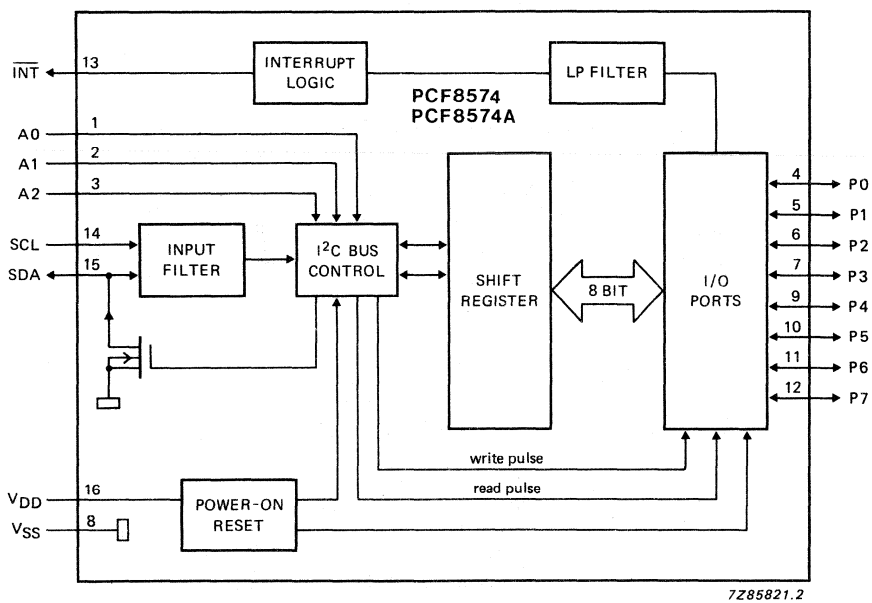


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT-38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

PINNING

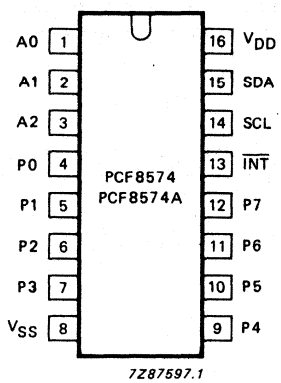


Fig. 2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

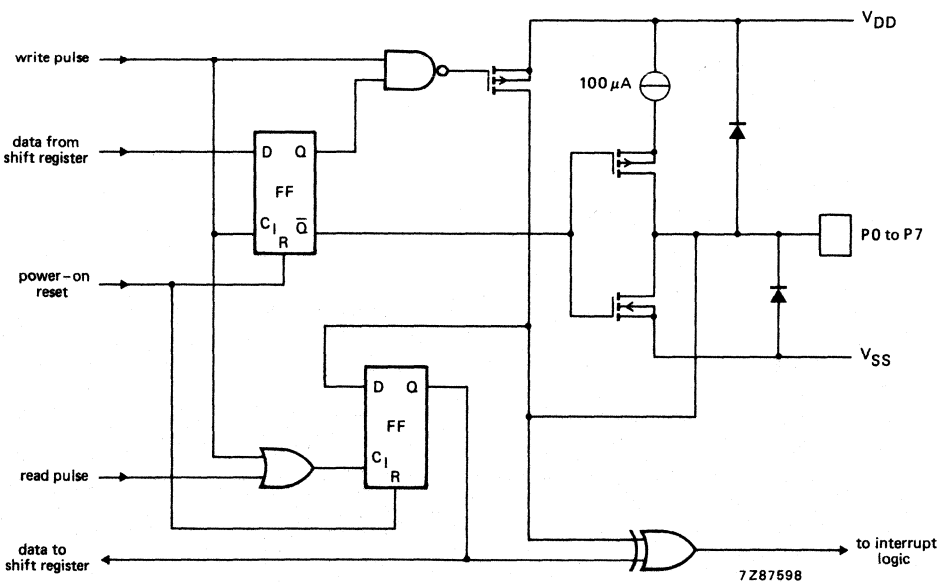


Fig. 3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

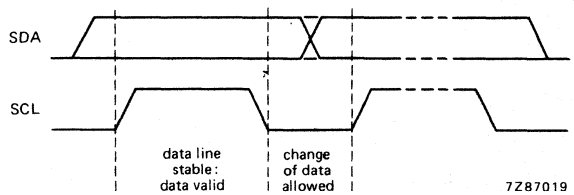


Fig. 4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

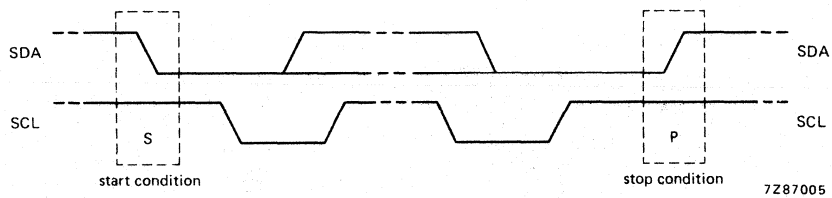


Fig. 5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

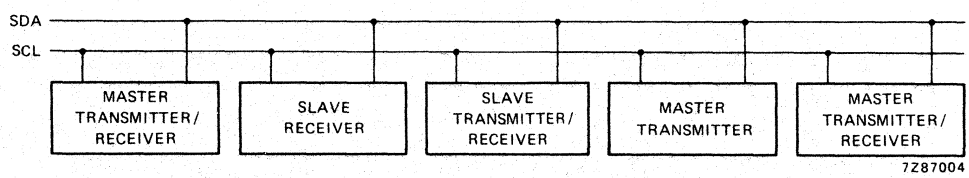


Fig. 6 System configuration.

CHARACTERISTICS OF THE I²C BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

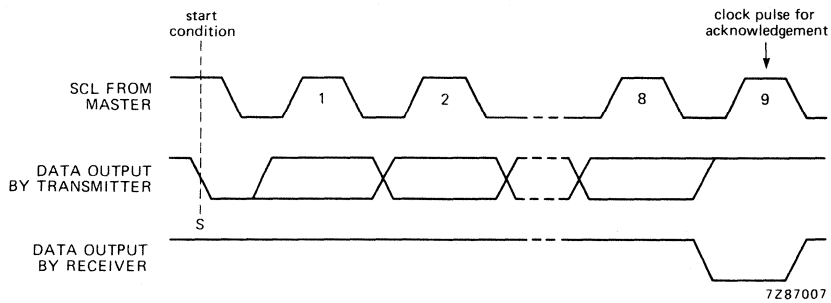


Fig. 7 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 8.

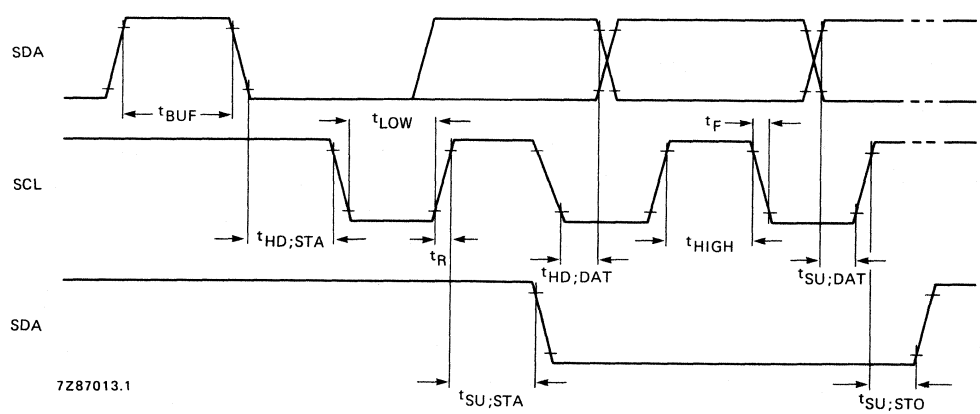


Fig. 8 I²C bus timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

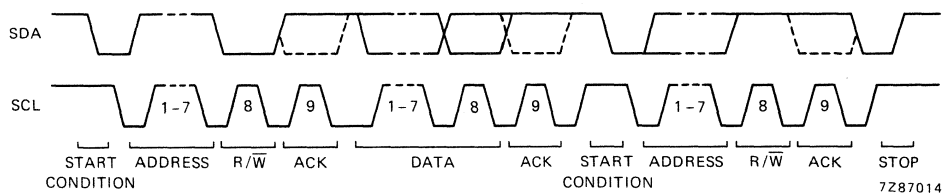


Fig. 9 Complete data transfer.

Where:

Clock t_{LOWmin} 4,7 μs

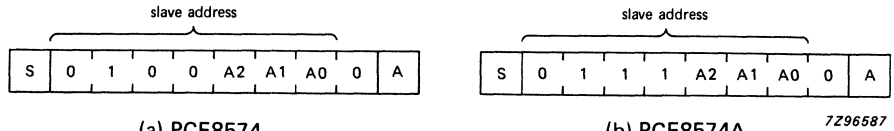
$t_{HIGHmin}$ 4 μs

The dashed line is the acknowledgement of the receiver

Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

FUNCTIONAL DESCRIPTION

Addressing (see Figs 10, 11 and 12)



(a) PCF8574. (b) PCF8574A.

Fig. 10 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

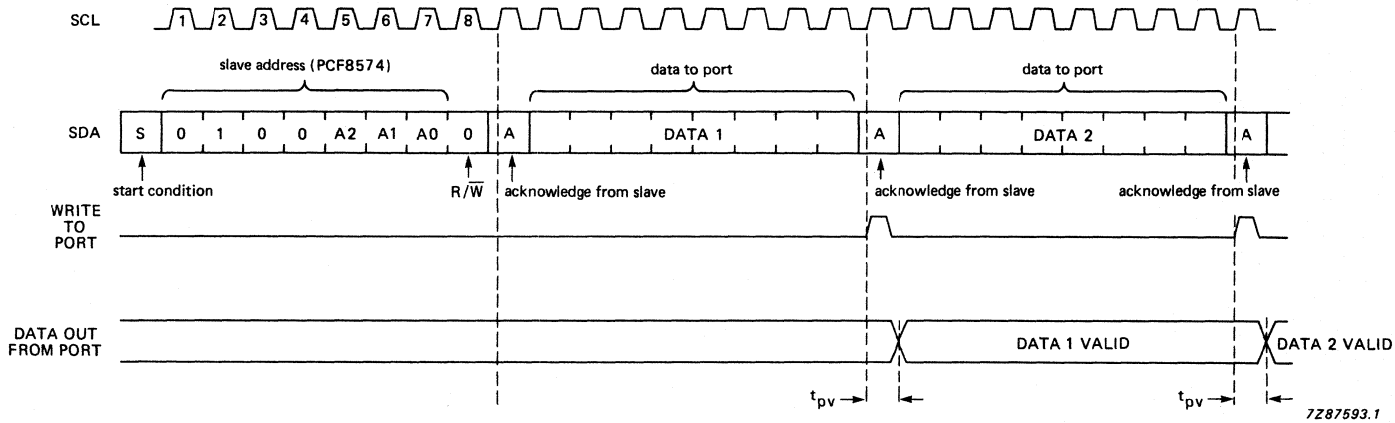


Fig. 11 WRITE mode (output port).

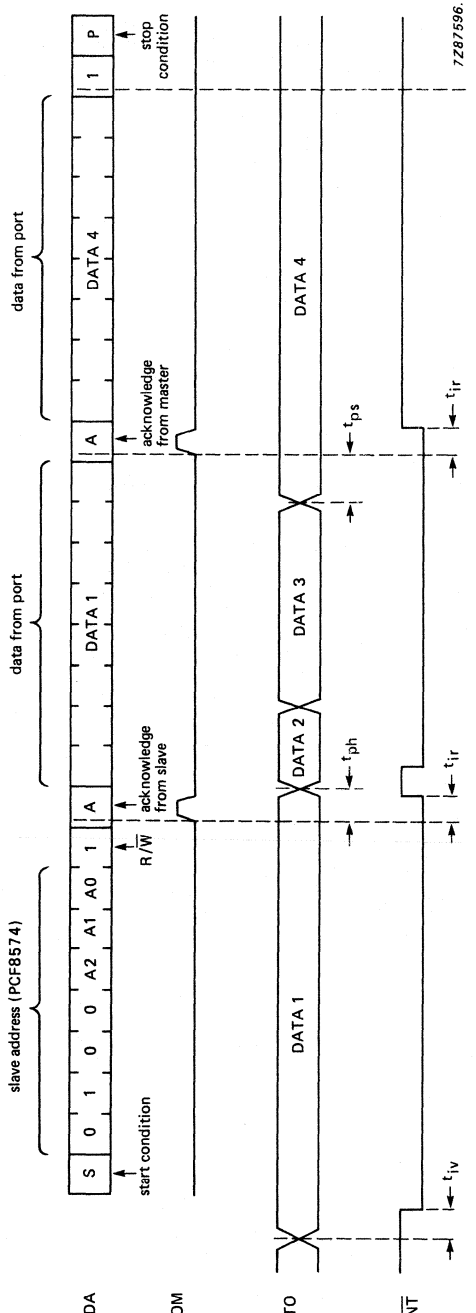


Fig. 12 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 13 and 14)

The PCF8574/PCF8574A provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

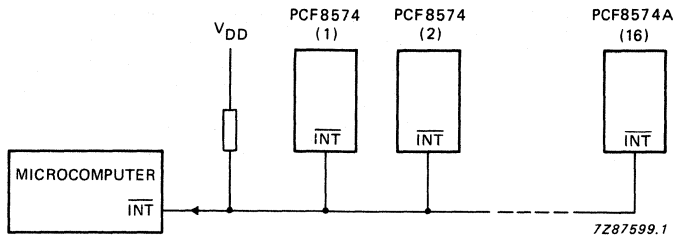


Fig. 13 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH to LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

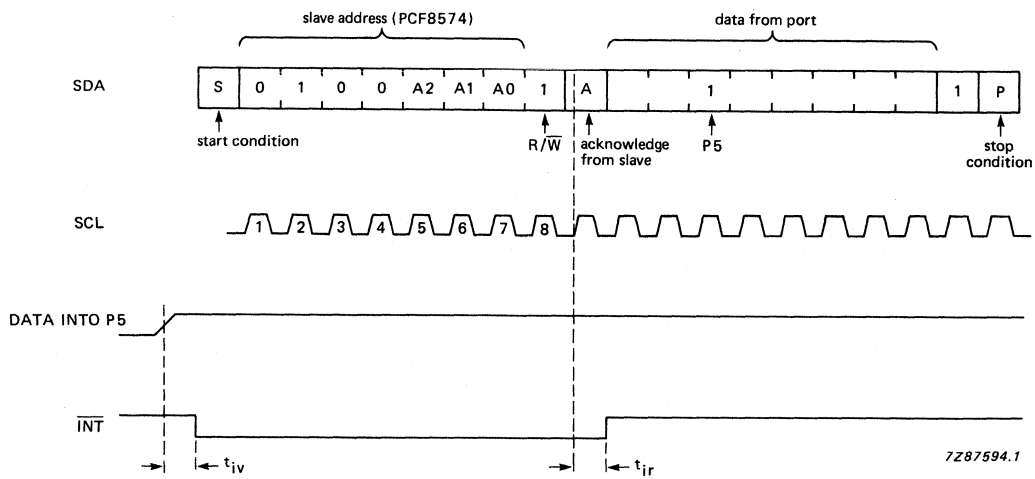


Fig. 14 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig. 15)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW to HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

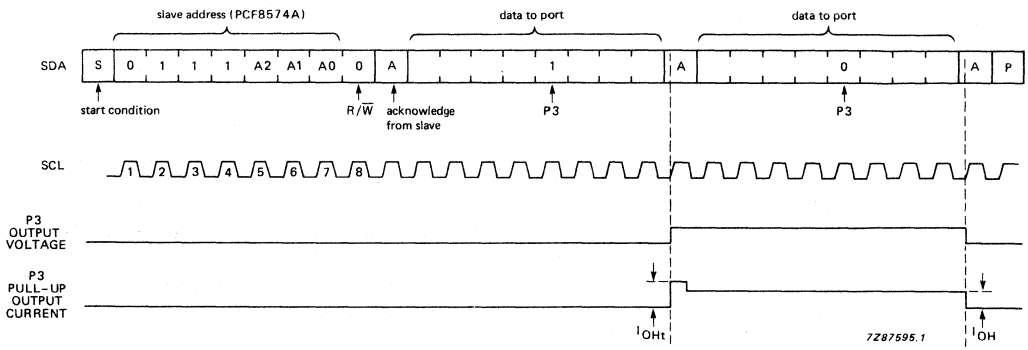


Fig. 15 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 7	V
Input voltage range (any pin)	V_I		V_{SS}−0,5 to V_{DD} + 0,5	V
D.C. current into any input	$\pm I_I$	max.	20	mA
D.C. current into any output	$\pm I_O$	max.	25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; I_{SS}	max.	100	mA
Total power dissipation	P_{tot}	max.	400	mW
Power dissipation per output	P_o	max.	100	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−40 to + 85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
at V_{DD} = 6 V; no load, inputs at V_{DD}, V_{SS}					
operating; (SCL = 100 kHz)	I_{DD}	–	40	100	μA
standby	I_{DDO}	–	1,5	10	μA
Power-on reset voltage level (note 1)	V_{REF}	–	1,3	2,4	V
Input SCL; input/output SDA (pins 14; 15)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Output current LOW					
at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Input/Output leakage current	$\|I_L\|$	–	–	100	nA
Clock frequency (see Fig. 8)	f_{SCL}	–	–	100	kHz
Tolerable spike width					
at SCL and SDA input	t_s	–	–	100	ns
Input capacitance (SCL, SDA)					
at V_I = V_{SS}	C_I	–	–	7	pF
I/O ports (pins 4 to 7; 9 to 12)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Maximum allowed input current					
through protection diode					
at $V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW					
at V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	30	–	mA
Output current HIGH					
at V_{OH} = V_{SS} (current source only)	$-I_{OH}$	30	100	300	μA
Transient pull-up current HIGH					
during acknowledge (see Fig. 16)					
at V_{OH} = V_{SS}	$-I_{OHt}$	–	0,5	–	mA
Input/Output capacitance	$C_{I/O}$	–	–	10	pF
Port timing; $C_L \leqslant 100$ pF (see Figs 12 and 13)					
Output data valid	t_{pv}	–	–	4	μs
Input data set-up	t_{ps}	0	–	–	μs
Input data hold	t_{ph}	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$ (pin 13)					
Output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA
Output current HIGH at $V_{OH} = V_{DD}$	$\|I_{OH}\|$	–	–	100	nA
$\overline{INT}$ timing; $C_L \leqslant 100$ pF (see Fig. 13)					
Input data valid	t_{iv}	–	–	4	μs
Reset delay	t_{ir}	–	–	4	μs
Select inputs A0, A1, A2 (pins 1 to 3)					
Input voltage LOW	V_{IH}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	100	nA

Note 1

The power-on reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24 segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO-56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8576U: uncased chip in tray
PCF8576U/10: chip-on-film frame carrier (FFC)

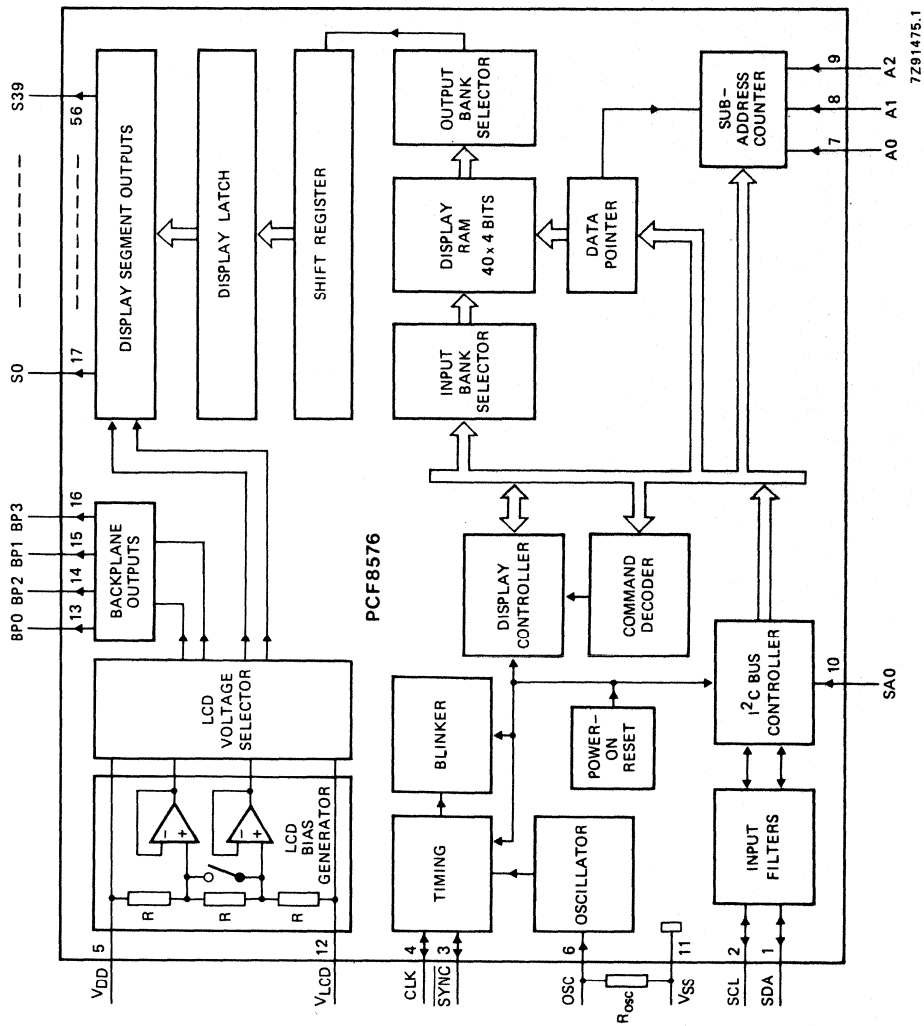


Fig. 1 Block diagram.

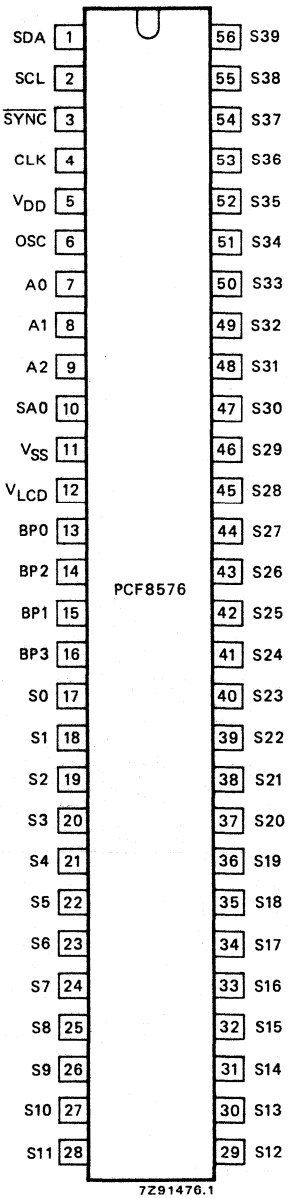


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 56	S0 to S39	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the 2-line I^2C bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropiate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

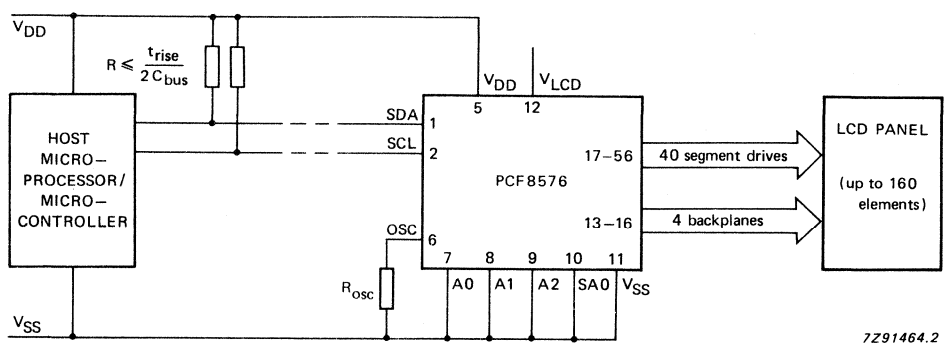


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\,V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\,V_{off(rms)} = 2{,}449\,V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\;V_{off(rms)} = 2{,}309\,V_{off(rms)}$

These compare with $V_{op} = 3\,V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

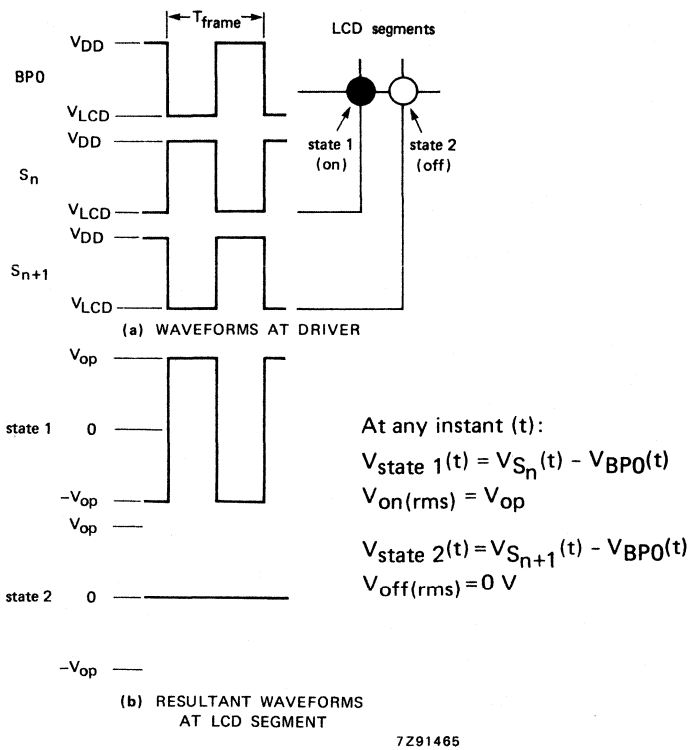


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

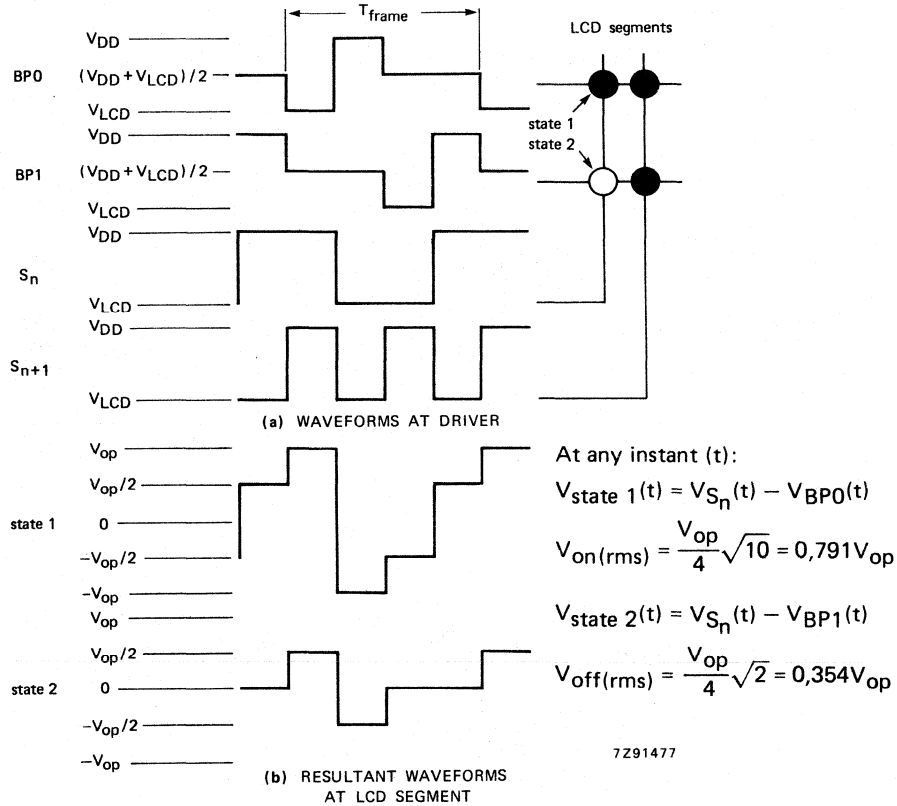


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

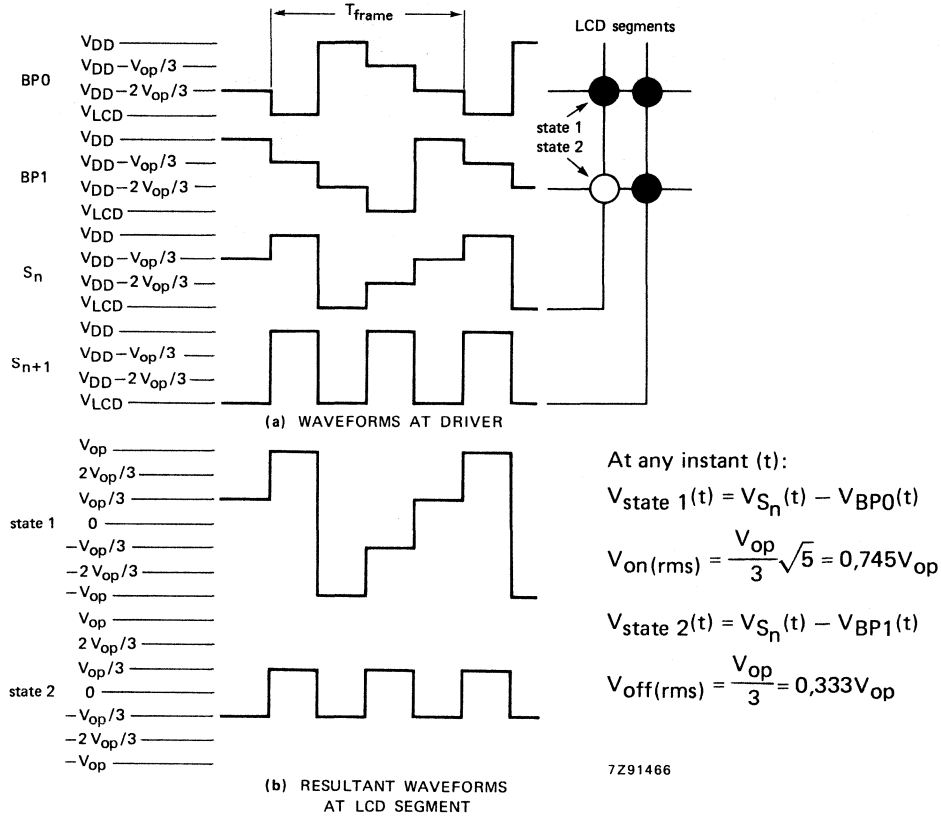


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive waveform for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

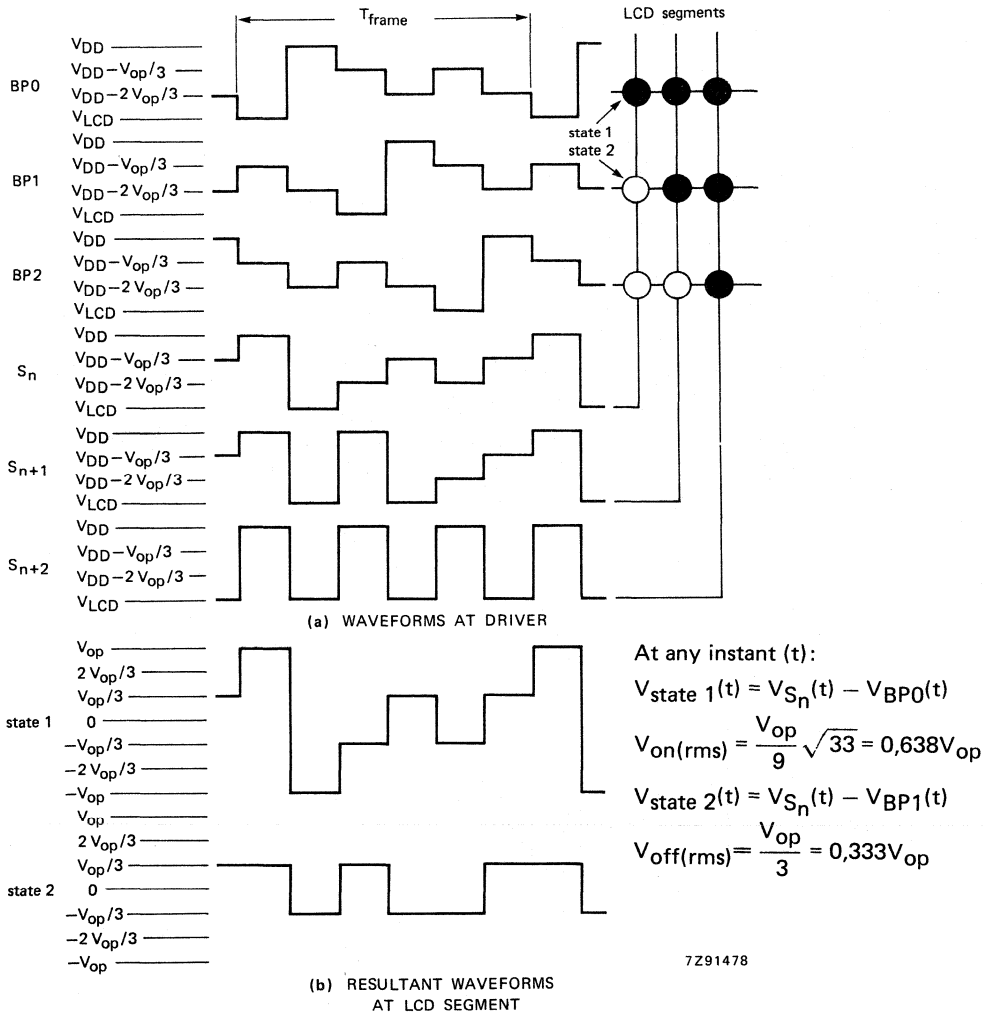


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

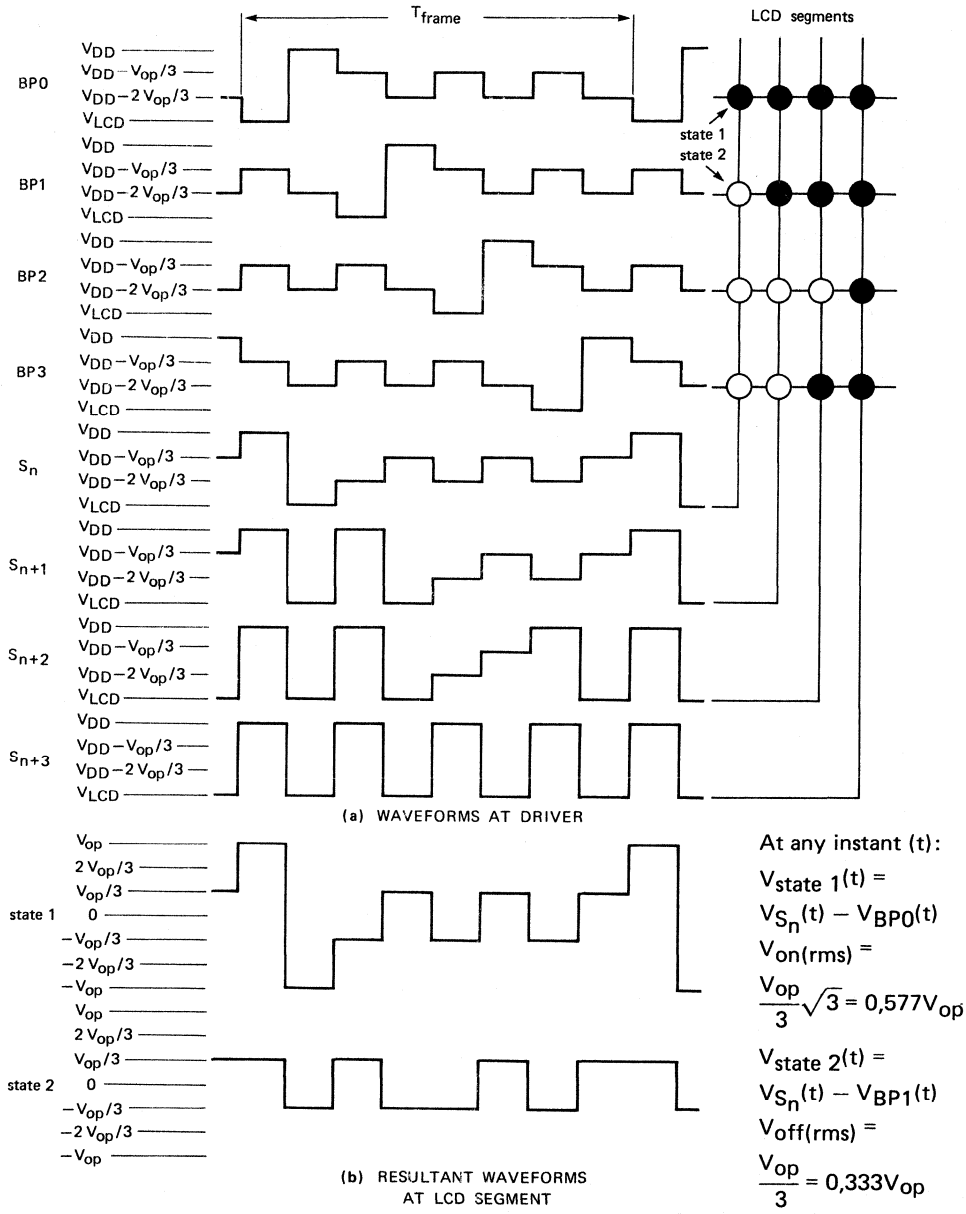


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig. 9. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

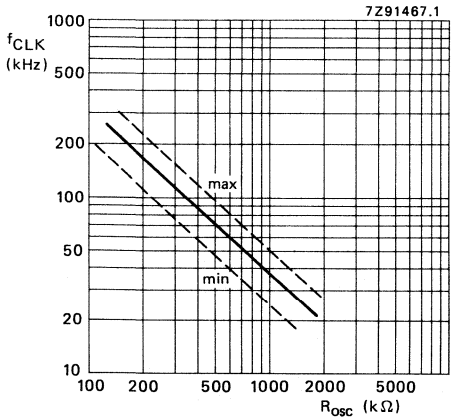


Fig. 9 Oscillator frequency as a function of R_{osc}: $f_{CLK} \approx (3{,}4 \times 10^7 / R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C bus. To allow I²C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	180	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{osc} = 180 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{osc} will be 1,2 MΩ. The reduced clock frequency and the increased value of R_{osc} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig. 10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

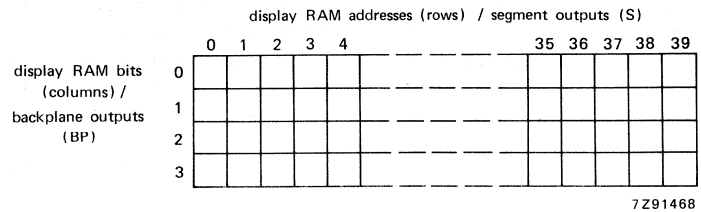


Fig. 10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

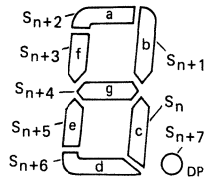
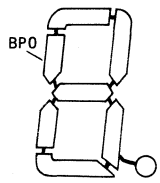
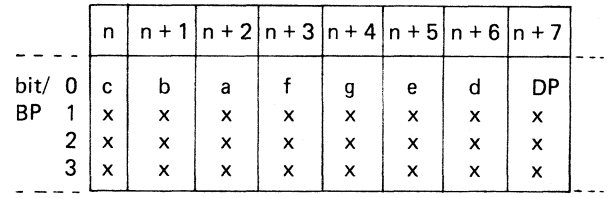
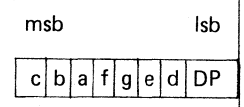
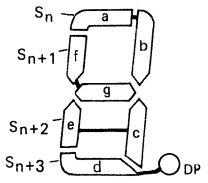
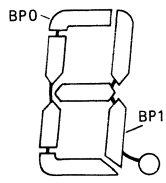
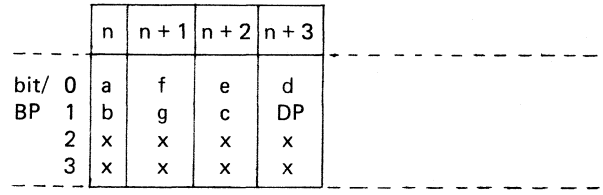
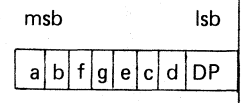
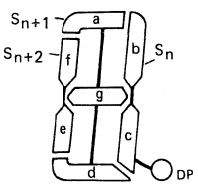
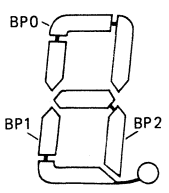
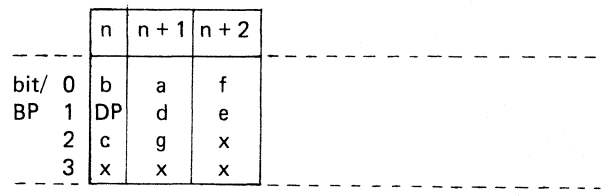
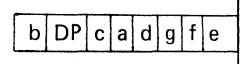
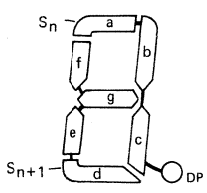
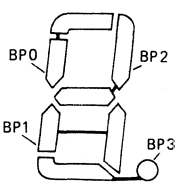
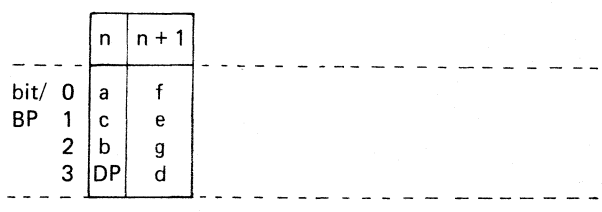
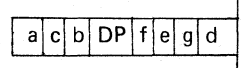
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

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Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

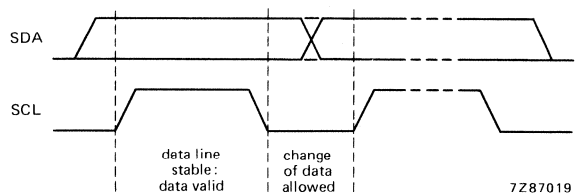


Fig. 12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

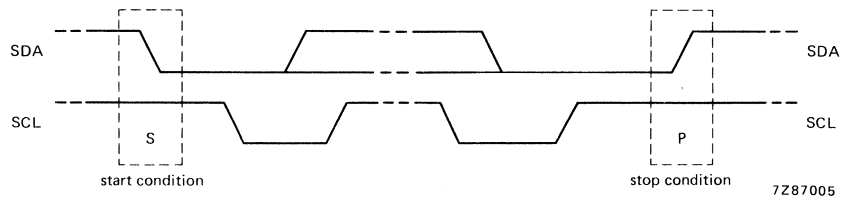


Fig. 13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

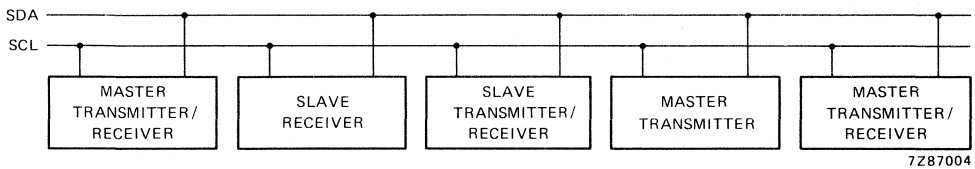


Fig. 14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

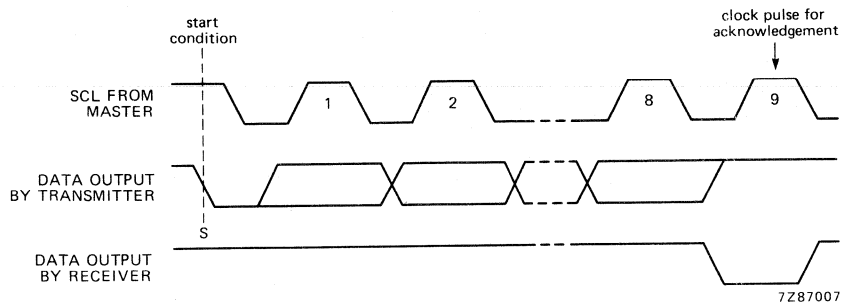


Fig. 15 Acknowledgement on the I^2C bus.

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8576 I²C bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8576s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 16. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C bus master issues a stop condition (P).

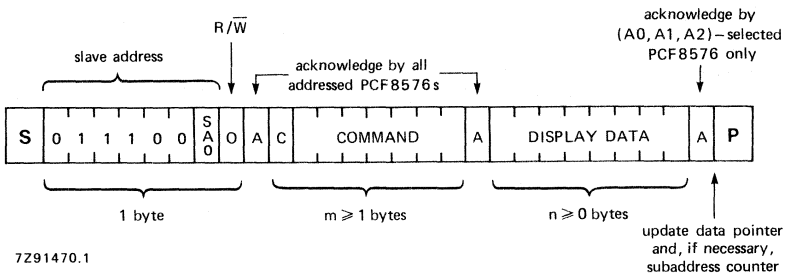


Fig. 16 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

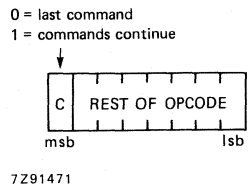


Fig. 17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>MODE SET

C | 1 | 0 | LP | E | B | M1 | M0</td><td>LCD drive mode | bits M1 M0
static (1 BP) | 0 1
1 : 2 MUX (2 BP) | 1 0
1 : 3 MUX (3 BP) | 1 1
1 : 4 MUX (4 BP) | 0 0

LCD bias | bit B
1/3 bias | 0
1/2 bias | 1

display status | bit E
disabled (blank) | 0
enabled | 1

mode | bit LP
normal mode | 0
power-saving mode | 1</td><td>Defines LCD drive mode

Defines LCD bias configuration

Defines display status
The possibility to disable the display allows implementation of blinking under external control

Defines power dissipation mode</td></tr>
<tr><td>LOAD DATA POINTER

C | 0 | P5 P4 P3 P2 P1 P0</td><td>bits P5 P4 P3 P2 P1 P0
6-bit binary value of 0 to 39</td><td>Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses</td></tr>
<tr><td>DEVICE SELECT

C | 1 1 0 0 | A2 A1 A0</td><td>bits A0 A1 A2
3-bit binary value of 0 to 7</td><td>Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses</td></tr>
</table>

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>I</td><td>O</td></tr></table></td><td><table><tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table><table><tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table></td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>0</td><td>A</td><td>BF1</td><td>BF0</td></tr></table></td><td><table><tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr><tr><td>off
2 Hz
1 Hz
0,5 Hz</td><td>0
0
1
1</td><td>0
1
0
1</td></tr></table><table><tr><td>blink mode</td><td>bit A</td></tr><tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr></table></td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 18).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 19.

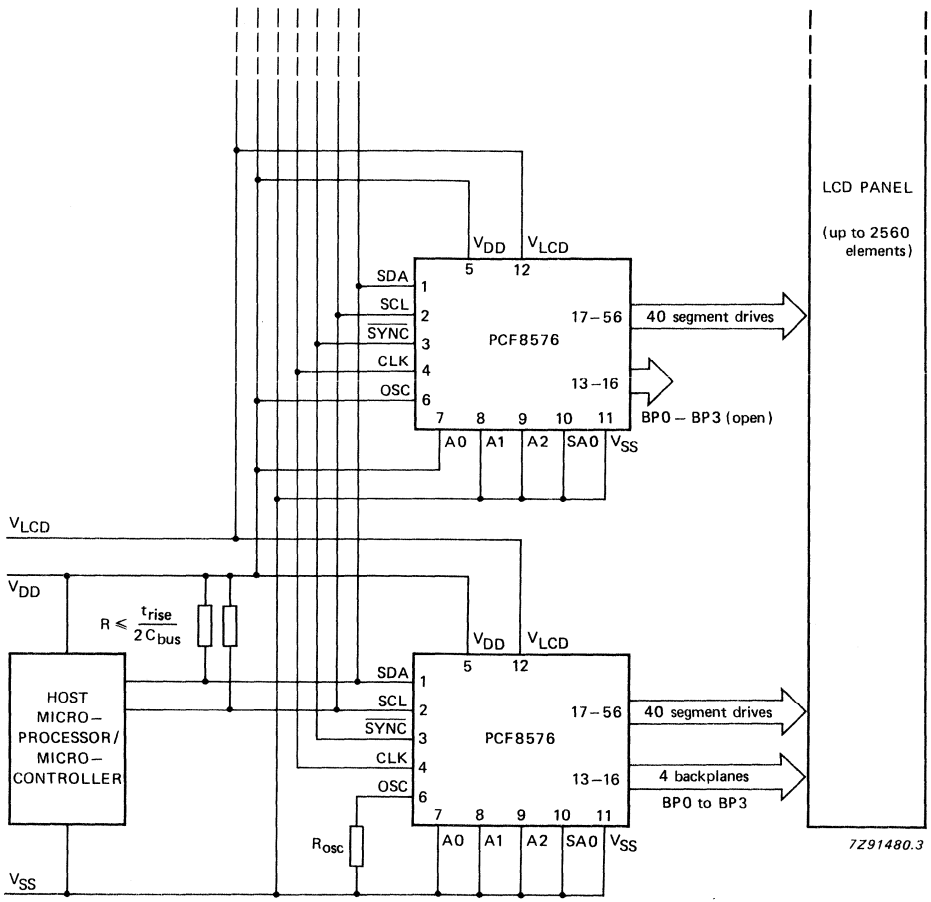
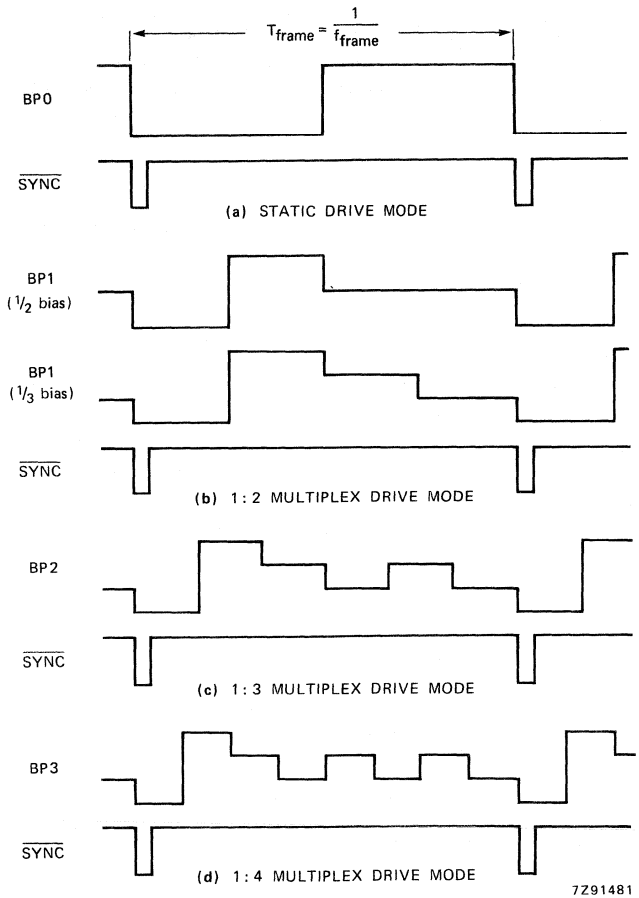


Fig. 18 Cascaded PCF8576 configuration.



Note

Excessive capacitive coupling between SCL or CLK and $\overline{SYNC}$ may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig. 19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see 'APPLICATION INFORMATION'.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 11 V
LCD supply voltage range	V_{LCD}		V_{DD}−11 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S39; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5 V
D.C. input current	$\pm I_I$	max.	20 mA
D.C. output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2 to 9 V; V_{LCD} = V_{DD}−2 to V_{DD}−9 V;

T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2	–	9	V
LCD supply voltage (note 1)	V_{LCD}	V_{DD}−9	–	V_{DD}−2	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 2)	I_{DD}	–	–	180	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz (note 2)	I_{LP}	–	–	60	μA
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD}−0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Leakage current (OSC) at $V_I = V_{DD}$	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	20	50	150	kΩ
Power-on reset level (note 3)	V_{REF}	–	1,0	1,6	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 4)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S39) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S39) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 6)

V_{SS} = 0 V; V_{DD} = 2 to 9 V; $V_{LCD} = V_{DD}-2$ to $V_{DD}-9$ V;
$T_{amb} = -40$ to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V; R_{osc} = 180 kΩ (note 7)	f_{CLK}	125	185	288	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V; R_{osc} = 1,2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at $V_{LCD} = V_{DD}-5$ V	t_{PLCD}	–	–	30	μs

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. $V_{LCD} \leqslant V_{DD}-3$ V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

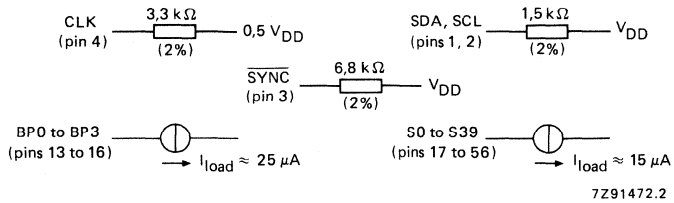


Fig. 20 Test loads.

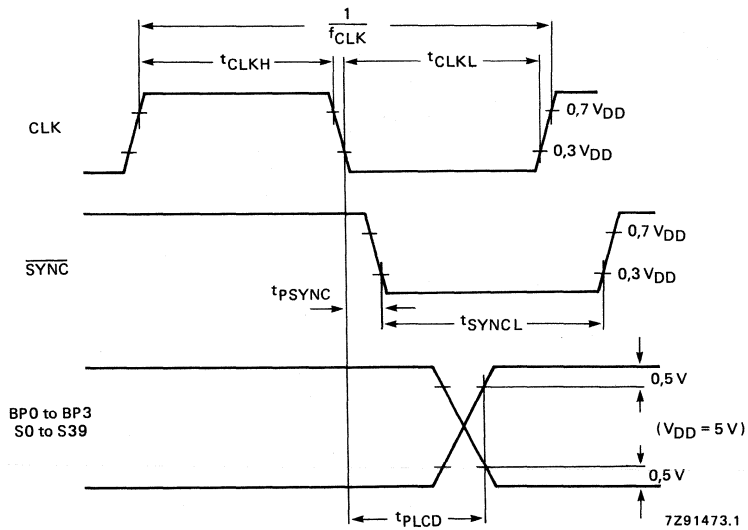


Fig. 21 Driver timing waveforms.

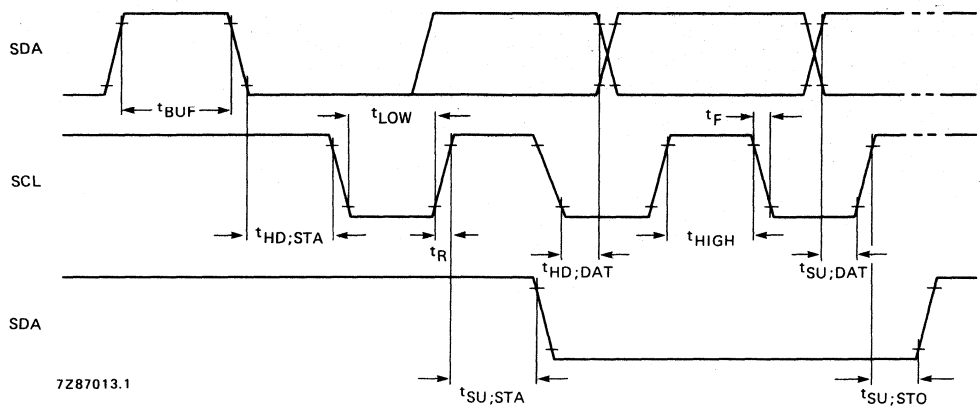
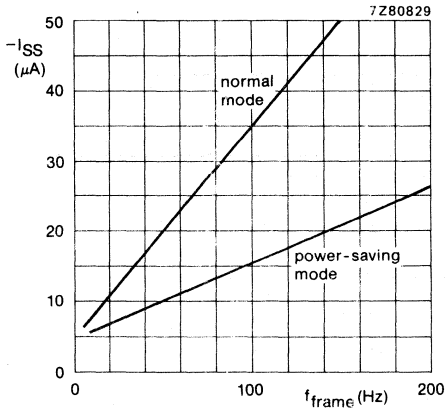
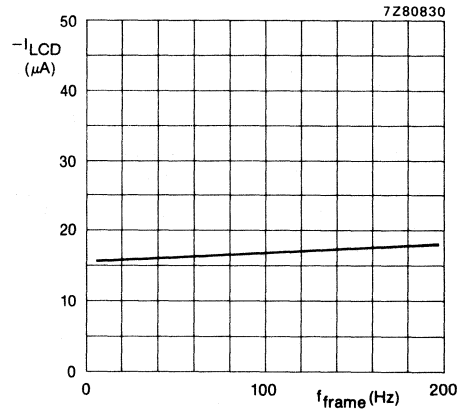


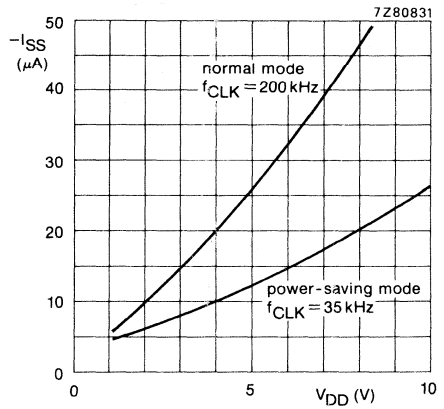
Fig. 22 I²C bus timing waveforms.



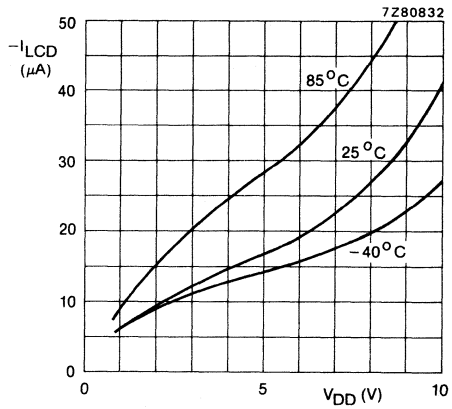
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

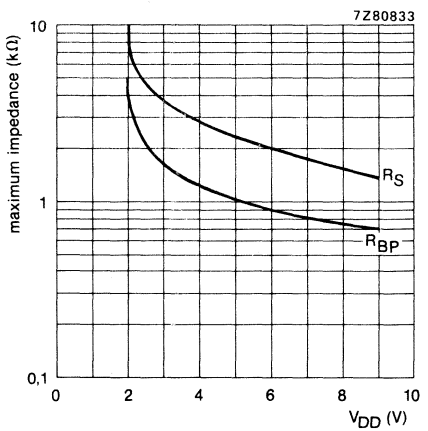


(c) V_{LCD} = 0 V; external clock; T_{amb} = −40 to + 85 °C.

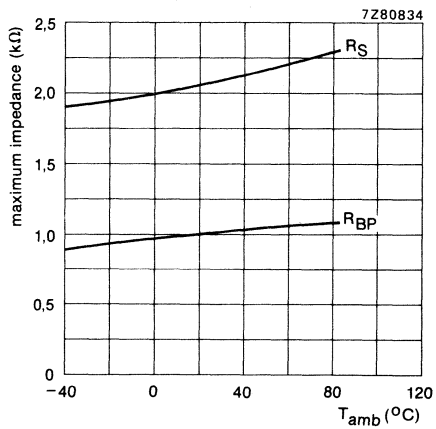


(d) V_{LCD} = 0 V; external clock; f_{CLK} = nominal frequency.

Fig. 23 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig. 24 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

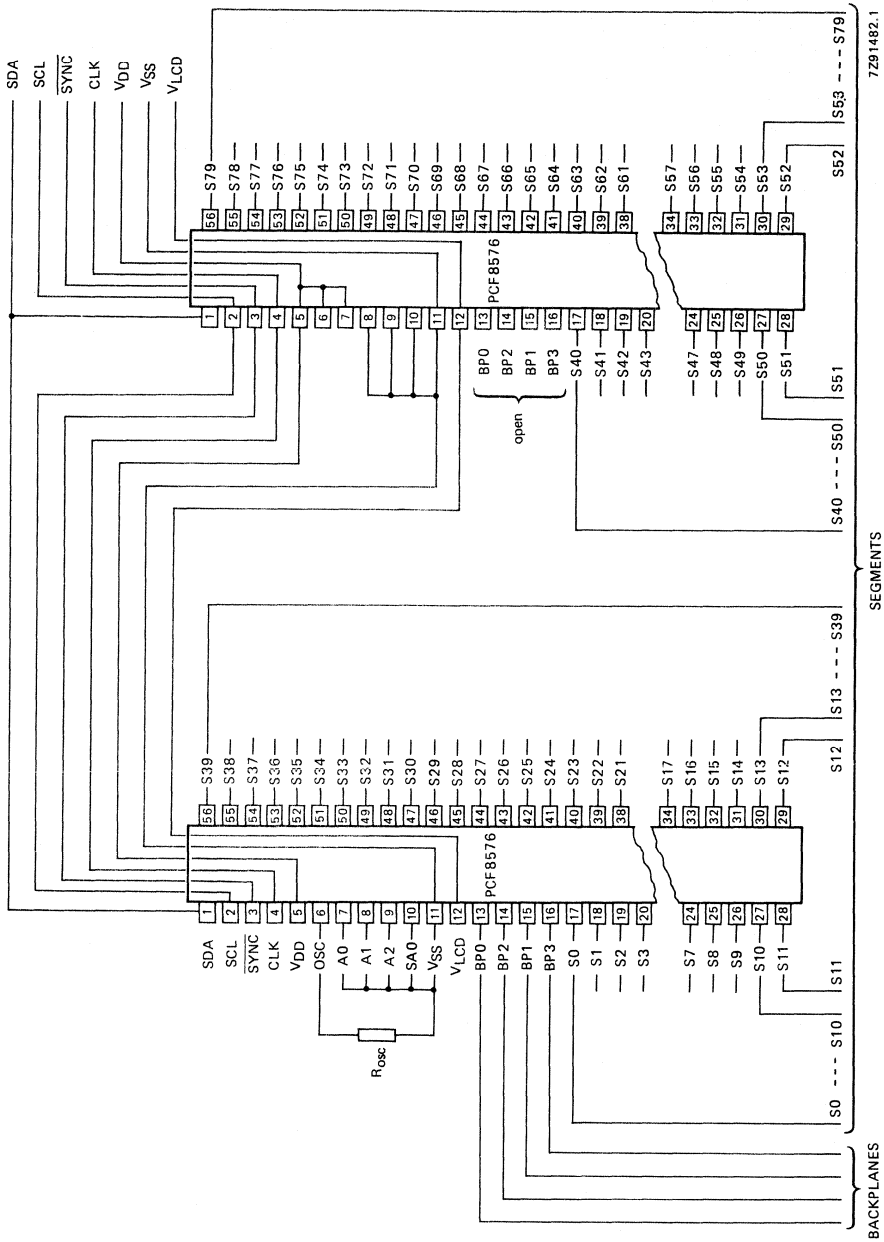


Fig. 25 Single plane wiring of packaged PCF8576s.

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig. 26). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between the V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

Fig. 27 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

APPLICATION INFORMATION (continued)

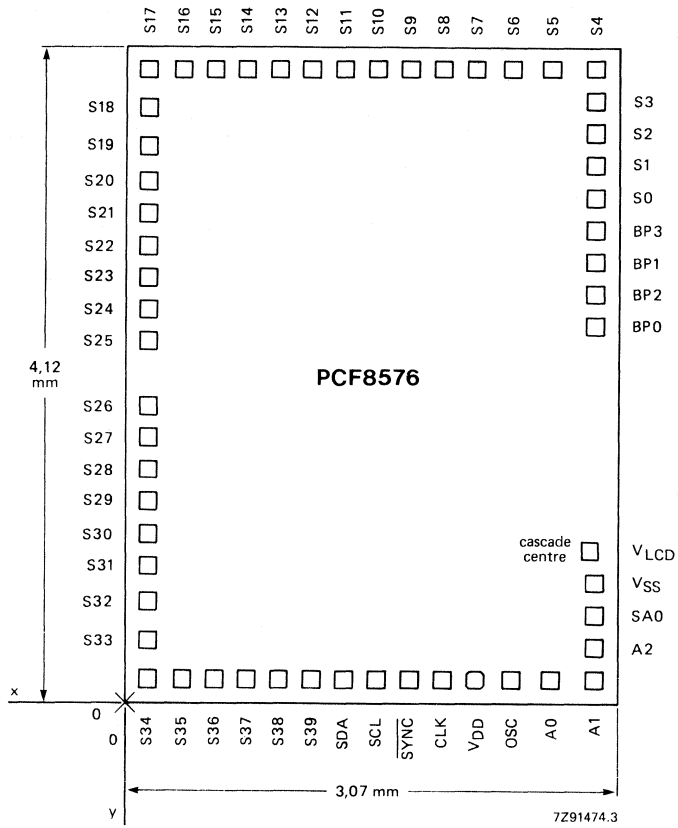


Fig. 26 PCF8576 bonding pad locations.

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0, Fig. 26).

Dimensions in μm

pad	x	y	
S34	160	160	bottom
S35	380	↑	↑
S36	580		
S37	780		
S38	980		
S39	1180		
SDA	1380		
SCL	1580		
$\overline{\text{SYNC}}$	1780		
CLK	1980		
V_{DD}	2180		
OSC	2400		
A0	2640	↓	↓
A1	2910	160	bottom
S17	160	3960	top
S16	380	↑	↑
S15	580		
S14	780		
S13	980		
S12	1180		
S11	1380		
S10	1580		
S9	1780		
S8	1980		
S7	2180		
S6	2400		
S5	2640		
S4	2910	3960	top

pad	x	y	
S33	160	400	left
S32	↑	640	↑
S31		860	
S30		1060	
S29		1260	
S28		1460	
S27		1660	
S26		1860	
S25		2260	
S24		2460	
S23		2660	
S22		2860	
S21		3060	
S20		3260	
S19		3480	
S18	160	3720	left
A2	2910	360	right
SA0	↕	560	↑
V_{SS}	2910	760	
V_{LCD}	2880	960	
BP0	2910	2360	
BP2	↑	2560	
BP1		2760	
BP3		2960	
S0		3160	
S1		3360	
S2		3560	
S3	2910	3760	right

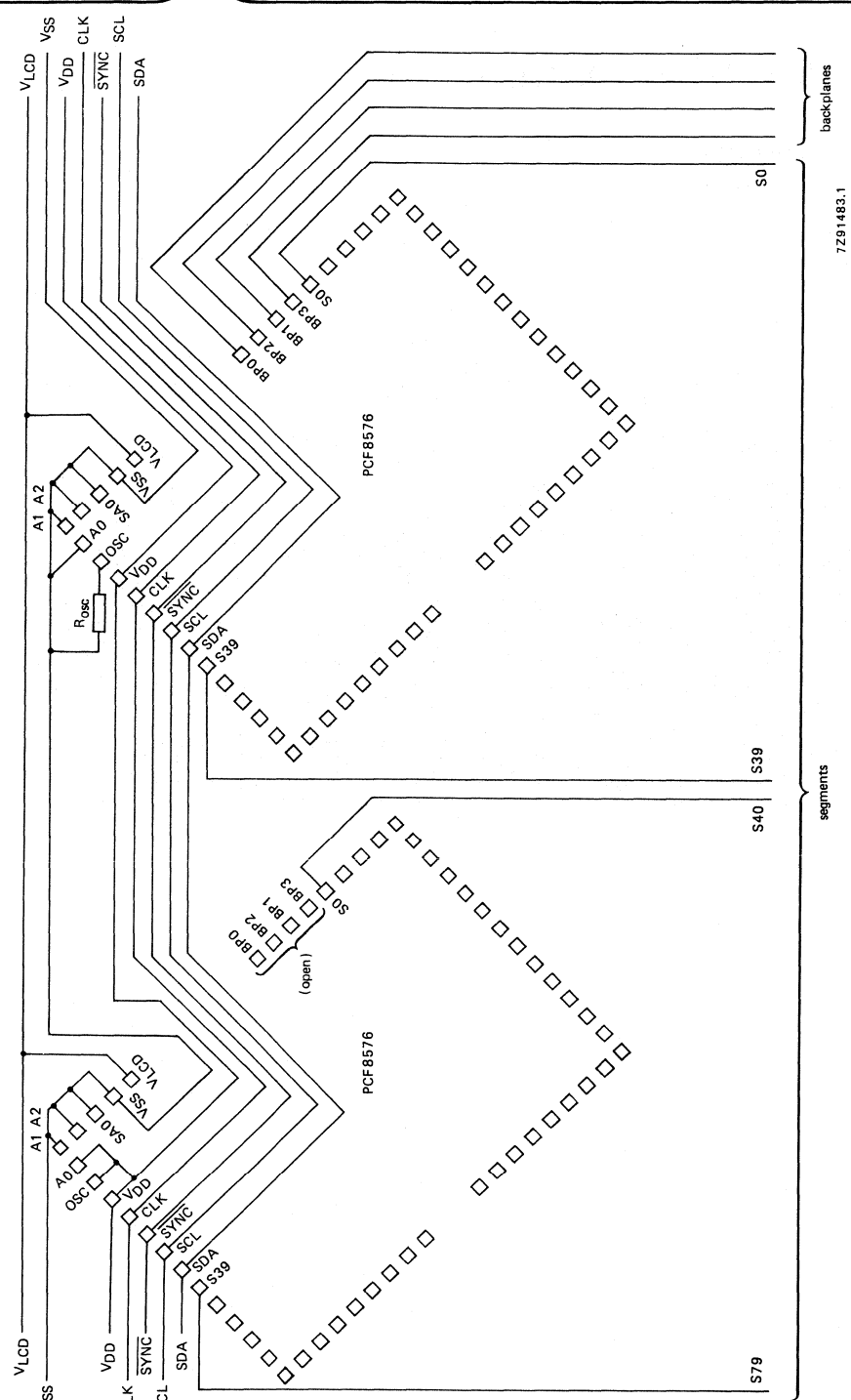


Fig. 27 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).

LCD DIRECT/DUPLEX DRIVER WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

The PCF8577 and PCF8577A differ only in their slave address.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2,5 to 9 V
- Low power consumption
- I²C bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device sub-address boundaries
- Display memory switching in direct drive mode
- May be used for I²C bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A)
- Power-on-reset sets all segments off (to blank)

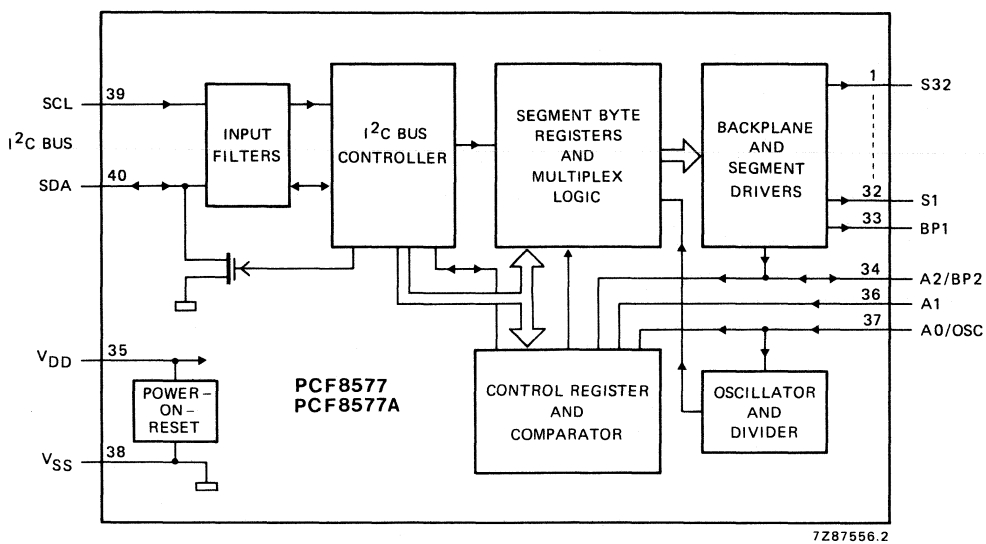


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP: 40-lead DIL; plastic (SOT-129).
PCF8577T, PCF8577AT: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

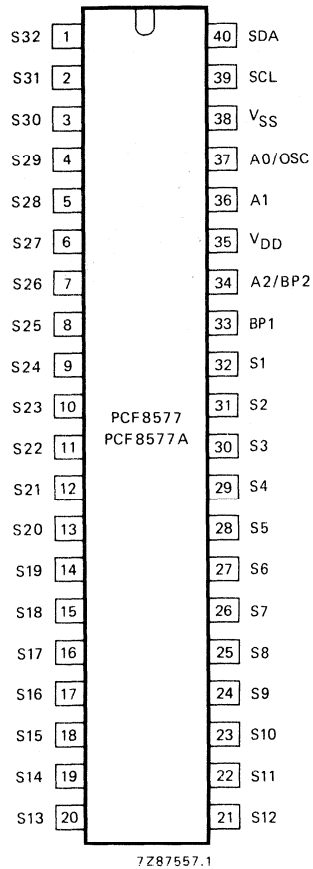


Fig. 2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C bus

40	SDA	I^2C bus data line
39	SCL	I^2C bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S1 – S32	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware sub-address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the expansion mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the expansion mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There are two slave addresses, one for PCF8577, and one for PCF8577A (see Fig. 14). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C bus protocol Fig. 15).

The control register is shown in more detail in Fig. 3. The least-significant bits select which device and which segment byte register are loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware sub-address input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

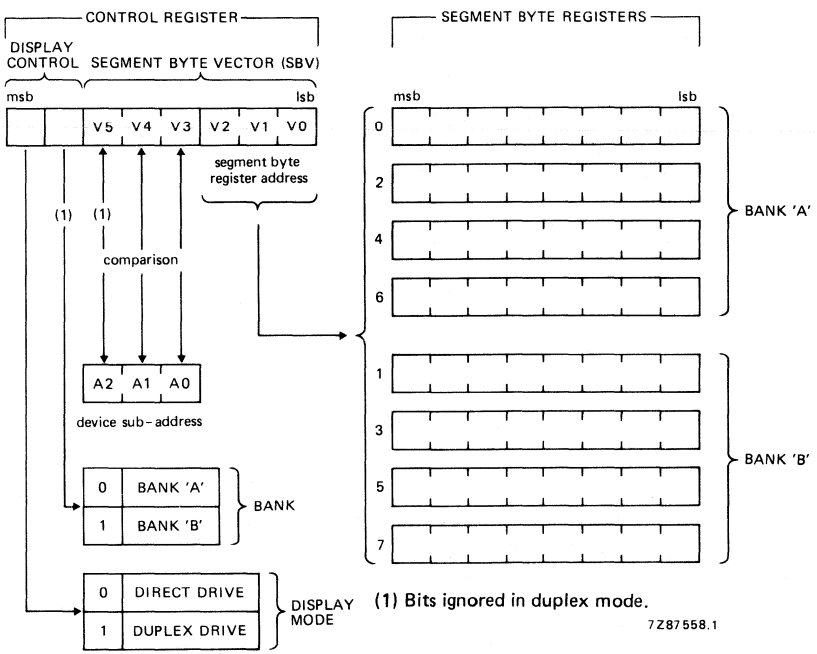


Fig. 3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

After each segment byte is loaded the SBV is incremented automatically, thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers, auto-incremented loading may proceed across device boundaries provided that the hardware sub-addresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig. 4.

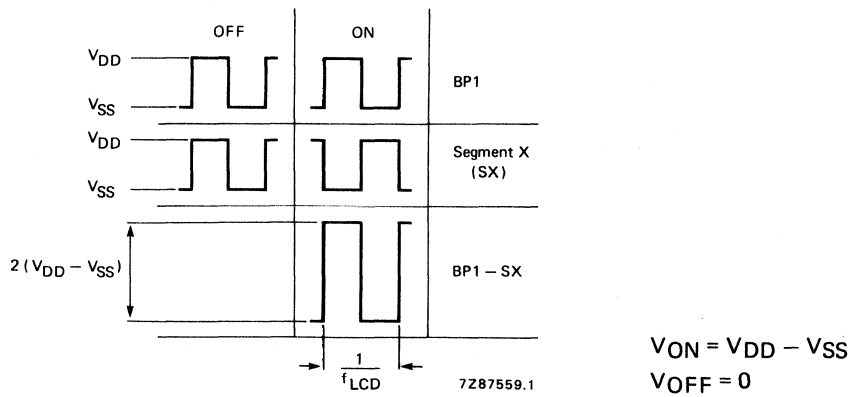


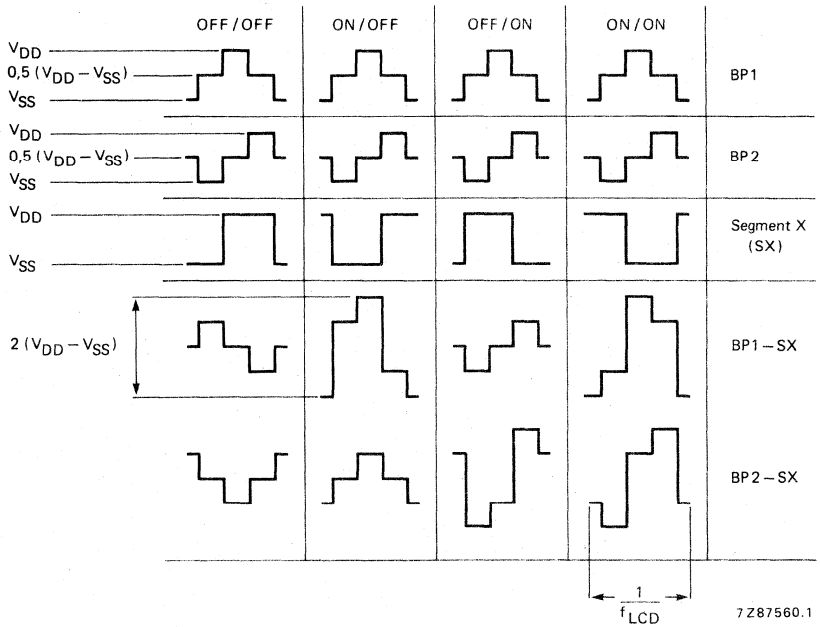
Fig. 4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig. 5.



$V_{ON} = 0{,}79\ (V_{DD} - V_{SS})$

$V_{OFF} = 0{,}35\ (V_{DD} - V_{SS})$

$\frac{V_{ON}}{V_{OFF}} = 2{,}26$

Fig. 5 Duplex mode display output waveforms.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

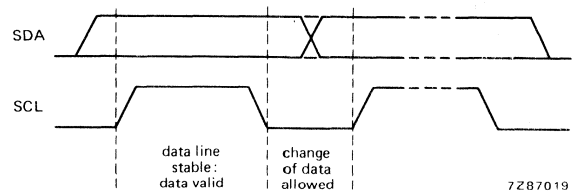


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

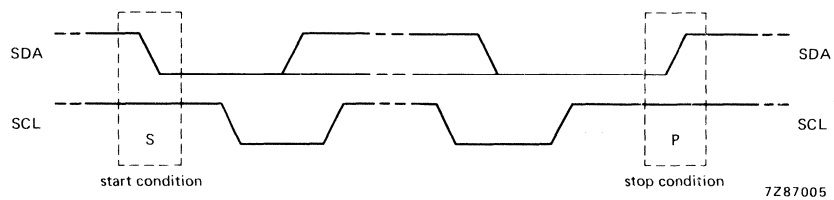


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

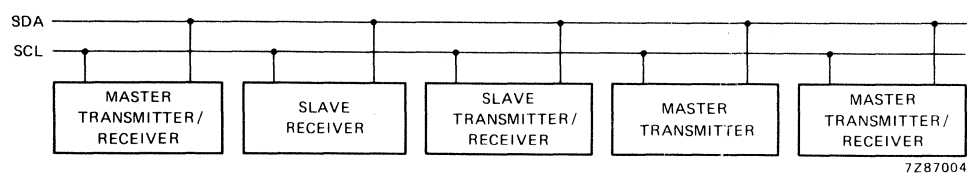


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

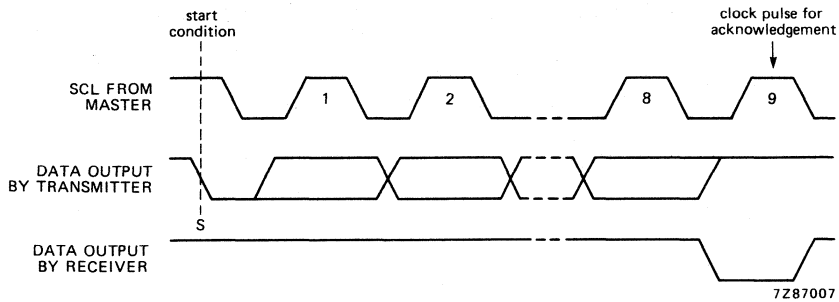


Fig. 9 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8577 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

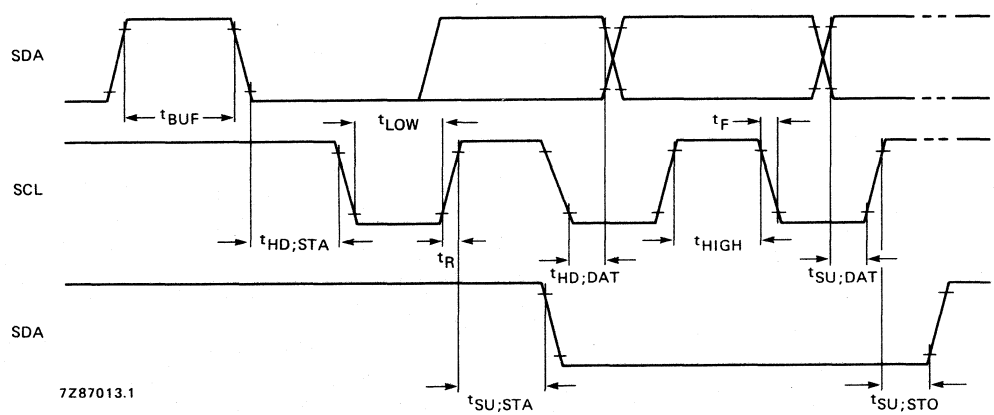


Fig. 10 Timing of the high-speed mode.

CHARACTERISTICS OF THE I^2C BUS (continued)

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

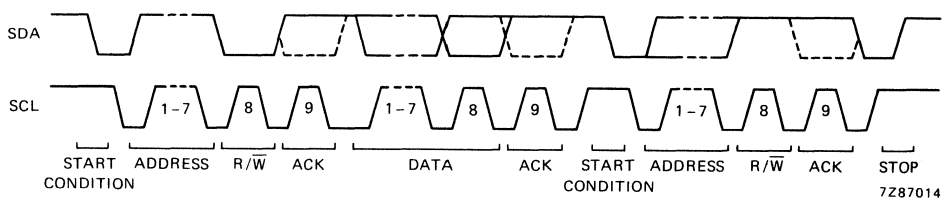


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

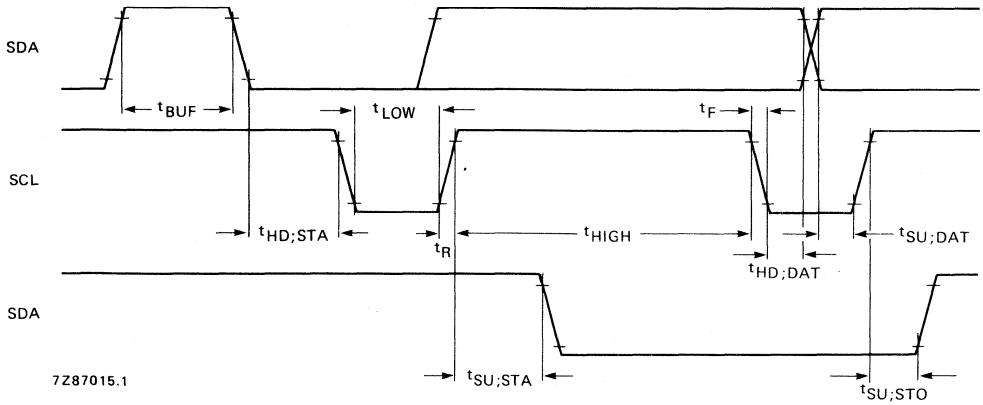


Fig. 12 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

CHARACTERISTICS OF THE I²C BUS (continued)

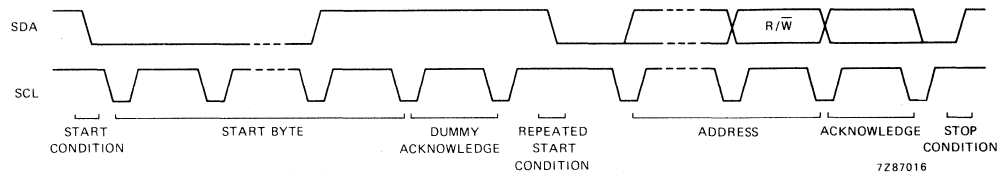


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

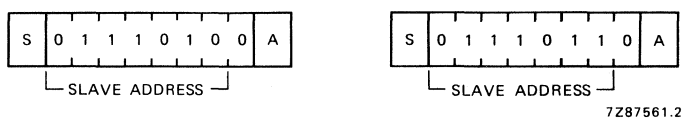
The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The slave address for PCF8577 and PCF8577A are shown in Fig. 14.



(a) PCF8577. (b) PCF8577A.

Fig. 14 PCF8577 and PCF8577A slave addresses.

I²C bus protocol

The PCF8577 I²C bus protocol is shown in Fig. 15.

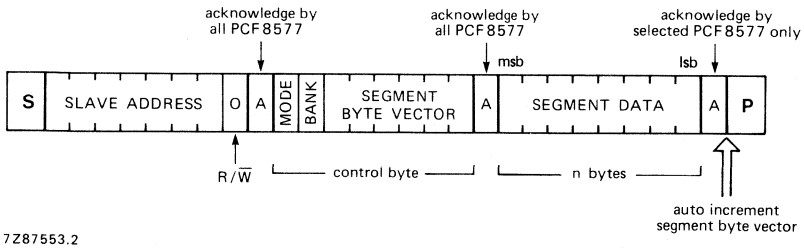


Fig. 15 I²C bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig. 14). All PCF8577 on the same bus acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DEVELOPMENT DATA

DISPLAY MEMORY MAPPING

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte — segment driver mapping in the direct drive mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

DISPLAY MEMORY MAPPING (continued)

Even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte — segment driver mapping in the duplex mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	M S B 7	6	5	4	3	2	1	L S B 0	BACKPLANE
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 11	V
Voltage on any pin	V_I	V_{SS} − 0,8 to V_{DD} + 0,8	V
D.C. input current	$\pm I_I$	max. 20	mA
D.C. output current	$\pm I_O$	max. 25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$, I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 500*	mW
Power dissipation per output	P	max. 100	mW
Operating ambient temperature range	T_{amb}	−40 to +85	°C
Storage temperature range	T_{stg}	−65 to +150	°C

* Derate 7,7 mW/K when $T_{amb} > 60$ °C.

DEVELOPMENT DATA

CHARACTERISTICS

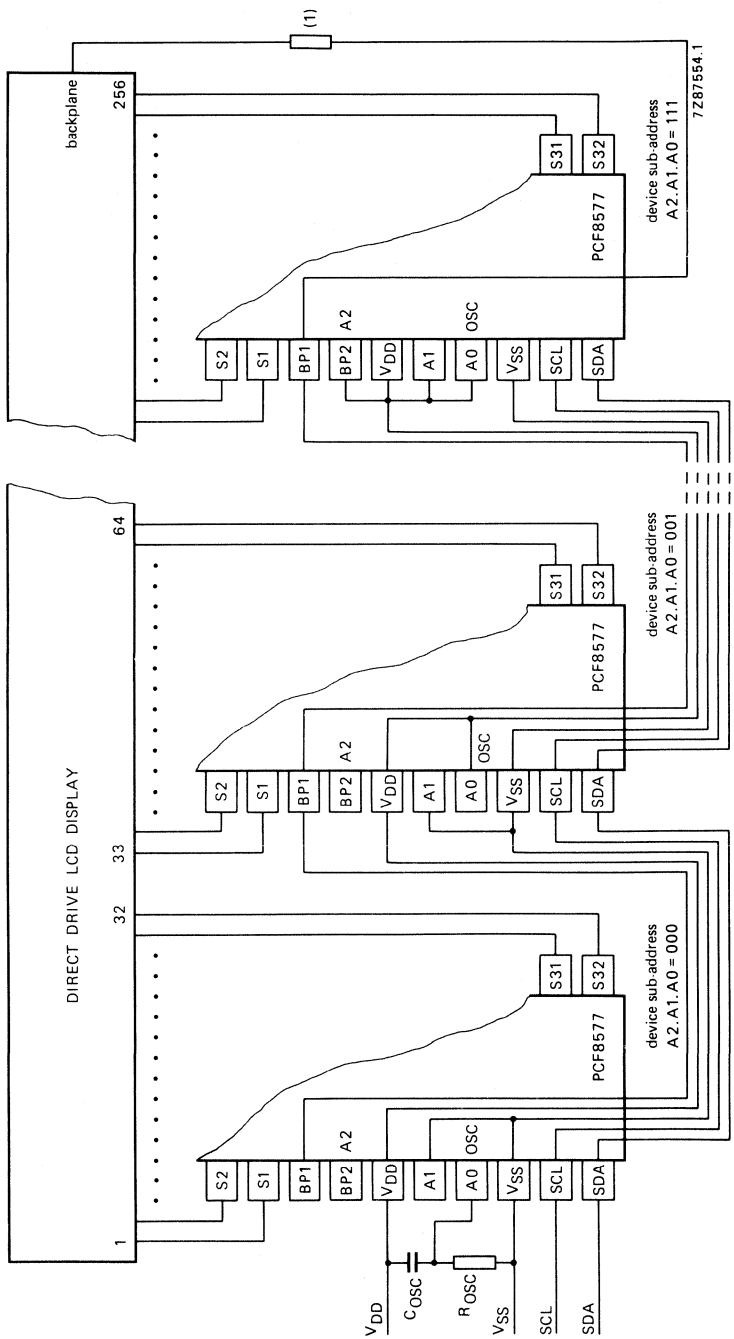
V_{DD} = 2,5 to 9 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.*	max.	unit
Supply voltage	V_{DD}	2,5	–	9,0	V
Supply current					
f_{SCL} = 100 kHz; no load; R_{OSC} = 1 MΩ	I_{DD}	–	80	250	μA
f_{SCL} = 0; no load; R_{OSC} = 1 MΩ; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	–	35	70	μA
Power-on-reset level**	V_{REF}	–	1,1	2,0	V
Input SCL; input/output SDA					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	9,0	V
output current LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA
output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
tolerable spike width on bus	t_{sw}	–	–	100	ns
input capacitance at V_I = V_{SS}	C_I	–	–	7	pF
A1 input leakage current at V_I = V_{SS} or V_{DD}	I_I	–	–	250	nA
A2/BP2 input current at V_I = V_{DD}	I_I	–	2,0	–	μA
A0/OSC input current at V_I = V_{SS} or V_{DD}	$\pm I_I$	–	5,0	–	μA
DC component of LCD driver	$\pm V_{BP}$	–	20	–	mV
Segment loads	C_{SX}	–	–	5	nF
	R_{SX}	1	–	–	MΩ
Segment output current					
at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL}	0,3	–	–	mA
Segment output current					
at V_{OH} = V_{DD} − 0,4 V; V_{DD} = 5 V	$-I_{OH}$	0,3	–	–	mA
Backplane load (direct drive)	C_{BP}	–	–	50	nF
	R_{BP}	100	–	–	kΩ
Backplane loads (duplex drive)	C_{BP}	–	–	35	nF
	R_{BP}	100	–	–	kΩ
Rise and fall times (V_{BP} − V_{SX})					
at maximum load	t_r, t_f	–	–	200	μs
Display frequency					
at C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz

* V_{DD} = 5 V; T_{amb} = 25 °C.

** The power-on-reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$.

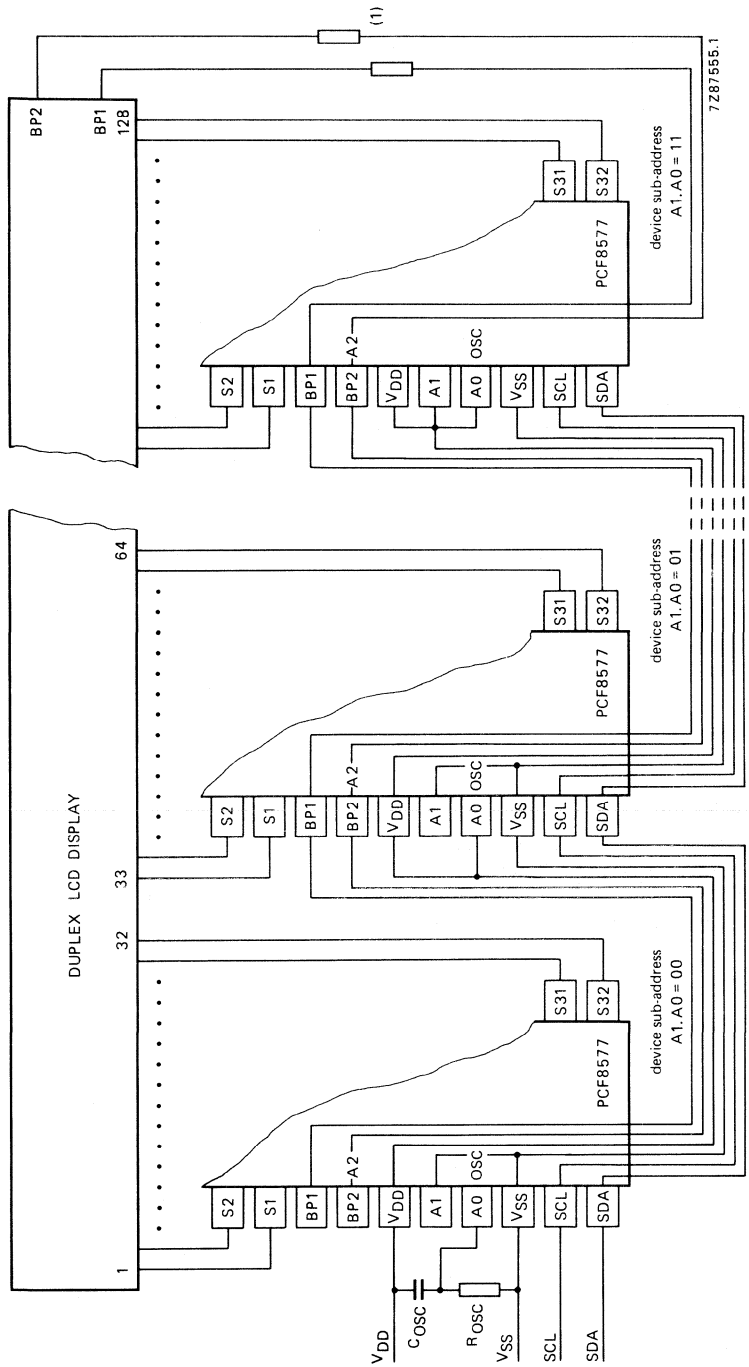
APPLICATION INFORMATION



(1) The series resistance of the display backplane must be greater than 1 Ω.

Fig. 16 Direct drive display; expansion to 256 segments using eight PCF8577.

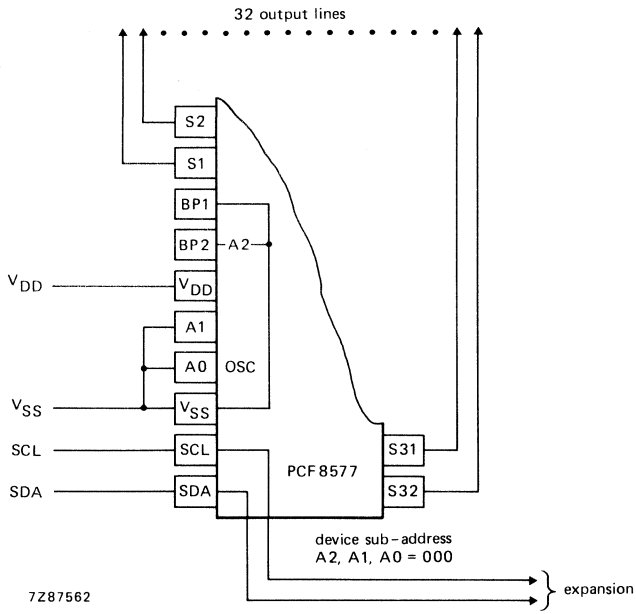
DEVELOPMENT DATA



(1) The series resistances of the display backplanes must be greater than 1 kΩ.

Fig. 17 Duplex display; expansion to 2 x 128 segments using four PCF8577.

APPLICATION INFORMATION (continued)



Notes

1. MODE bit must always be set to 0 (direct drive)
2. BANK switching is permitted
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation)

Fig. 18 Use of PCF8577 as 32-bit output expander in I²C bus application.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

256 × 8-bit STATIC CMOS EEPROM WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8582 is a 2K-bit 5 V electrically erasable programmable read only memory (EEPROM) organized as 256 by 8 bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I²C bus, an eight pin DIL package is sufficient. Up to eight PCF8582 devices may be connected to the I²C bus.

Chip select is accomplished by three address inputs.

Features

- Non-volatile storage of 2K-bit organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- Power on reset
- 10 000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571 and PCD8572

PACKAGE OUTLINES

PCF8582P: 8-lead DIL; plastic (SOT-97).
PCF8582T: 16-lead mini pack plastic (SO-16L; SOT-162A).

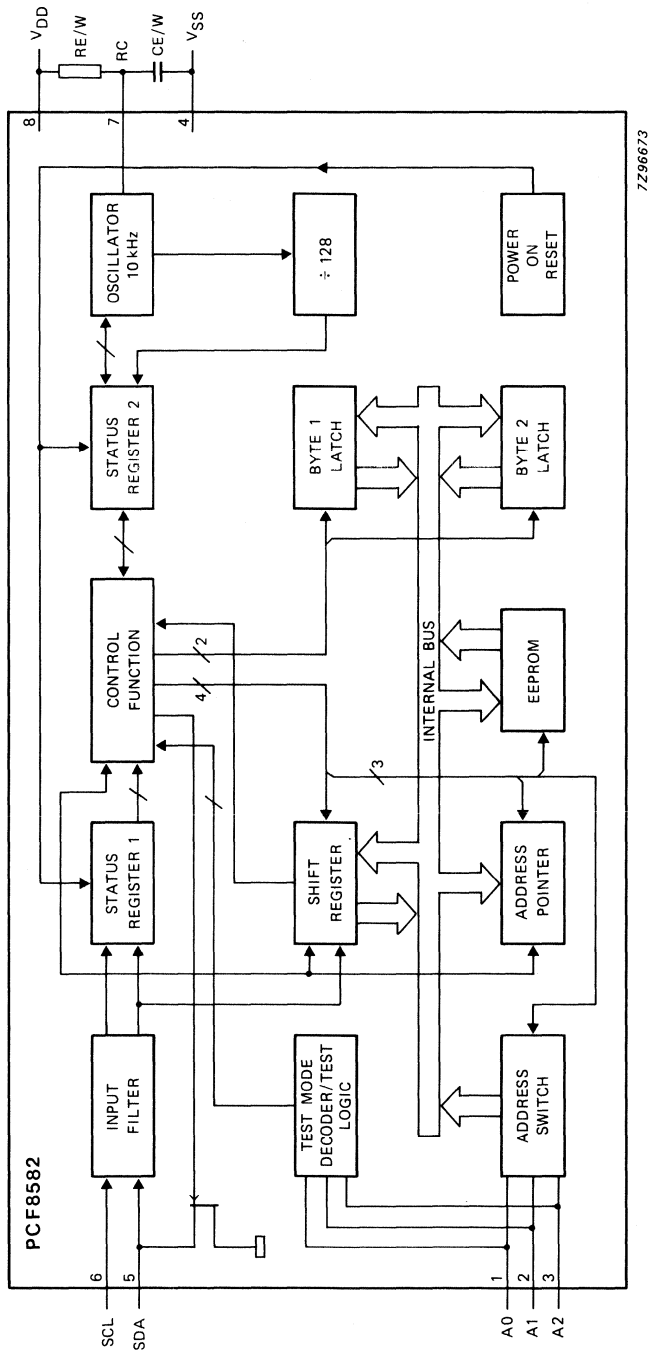


Fig. 1 Block diagram.

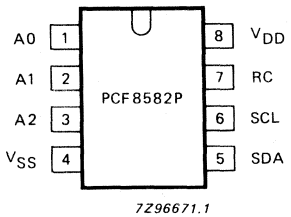


Fig. 2(a) Pinning diagram; PCF8582P.

PINNING

1	A0	
2	A1	address inputs/test
3	A2	mode select
4	V_{SS}	ground
5	SDA	I^2C bus lines
6	SCL	I^2C bus lines
7	RC	input for timer constant
8	V_{DD}	positive supply

DEVELOPMENT DATA

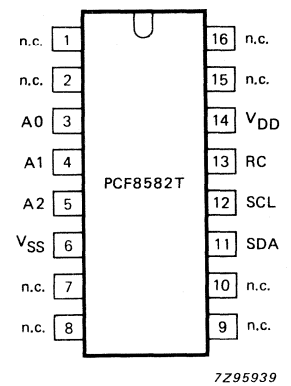


Fig. 2(b) Pinning diagram; PCF8582T.

1	NC	
2	NC	
3	A0	
4	A1	address inputs/test
5	A2	mode select
6	V_{SS}	ground
7	NC	
8	NC	
9	NC	
10	NC	
11	SDA	I^2C bus lines
12	SCL	I^2C bus lines
13	RC	input for timer constant
14	V_{DD}	positive supply
15	NC	
16	NC	

FUNCTIONAL DESCRIPTION

Characteristics of the I²C bus

The I²C bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:
Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:
Bus not busy: both data and clock lines remain HIGH.
Start data transfer: a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition.
Stop data transfer: a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transfered between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C bus specifications a low-speed mode (2 kHz clock rate) and a high-speed mode (100 kHz clock rate) are defined. The PCF8582 operates in both modes.
By definition a device that gives out a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse.
Set-up-and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

Note

The general characteristics and detailed specification of the I²C bus is available on request.

I²C bus protocol

The I²C bus configuration for different READ and WRITE cycles of the PCF8582 are shown in Fig. 3.

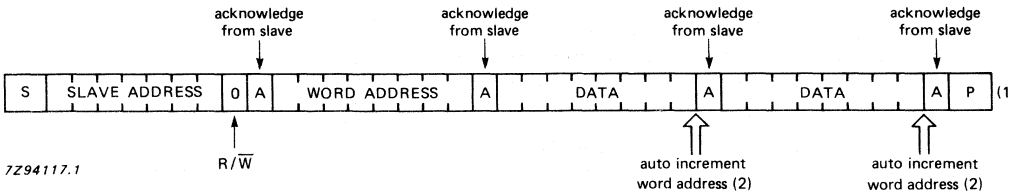


*Fig. 3(a) Slave receiver ERASE/WRITE mode.

(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission; the duration of the erase/write cycle is approximatly 30 ms if only one byte is written, and 60 ms, if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via I²C bus.

(2) The second data byte is voluntary. It is not allowed to erase/write more than two bytes.

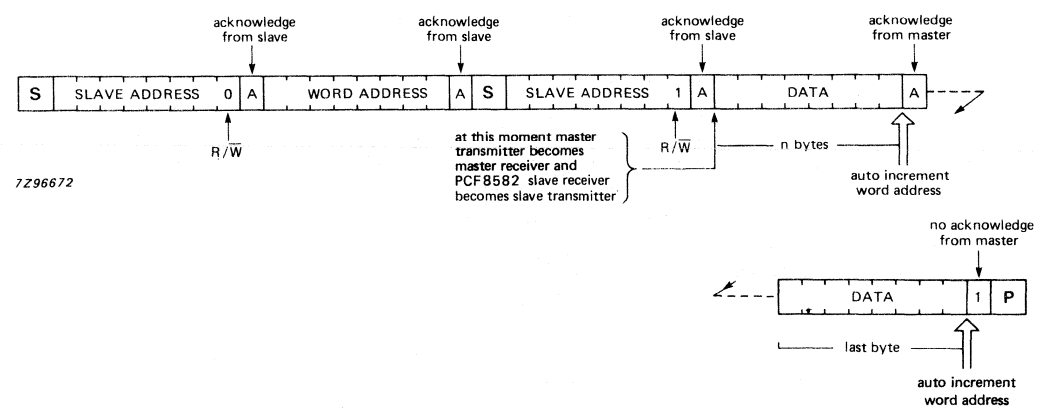


Fig. 3(b) Master reads PCF8582 slave after setting word address. (WRITE word address; READ data).

Note: The slave address is defined in accordance with the I²C bus specification as:

1	0	1	0	A2	A1	A0	R/$\overline{W}$

DEVELOPMENT DATA

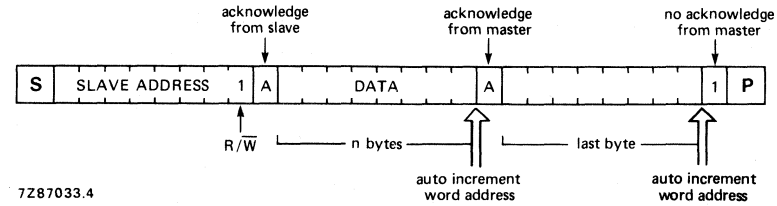


Fig. 3(c) Master reads PCF8582 slave immediately after first byte (READ mode).

I²C bus timing

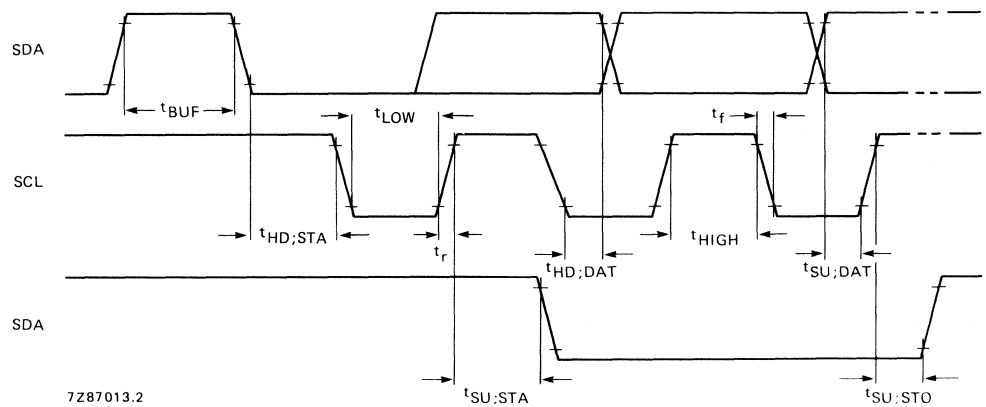


Fig. 4 I²C bus timing.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 7 V
Voltage, on any input pin (input impedance 500 Ω)	V_I	V_{SS}−0,8 to V_{DD} +0,8 V
Operating temperature range	T_{amb}	−40 to +85 °C
Storage temperature range	T_{stg}	−65 to +150 °C
Current into any input pin	I_I	1 mA
Output current	I_O	10 mA

CHARACTERISTICS

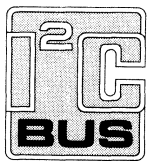
V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5	5,5	V
Operating supply current, READ (f_{SCL} = 100 kHz; $V_{DD\ max}$)	I_{DDR}	–	–	0,4	mA
Operating supply current, WRITE/ERASE($V_{DD\ max}$)	I_{DDW}	–	–	2,0	mA
Standby supply current ($V_{DD\ max}$)	I_{DDO}	–	–	10	μA
Input SCL and input/output SDA					
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input voltage HIGH	V_{IH}	3	–	V_{DD}+0,8	V
Output voltage LOW (I_{OL} = 3 mA, V_{DD} = 4,5 V)	V_{OL}	–	–	0,4	V
Output leakage current HIGH (V_{OH} = V_{DD})	I_{OH}	–	–	1	μA
Input leakage current (A0,A1,A2,SCL), (note 1)	$\pm I_{IN}$	–	–	1	μA
Clock frequency	f_{SCL}	0	–	100	kHz
Input capacity (SCL,SDA)	C_I	–	–	7	pF
Time the bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	μs
Hold time start condition. After this period the first clock pulse is generated	$t_{HD;STA}$	4	–	–	μs
The LOW period of the clock	t_{LOW}	4,7	–	–	μs
The HIGH period of the clock	t_{HIGH}	4	–	–	μs
Set-up time for start condition (only relevent for a repeated start condition)	$t_{SU;STA}$	4,7	–	–	μs
Hold time DATA for:					
I²C bus compatible masters	$t_{HD;DAT}$	5	–	–	μs
I²C devices (note 2)	$t_{HD;DAT}$	200	–	–	ns
Set-up time DATA	$t_{SU;DAT}$	500	–	–	ns
Rise time for both SDA and SCL lines	t_R	–	–	1	μs
Fall time for both SDA and SCL lines	t_F	–	–	300	ns
Set-up time for stop condition	$t_{SU;STO}$	4,7	–	–	μs
Erase/write timer constant (note 3)					
Erase/write cycle time	$t_{E/W}$	20	–	100	ms
Erase/write timing capacitor for erase/write cycle of 30 ms (± 10% tolerance)	$C_{E/W}$	–	3,3	–	nF
Erase/write timing resistor for erase/write cycle of 30 ms (± 5% tolerance)	$R_{E/W}$	–	56	–	kΩ
Data retention time (T_{amb} = +55 °C)	t_S	10	–	–	years

DEVELOPMENT DATA

Notes to the characteristics

1. Selection of the chip address is done by connecting the A0, A1, and A2 inputs either to V_{SS} or V_{DD}.
2. A transmitter must internally provide a hold time to bridge the undefined region (maximum 300 ns) of the falling edge of SCL.
3. Endurance (number of erase/write cycles), NE/W, is 10^4 E/W cycles.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CLOCK CALENDAR WITH 256 × 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32,768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I^2C bus interface operating supply voltage: 2,5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1,0 V to 6 V
- Data retention voltage: 1,0 V to 6 V
- Operating current (f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32,768 kHz or 50 Hz time base
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

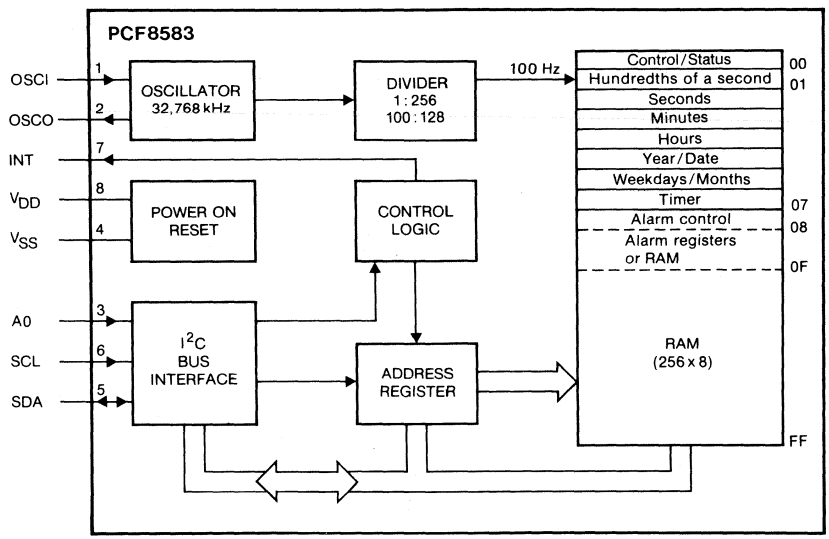


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT-97).
PCF8583T: 8-lead mini-pack; plastic (SO-8L; SOT-176).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input	
2	OSCO	oscillator output	
3	A0	address input	
4	V_{SS}	negative supply	
5	SDA	serial data line	I^2C bus
6	SCL	serial clock line	I^2C bus
7	INT	open drain interrupt output (active low)	
8	V_{DD}	positive supply	

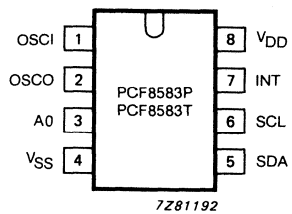


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8); note 1	V_{DD}		−0,8 to 8,0 V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8 V
DC input current (any input)	I_I	max.	10 mA
DC output current (any output)	I_O	max.	10 mA
Supply current (pin 4 or pin 8)	I_{DD}; I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	50 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−40 to + 85 °C

Note

1. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32,768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is set a 32,768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event-counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore faulty reading of the count during a carry condition is prevented.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled).

When a timer function without any alarm function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C bus. All functions and options are controlled by the contents of the control/status register (see Fig. 3).

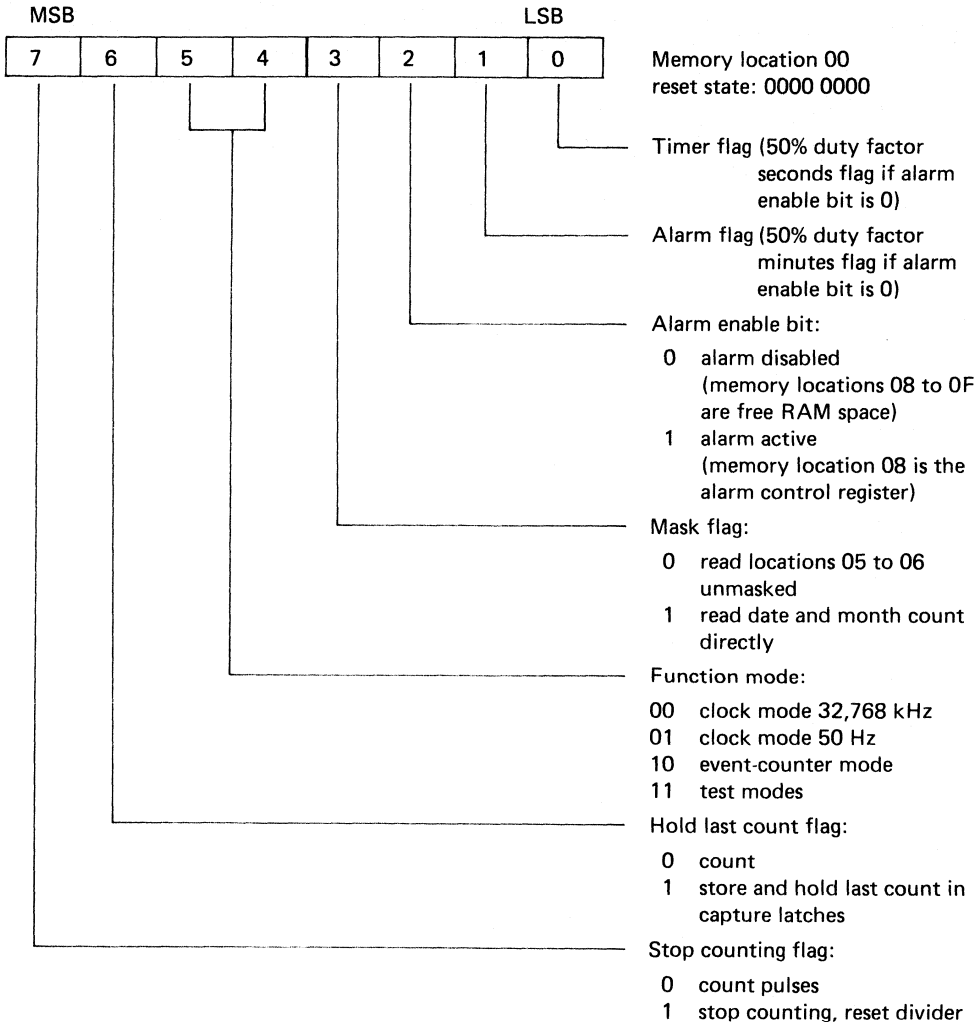


Fig. 3 Control/status register.

Counter registers

In the different modes the counter registers are programmed and arranged as shown in Fig. 4. Counter cycles are listed in Table 1.

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig. 5.

The year and date are packed into memory location 05 (see Fig. 6). The weekdays and months are packed into memory location 06 (see Fig. 7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

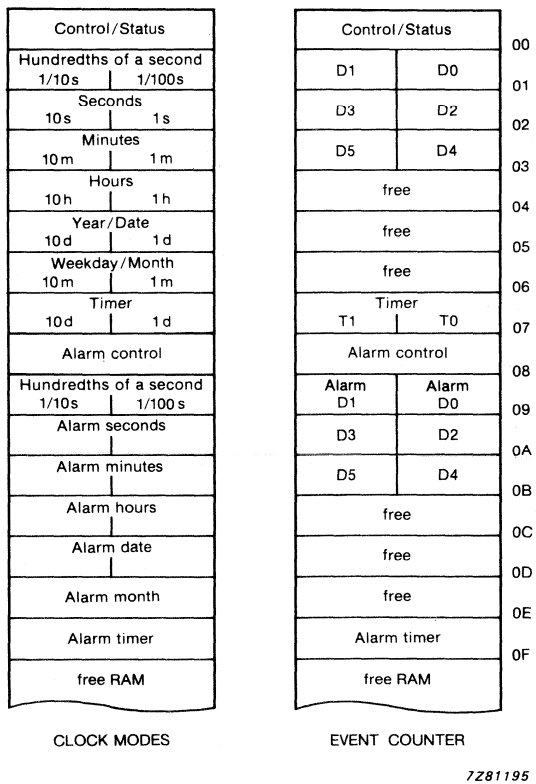
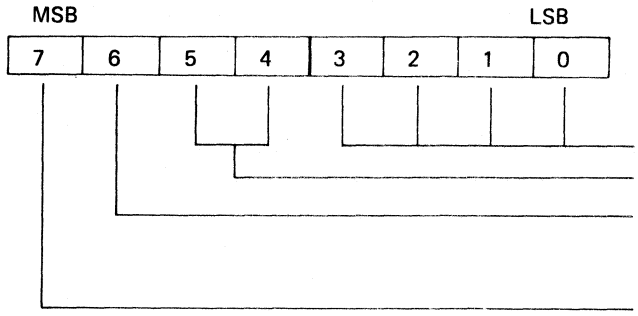


Fig. 4 Register arrangement.

Counter registers (continued)



Memory location 04 (hours counter)
reset state: 0000 0000

Unit hours BCD

Ten hours (0 to 2 binary)

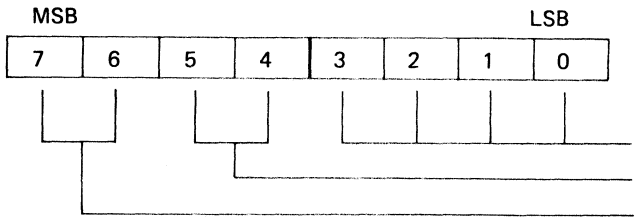
AM/PM flag:

0 AM
1 PM

Format:

0 24 h format, AM/PM flag remains unchanged
1 12 h format, AM/PM flag will be updated

Fig. 5 Format of the hours counter.



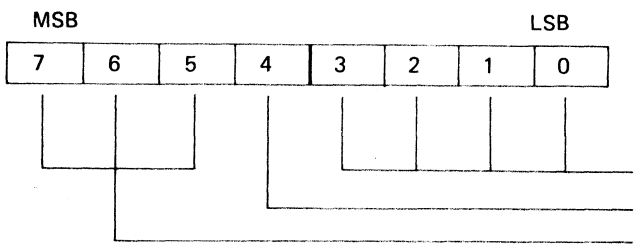
Memory location 05 (year/date)
reset state: 0000 0001

Unit days BCD

Ten days (0 to 3 binary)

Year (0 to 3 binary, read as 0 if the mask flag is set)

Fig. 6 Format of the year/date counter.



Memory location 06 (weekdays/months)
reset state: 0000 0001

Unit months BCD

Ten months

Weekdays (0 to 6 binary, read as 0 if the mask flag is set)

Fig. 7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

unit	counting cycle	carry to the next unit	contents of the month counter
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
date	01 to 31 01 to 30 01 to 29 01 to 28	31 to 01 30 to 01 29 to 01 28 to 01	1, 3, 5, 7, 8, 10, 12 4, 6, 9, 11 2, year = 0 2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer/days	00 to 99	no carry	

Alarm control register

When the alarm enable bit of the control/status register is set the alarm control register (address 08) is activated. All alarm, timer and interrupt output functions are controlled by the contents of the alarm control register (see Figs 8a and 8b).

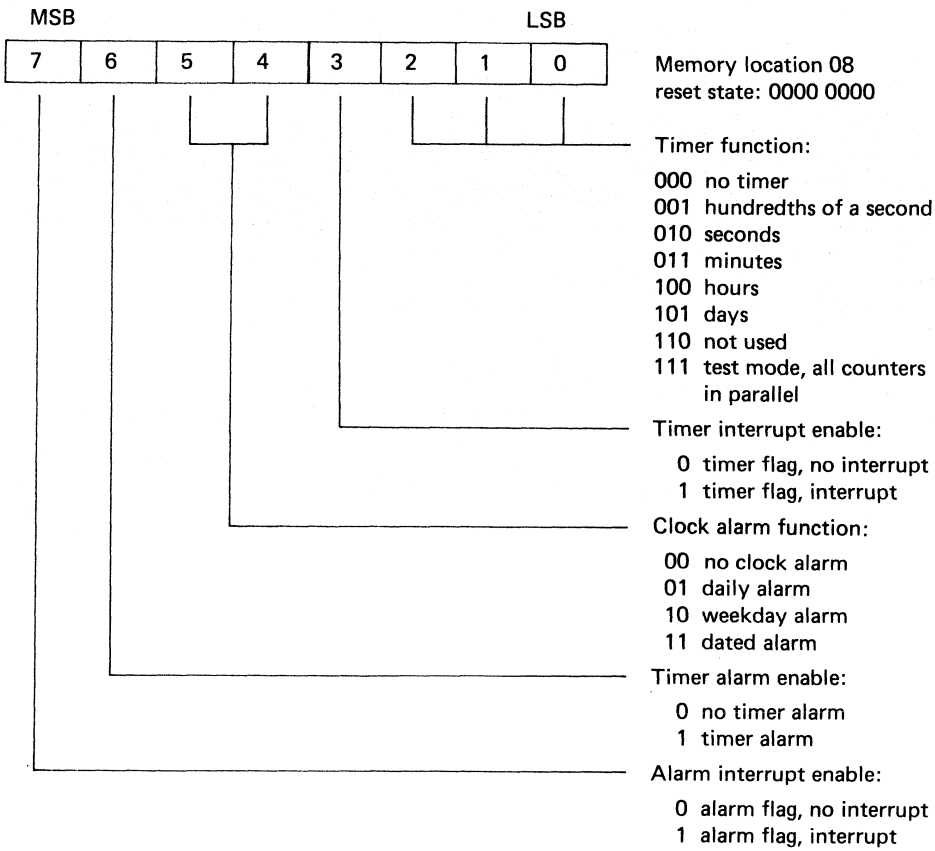
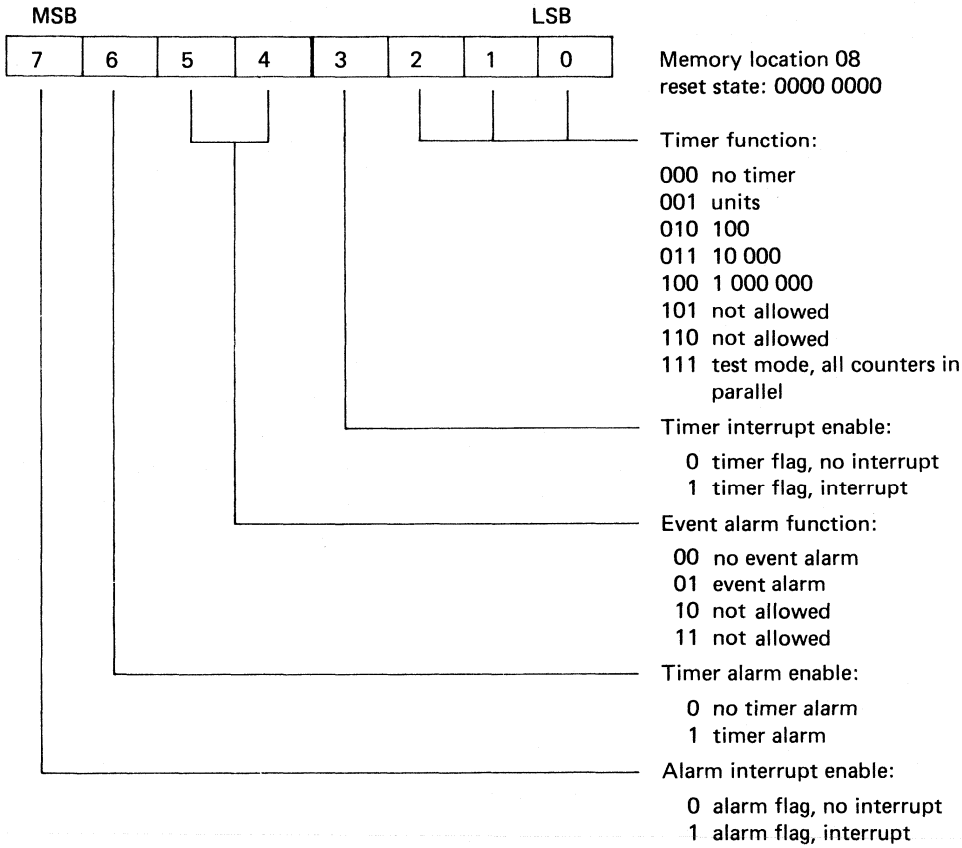


Fig. 8a Alarm control register, clock modes.



DEVELOPMENT DATA

Fig. 8b Alarm control register, event-counter mode.

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig. 9).

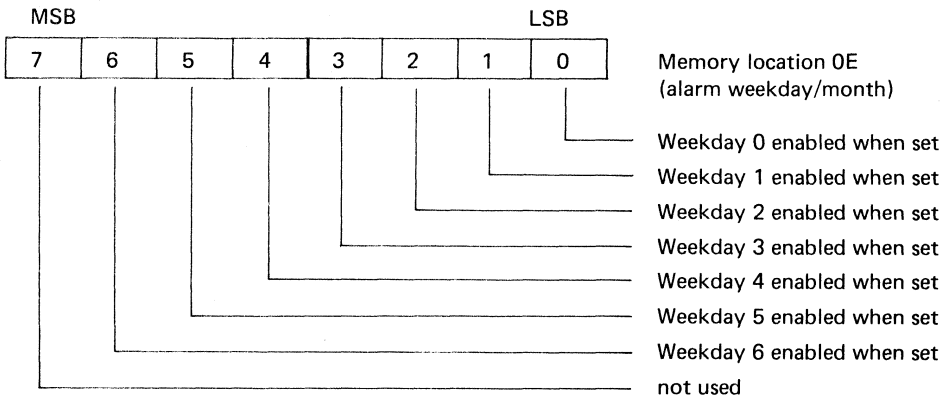


Fig. 9 Selection of alarm weekdays.

Interrupt output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (active LOW) when the alarm flag or the timer flag is set. In the clock mode without alarm the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

Oscillator and divider

A 32,768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator. The oscillator frequency is scaled down to 128 Hz by the divider. A 100 Hz clock signal is derived from this signal.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I^2C bus interface, the control/status register and all clock counters are reset. The device starts time keeping in the 32,768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00.

A second level-sensitive reset signal to the I^2C bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction but will not latch-up the device.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

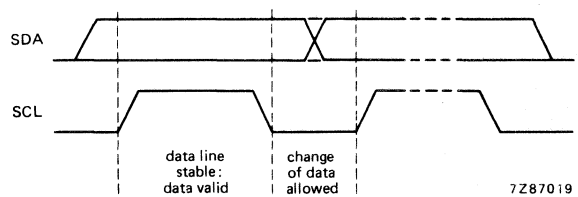


Fig. 10 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

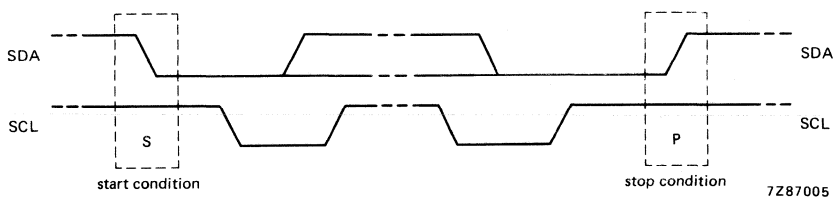


Fig. 11 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

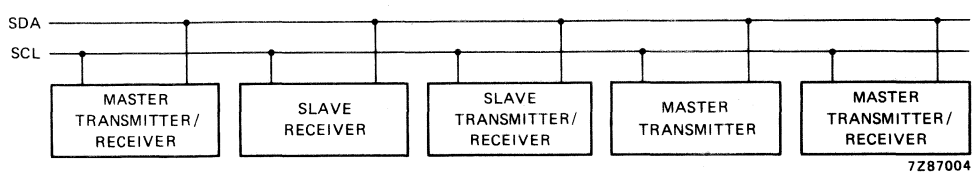


Fig. 12 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

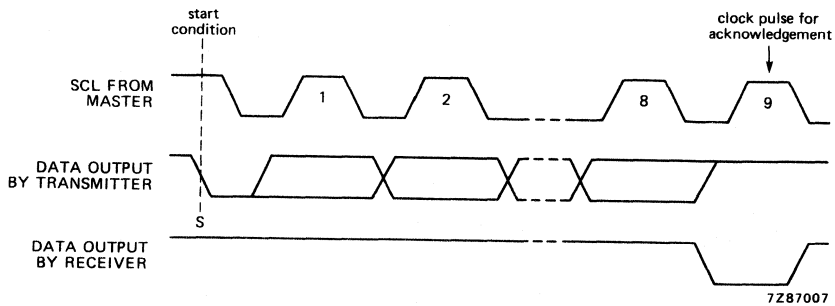


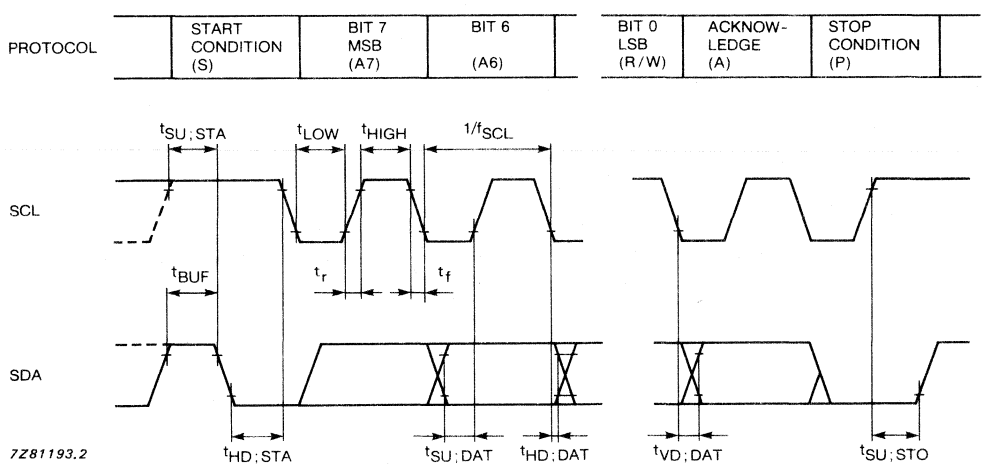
Fig. 13 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_r	–	–	1,0	μs
SCL and SDA fall time	t_f	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs



I²C bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for the different PCF8583 READ and WRITE cycles is shown in Fig. 15.

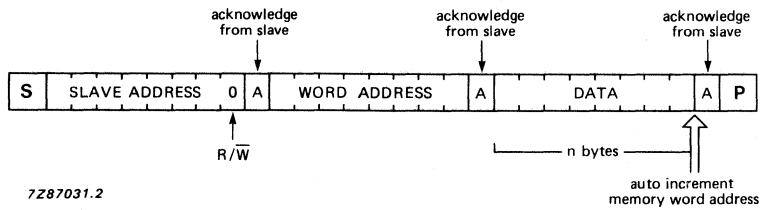


Fig. 15a Master transmits to slave receiver (WRITE mode).

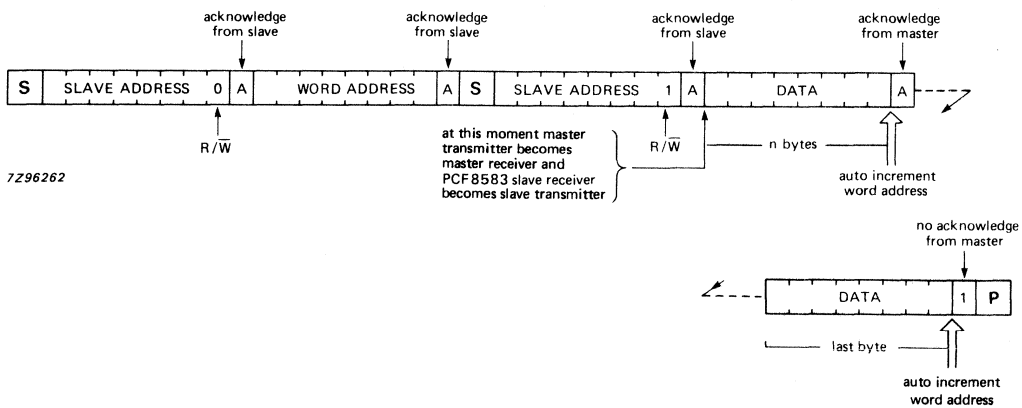


Fig. 15b Master reads after setting word address (WRITE word address; READ data).

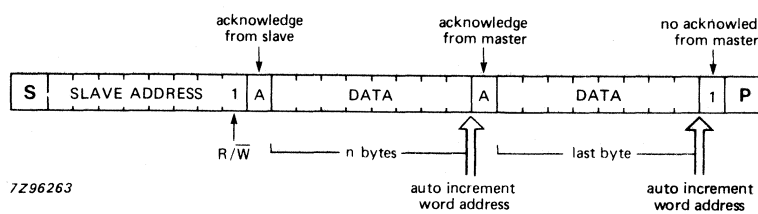


Fig. 15c Master reads slave immediately after first byte (READ mode).

CHARACTERISTICS

V_{DD} = 2,0 to 6,0 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (operating)	V_{DD}	2,5	–	6	V
Supply voltage (clock)	V_{DD}	1,0	–	6	V
Supply current T_{amb} = 0 to 70 °C operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
Clock at V_{DD} = 5 V	I_{DDO}	–	10	50	μA
Clock at V_{DD} = 1 V	I_{DDO}	–	2	10	μA
Power-on reset voltage level (note 1)	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW (note 2)	V_{IL}	–0,8	–	0,3 x V_{DD}	V
Input voltage HIGH (note 2)	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
Input leakage current at V_I = V_{DD} or V_{SS}	± I_I	–	–	250	nA
Input capacitance (SCL, SDA) at V_I = V_{SS}	C_I	–	–	7	pF
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V (note 3)	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = –25 to + 70 °C (note 3)	I_{DDR}	–	–	2	μA
Oscillator					
Integrated oscillator capacitance	C_{OSC}	–	40	–	pF
Oscillator stability for: ΔV_{DD} = 100 mV at V_{DD} = 1,5 V; T_{amb} = 25 °C	f/f_{OSC}	–	2×10^{-6}	–	–

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	KΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	5	–	25	pF

Notes to characteristics

1. The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0,5 mA.
3. Event or 50 Hz mode only (no Quartz).

APPLICATION INFORMATION

The PCF8583 slave address has a fixed combination 1010 as group 1.

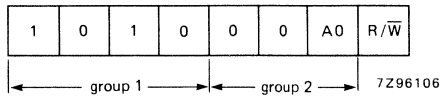


Fig. 16 PCF8583 address.

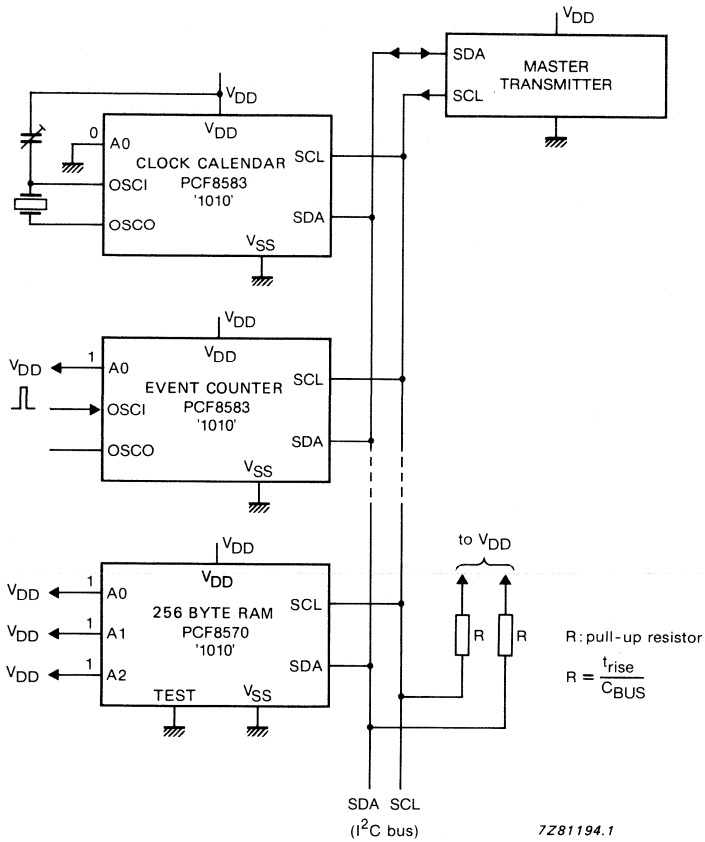


Fig. 17 PCF8583 application diagram.

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

FEATURES

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT-38).
PCF8591T:16-lead mini-pack; plastic (SO-16L; SOT-162A).

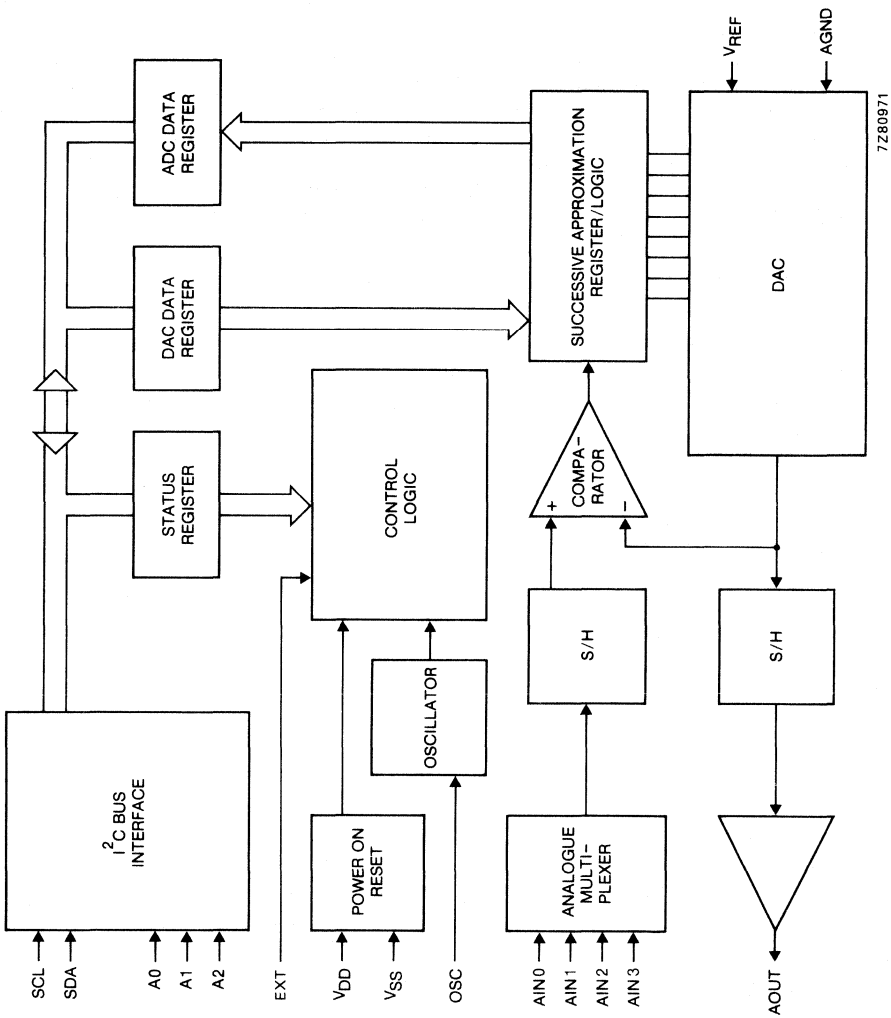


Fig. 1 Block diagram.

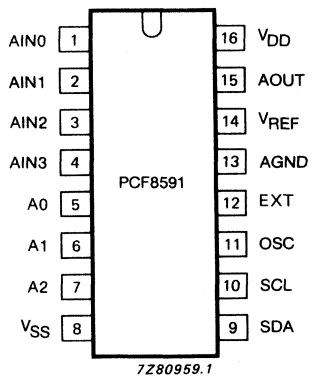


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

DEVELOPMENT DATA

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

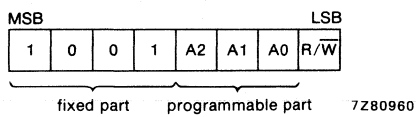


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

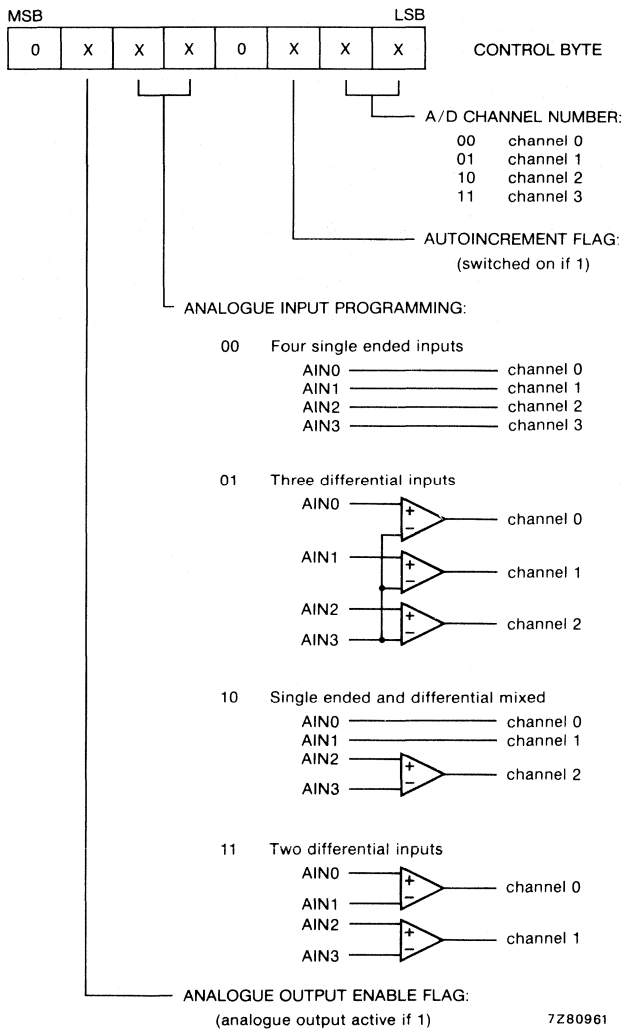


Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

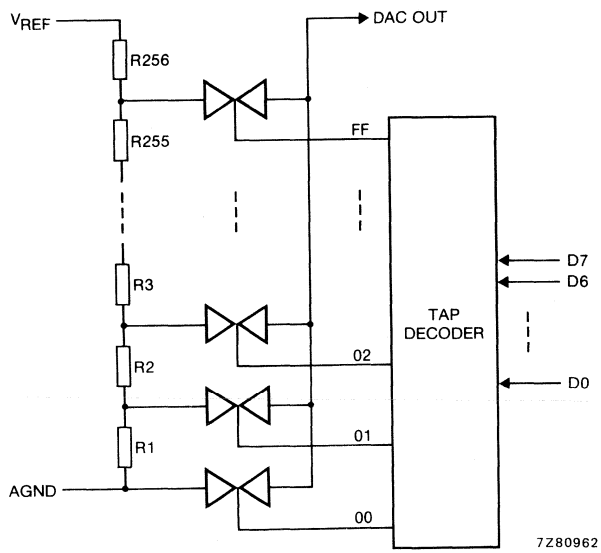


Fig. 5 DAC resistor divider chain.

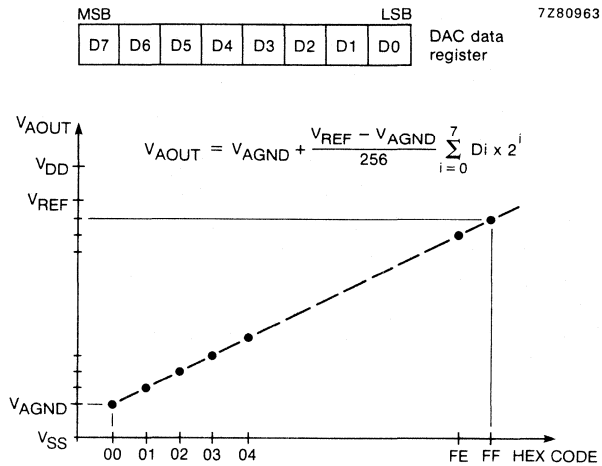


Fig. 6 DAC data and d.c. conversion characteristics.

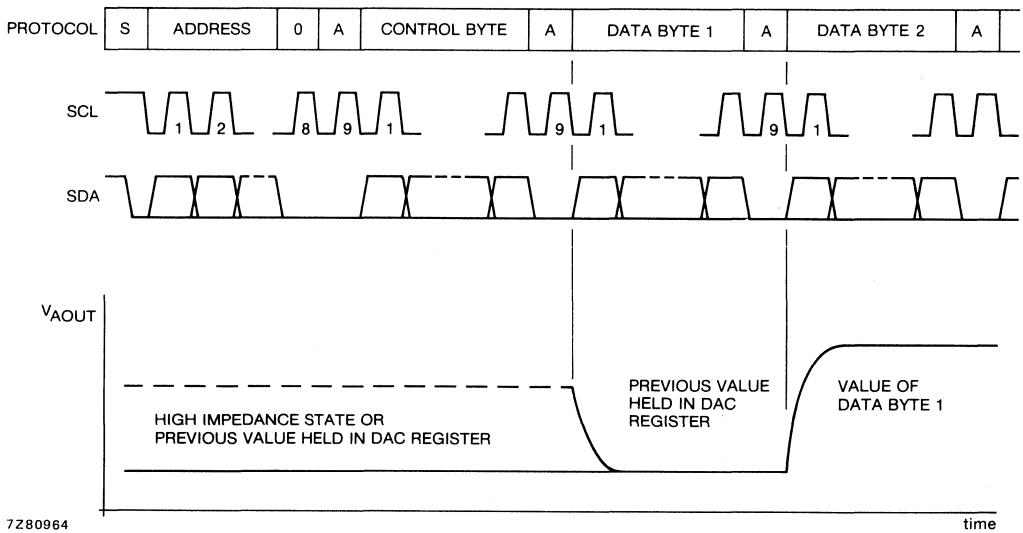


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

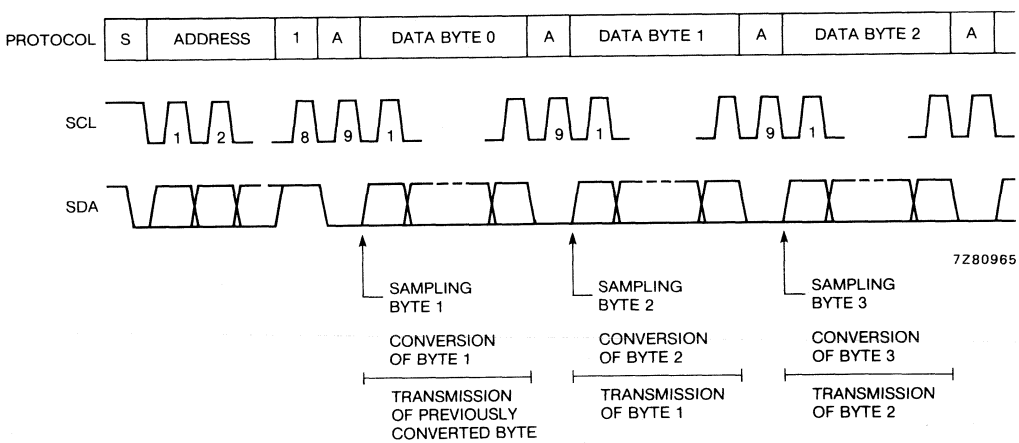


Fig. 8 A/D conversion sequence.

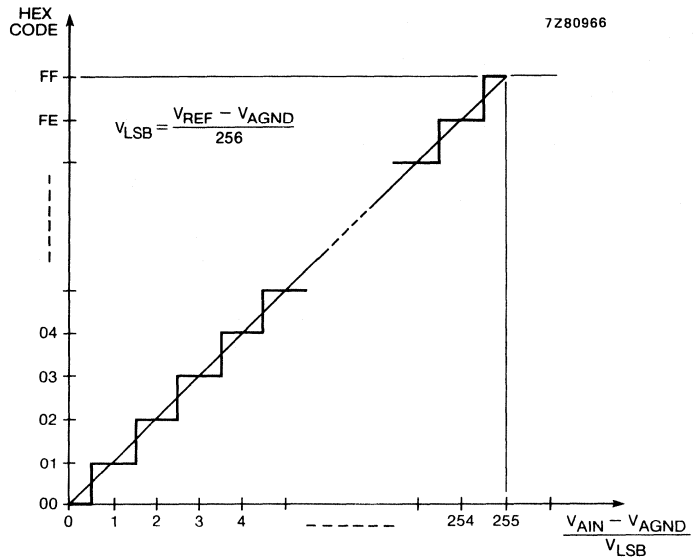


Fig. 9a A/D conversion characteristics of single-ended inputs.

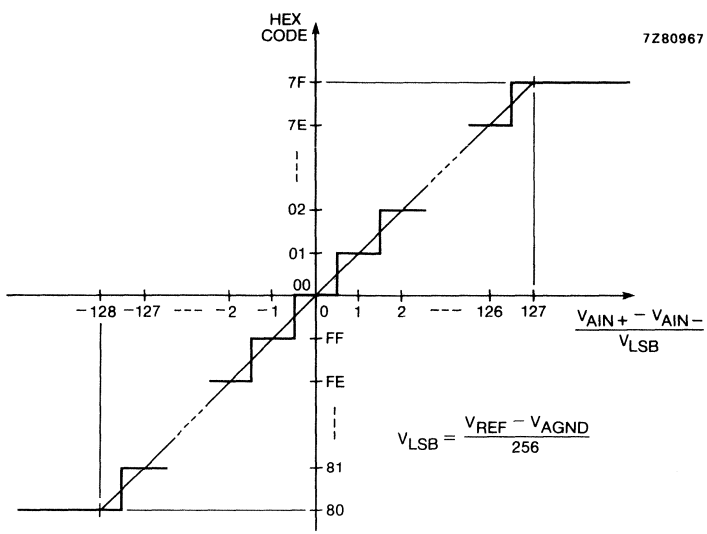


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

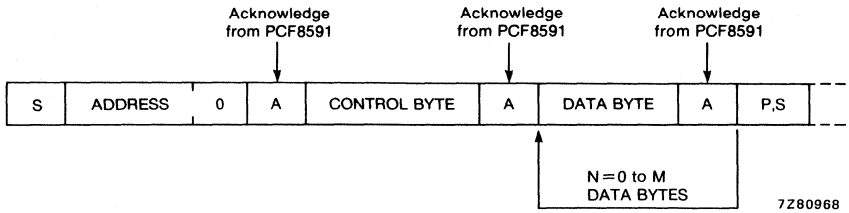


Fig. 10a Bus protocol for write mode, D/A conversion.

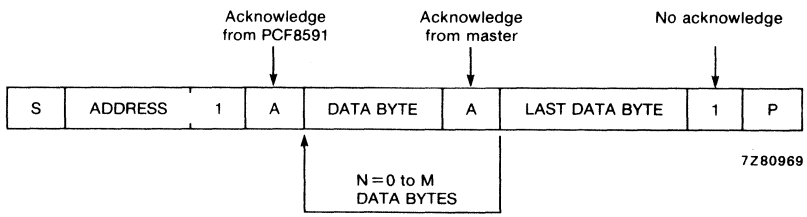


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

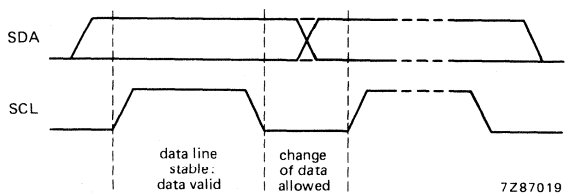


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

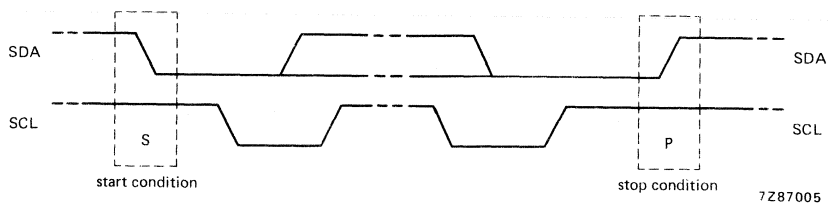


Fig. 12 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

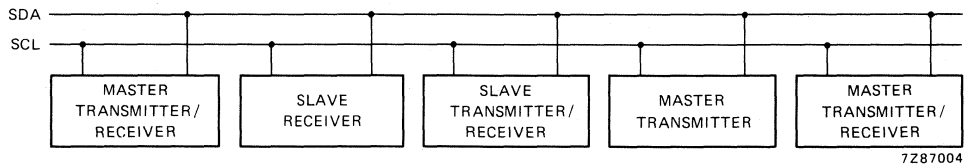


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

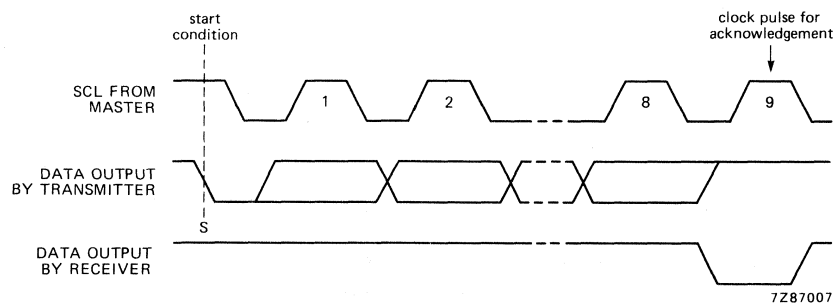


Fig. 14 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

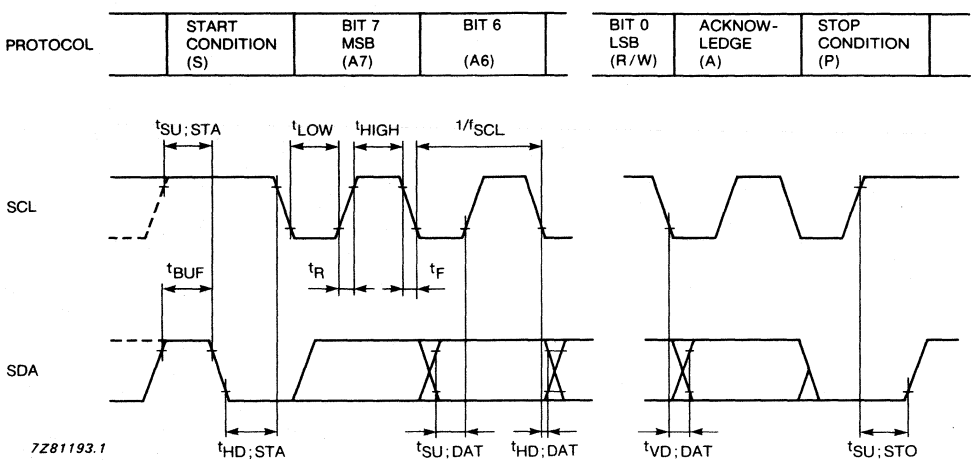


Fig. 15 I^2C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby $V_I = V_{SS}$ or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; $V_I = V_{SS}$ to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs	V_{REF}, AGND					
Voltage range	reference	V_{REF}	V_{AGND}	–	V_{DD}	V
Voltage range	analogue ground	V_{AGND}	V_{SS}	–	V_{REF}	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	0,9xV_{DD}	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

DEVELOPMENT DATA

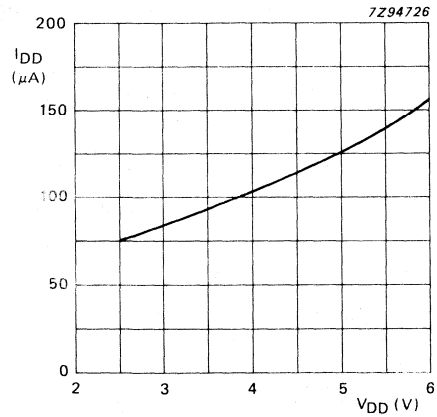
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

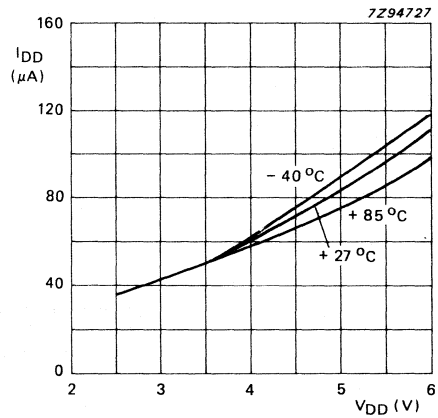
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; V_{DDN} = 0,1xV_{PP}	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.



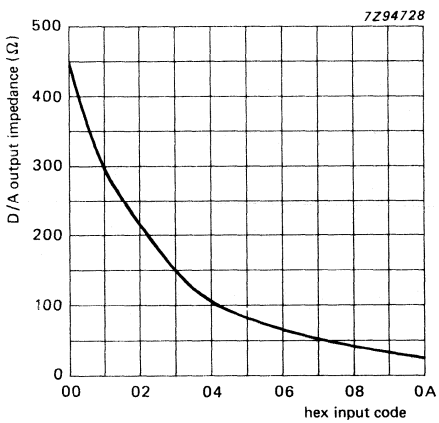
(a) internal oscillator; T_{amb} = + 27 °C.



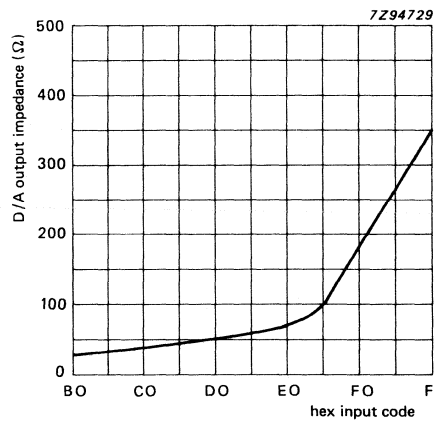
(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).

DEVELOPMENT DATA



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors ($> 10\ \mu F$) are recommended for power supply and reference voltage inputs.

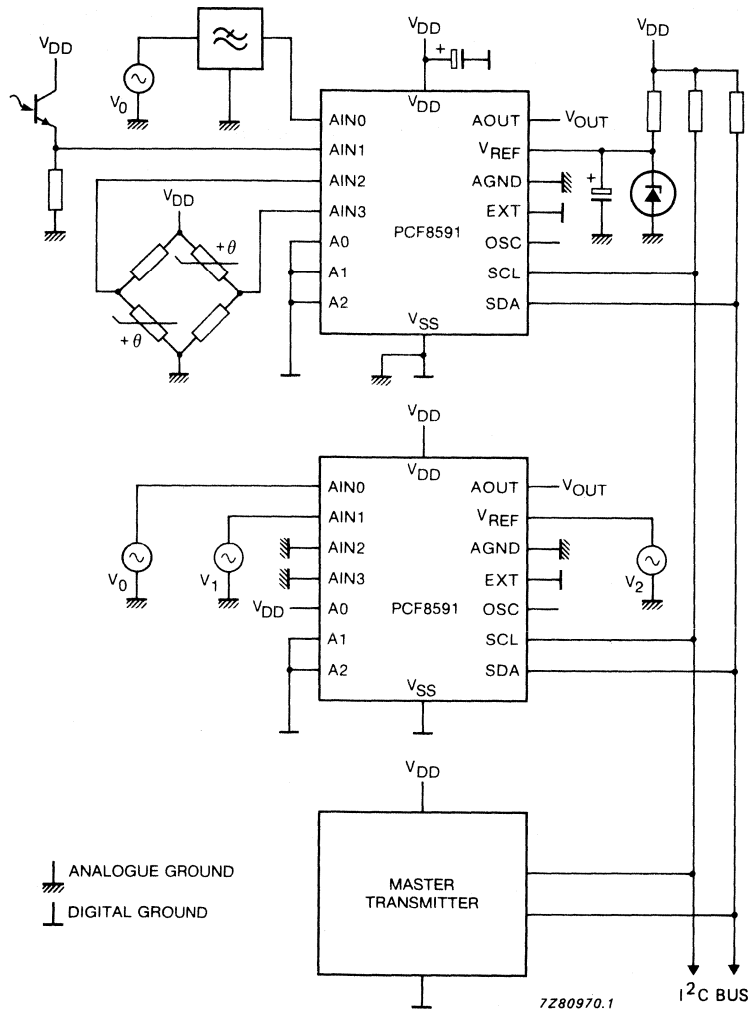


Fig. 18 Application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

7-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC 7)

GENERAL DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analogue-to-digital converter (ADC) designed for video applications. The device converts the analogue input signal into 7-bit binary coded digital words at a sampling rate of 22 MHz.

The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

- 7-bit resolution
- No external sample and hold required
- High input impedance
- Binary or two's complement 3-state TTL outputs
- Overflow and underflow 3-state TTL outputs
- All outputs positive-edge triggered
- Standard 24-pin package

Applications

- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

QUICK REFERENCE DATA

Measured over full voltage and temperature range unless otherwise specified

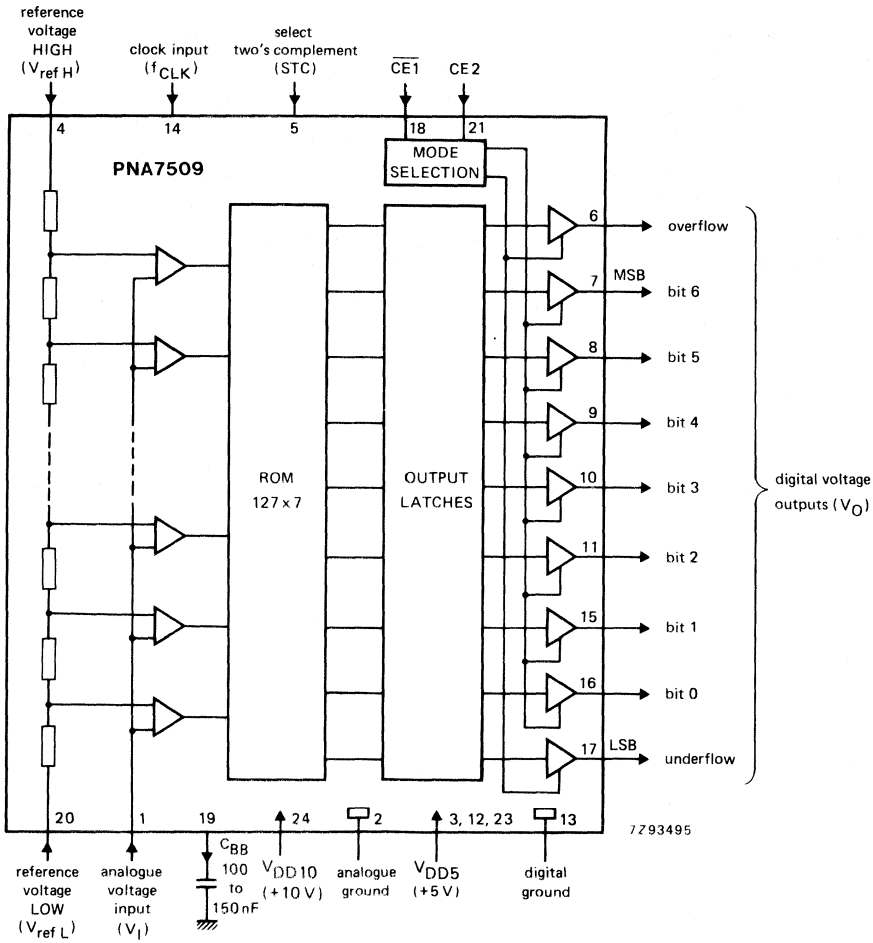
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pins 3, 12, 23)		V_{DD5}	4,5	–	5,5	V
Supply voltage (pin 24)		V_{DD10}	9,5	–	10,5	V
Supply current (pins 3, 12, 23)	note 1	I_{DD5}	–	–	65	mA
Supply current (pin 24)	note 1	I_{DD10}	–	–	13	mA
Reference current (pins 4, 20)		I_{ref}	150	–	450	μA
Reference voltage LOW (pin 20)		V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)		V_{refH}	5,0	5,1	5,2	V
Non-linearity	f_i = 1,1 kHz					
integral		INL	–	–	± ½	LSB
differential		DNL	–	–	± ½	LSB
–3 dB Bandwidth		B	11	–	–	MHz
Clock frequency (pin 14)		f_{CLK}	1	–	22	MHz
Total power dissipation	note 1	P_{tot}	–	–	500	mW

Note to quick reference data

1. Measured under nominal conditions: V_{DD5} = 5 V; V_{DD10} = 10 V; T_{amb} = 22 °C.

PACKAGE OUTLINES

24-lead DIL; plastic (SOT-101A).



Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Fig. 1 Block diagram.

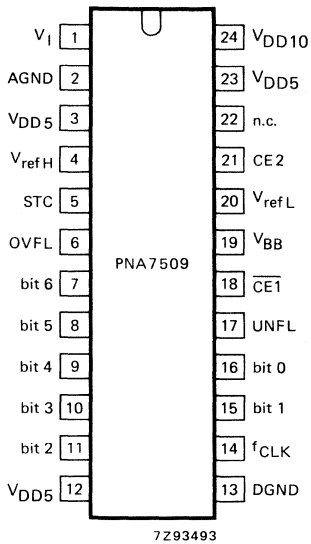


Fig. 2 Pinning diagram.

PINNING

1	V_I	analogue voltage input
2	AGND	analogue ground
3	V_{DD5}	positive supply voltage (+ 5 V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD5}	positive supply voltage (+ 5 V)
13	DGND	digital ground
14	f_{CLK}	clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	$\overline{CE1}$	chip enable input 1
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	CE 2	chip enable input 2
22	n.c.	not connected
23	V_{DD5}	positive supply voltage (+ 5 V)
24	V_{DD10}	positive supply voltage (+ 10 V)

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pins 3, 12, 23)	V_{DD5}	−0,5 to + 7	V
Supply voltage range (pin 24)	V_{DD10}	−0,5 to + 12	V
Input voltage range	V_I	−0,5 to + 7	V
Output current	I_O	5	mA
Total power dissipation	P_{tot}	1	W
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD5} = V_{3, 12, 23-13} = 4{,}5$ to 5,5 V; $V_{DD10} = V_{24-2} = 9{,}5$ to 10,5 V; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pins 3, 12, 23)	V_{DD5}	4,5	–	5,5	V
Supply voltage (pin 24)	V_{DD10}	9,5	–	10,5	V
Supply current (pins 3, 12, 23)	I_{DD5}	–	–	85	mA
Supply current (pin 24)	I_{DD10}	–	–	18	mA
Reference voltages					
Reference voltage LOW (pin 20)	V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)	V_{refH}	5,0	5,1	5,2	V
Reference current	I_{ref}	150	–	450	μA
Inputs					
Clock input (pin 14)					
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input voltage HIGH (note 1)	V_{IH}	3,0	–	V_{DD5}	V
Digital input levels (pins 5,18,21; note 2)					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD5}	V
Input current					
at $V_5 = 0$ V; V_{13} = GND	$-I_5$	15	–	70	μA
at $V_{18} = 5$ V; V_{13} = GND	I_{18}	15	–	70	μA
at $V_{21} = 0$ V; V_{13} = GND	$-I_{21}$	15	–	120	μA
Input leakage current (except pins 5, 18 and 21)	I_{LI}	–	–	10	μA
Analogue input levels (pin 1) at $V_{refL} = 2{,}5$ V; $V_{refH} = 5{,}1$ V					
Input voltage amplitude (peak-to-peak value)	$V_{I(p-p)}$	–	2,6	–	V
Input capacitance (note 3)	C_{1-2}	–	–	30	pF

Notes to characteristics

1. Maximum input voltage must not exceed 5,0 V.
2. If pin 5 is LOW binary coding is selected.
   If pin 5 is HIGH two's complement is selected.
   If pin 5, 18 and 21 are open-circuit, pin 5, 21 are HIGH and pin 18 is LOW.
   For output coding see Table 1 and mode selection see Table 2.
3. Tested on sample base.

parameter	symbol	min.	max.	unit
Outputs				
Digital voltage outputs (pins 6 to 11 and 15 to 17)				
Output voltage LOW at I_O = 2 mA	V_{OL}	0	+0,4	V
Output voltage HIGH at $-I_O$ = 0,5 mA	V_{OL}	2,4	V_{DD5}	V

Table 1 Output coding (V_{refL} = 2,50 V; V_{refH} = 5,08 V)

step	V_{1-2} (1)	UNFL	OVFL	binary bit 6 – bit 0	two's complement bit 6 – bit 0
underflow	< 2,51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
0	2,51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
1	2,53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
126	5,03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0
127	5,05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1
overflow	⩾ 5,07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1

steps 2-125

Note to Table 1

1. Approximate values.

Table 2 Mode selection

$\overline{CE\ 1}$	CE 2	bit 0 to bit 6	UNFL, OVFL
X	0	HIGH impedance	HIGH impedance
0	1	active	active
1	1	HIGH impedance	active

DEVELOPMENT DATA

CHARACTERISTICS (continued)

$V_{DD5} = V_{3, 12, 23-13} = 4{,}5$ V to 5,5 V; $V_{DD10} = V_{24-2} = 9{,}5$ V to 10,5 V; $V_{refL} = 2{,}5$ V; $V_{refH} = 5{,}1$ V; $f_{CLK} = 22$ MHz; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C

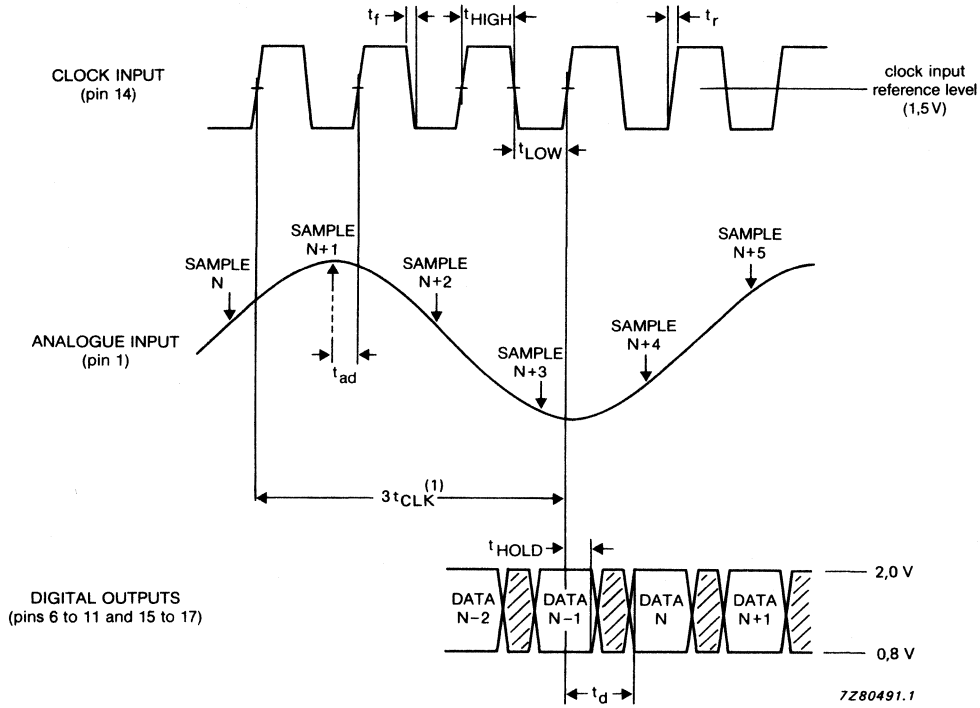
parameter	symbol	min.	max.	unit
Switching characteristics (see also Fig. 3)				
Clock input (pin 14)				
Clock frequency	f_{CLK}	1	22	MHz
Clock cycle time LOW	t_{LOW}	20	–	ns
Clock cycle time HIGH	t_{HIGH}	20	–	ns
Input rise and fall times (pin 1)				
rise time	t_r	–	3	ns
fall time	t_f	–	3	ns
Analogue input (note 1)				
Bandwidth (−3 dB)	B	11	–	MHz
Differential gain (note 2)	dG	–	± 5	%
Differential phase (note 2)	d_p	–	± 2,5	deg
Phase error (note 3)	P_e	–	± 12	deg
Non-harmonic noise		–	−36	dB
Peak error (non-harmonic noise)		–	3	LSB
Harmonics (full scale)				
fundamental	f_0	–	0	dB
r.m.s. (2nd + 3rd harmonic)	$f_{2,3}$	–	−28	dB
r.m.s. (4th + 5th + 6th + 7th harmonic)	f_{4-7}	–	−35	dB

parameter	symbol	min.	max.	unit
Digital outputs (notes 1 and 4)				
Output hold time	t_{HOLD}	6	—	ns
Output delay time at C_L = 15 pF	t_d	—	38	ns
Output delay time at C_L = 50 pF	t_d	—	48	ns
3-state delay time	t_{dt}	—	25	ns
Capacitive output load	C_{OL}	0	15	pF
Transfer function				
Non-linearity at f_i = 1,1 kHz				
integral	INL	—	± ½	LSB
differential	DNL	—	± ½	LSB

Notes to timing characteristics

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. Low frequency sinewave (peak-to-peak value of the analogue input voltage at $V_{I(p-p)}$ = 1,8 V) combined with a sinewave voltage ($V_{I(p-p)}$ = 0,7 V) at f_i = 5 MHz.
3. Sinewave voltage with increasing amplitude at f_i = 5 MHz (minimum amplitude $V_{I(p-p)}$ = 0,25 V; maximum amplitude $V_{I(p-p)}$ = 2,5 V).
4. The timing values of the digital outputs at pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1,5 V.

DEVELOPMENT DATA



(1) There is a delay of 3 clock cycles between sampling of an analogue input signal and the corresponding digital output.

Fig. 3 Timing diagram.

APPLICATION NOTE

The minimum and maximum values provided in the data sheet are guaranteed over the whole voltage and temperature range. This note gives additional information to the data sheet where the typical values indicate the behaviour under nominal conditions; $V_{DD5} = 5$ V, $V_{DD10} = 10$ V, $T_{amb} = 22\ ^{o}C$.

parameter	symbol	typ.	unit
Supply			
Supply current (pins 3, 12, 23)	I_{DD5}	51	mA
Supply current (pin 24)	I_{DD10}	11	mA
Maximum clock frequency	f_{CLK}	25	MHz
Bandwidth (−3 dB)	B	20	MHz
Total power dissipation	P_{tot}	365	mW
Peak error (non-harmonic noise)		1,5	LSB
Suppression of harmonics sum of:			
$f_{2nd} + f_{3rd}$		31	dB
$f_{4th} + f_{5th} + f_{6th} + f_{7th}$		39	dB
Non-linearity			
integral	INL	± 1/4	LSB
differential	DNL	± 1/3	LSB
Differential gain	dG	± 3	%
Differential phase	dP	± 1	%
Large signal phase error	P_e	10	deg
Non-harmonic noise		40	dB

Typical values are measured on sample base.

Application recommendation

Spikes at the 10 V supply input must be avoided (e. g. overshoots during switching).
Even a spike duration of less than 1 μs can destroy the device.

DEVELOPMENT DATA

APPLICATION NOTE (continued)

Test philosophy

Fig. 4 is a block diagram showing analogue-to-digital testing with a phase locked signal source. The signal generator provides a 5 MHz sinewave for the device under test (except for the linearity test). The 22 MHz clock input is provided by the clock generator. The phase relationship between signal and clock generator is shifted by 100 pico sec. each signal period to provide an effective clock rate of 10 GHz for analysis.
Most calculations are carried out in the spectral domain using Fast Fourier Transformation (FFT) and the inverse FFT to return to time domain.
The successive processing completes the specific measurement (Fig. 5, 6, 7 and 8).

The non-linearities of the converter, integral (INL) and differential (DNL), are measured using a low frequency ramp signal. Within a general uncertain range of conversion between two steps the output signal of the converter randomly switches.
After low-pass filtering the different step width is used for calculating the line of least squares to obtain integral non-linearity.
To calculate differential non-linearity a counter is used to count the frequency of each step. A histogram is calculated from the counter result to provide the basis for further computation (Fig. 7).

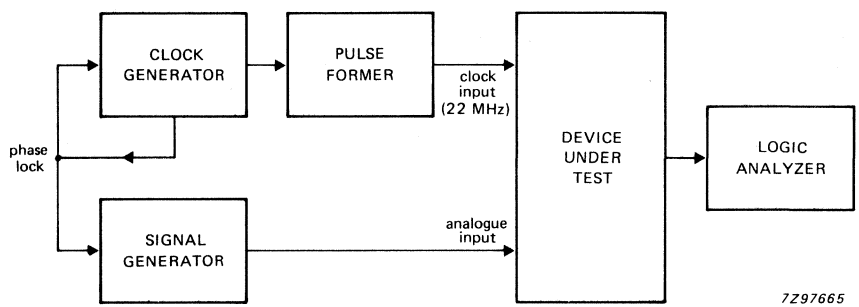
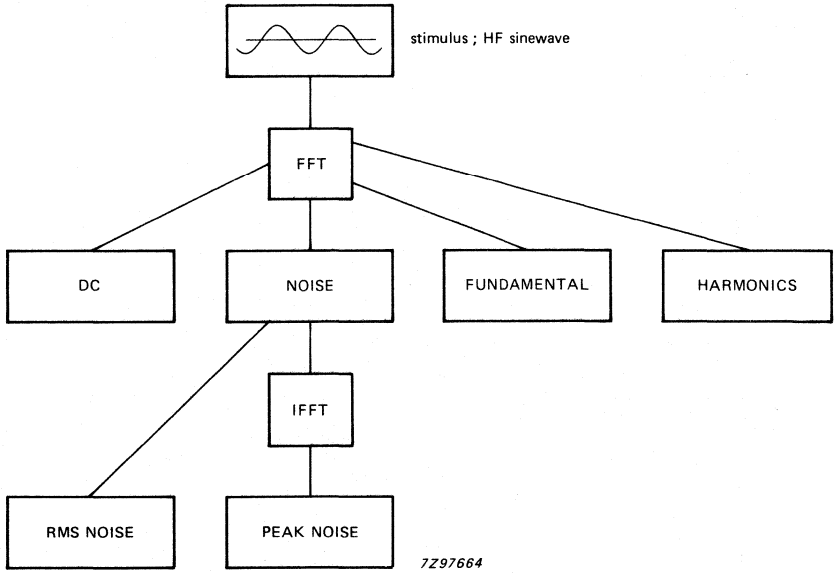


Fig. 4 Analogue-to-digital converter testing with locked signal source.



Where: FFT = Fast Fourier Transformation.
IFFT = Inverse Fast Fourier Transformation.

Fig. 5 Sinewave test; non-harmonic noise and peak error.

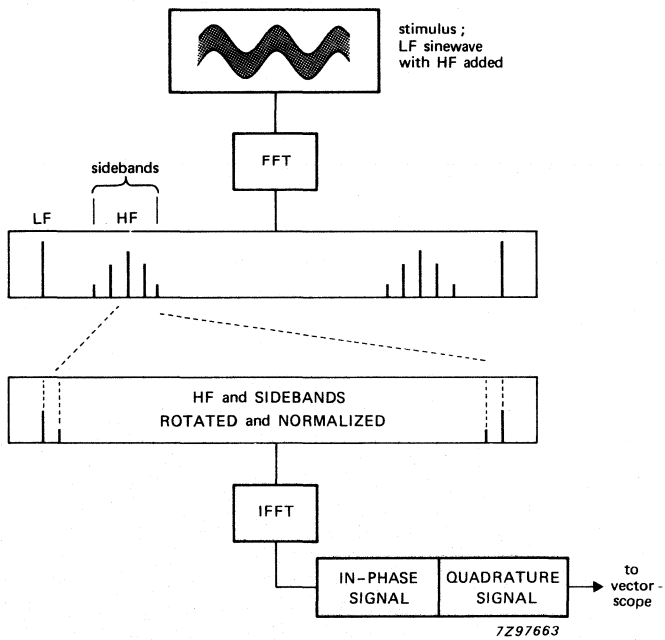
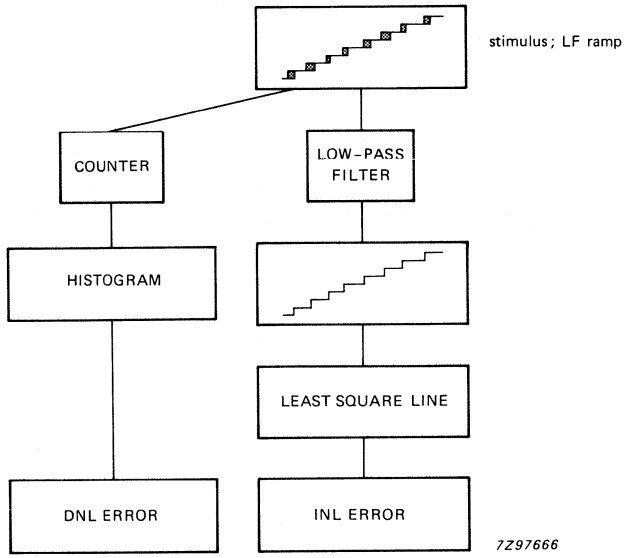


Fig. 6 Differential gain and phase.

APPLICATION NOTE (continued)



Where: INL = Integral Non-Linearity.
DNL = Differential Non-Linearity.

Fig. 7 Low frequency ramp test; linearity.

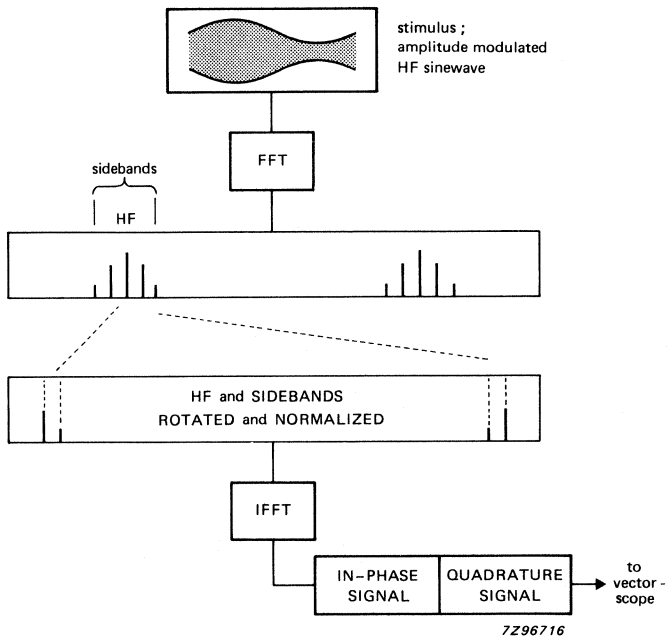


Fig. 8 Large signal phase error.

8-BIT MULTIPLYING DAC

GENERAL DESCRIPTION

The PNA7518 is a NMOS 8-bit multiplying digital-to-analogue converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analogue output at a sampling rate of 30 MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analogue signal from a resistor chain. Two external reference voltages supply the resistor chain. The multiplying capability is obtained by using the independent reference voltages.

The input latches are positive-edge triggered. The output impedance is approximately 0,5 kΩ depending on the applied digital code. An additional operational amplifier is required for the 75 Ω output impedance. Two's complement is selected when STC (pin 11) is HIGH or is not connected. STC inverts the most significant bit (MSB).

Features

- TTL input levels
- Positive-edge triggered
- Analogue voltage output at 30 MHz sampling rate
- Binary or two's complement input
- Output voltage accuracy to within ± ½ of the input LSB
- Multiplying capability
- 12 MHz bandwidth
- 8-bit resolution

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	4,5	–	5,5	V
Supply current		I_{DD}	–	–	80	mA
Reference voltage LOW		V_{refL}	0	–	2,0	V
Reference voltage HIGH		V_{refH}	0	–	2,0	V
Static non-linearity	note 1		–	–	± 0,5	LSB
Bandwidth at –3 dB	note 2	B	12	–	–	MHz
Clock frequency	T_{amb} = 25 °C; V_{DD} = 5 V	f_{CLK}	10	–	30	MHz
Total power consumption		P	–	–	470	mW

For explanation of notes see "Notes to the characteristics".

Applications

- Video data conversion
- CRT displays
- Waveform/test signal generation
- Colour/black-and-white graphics

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38D).

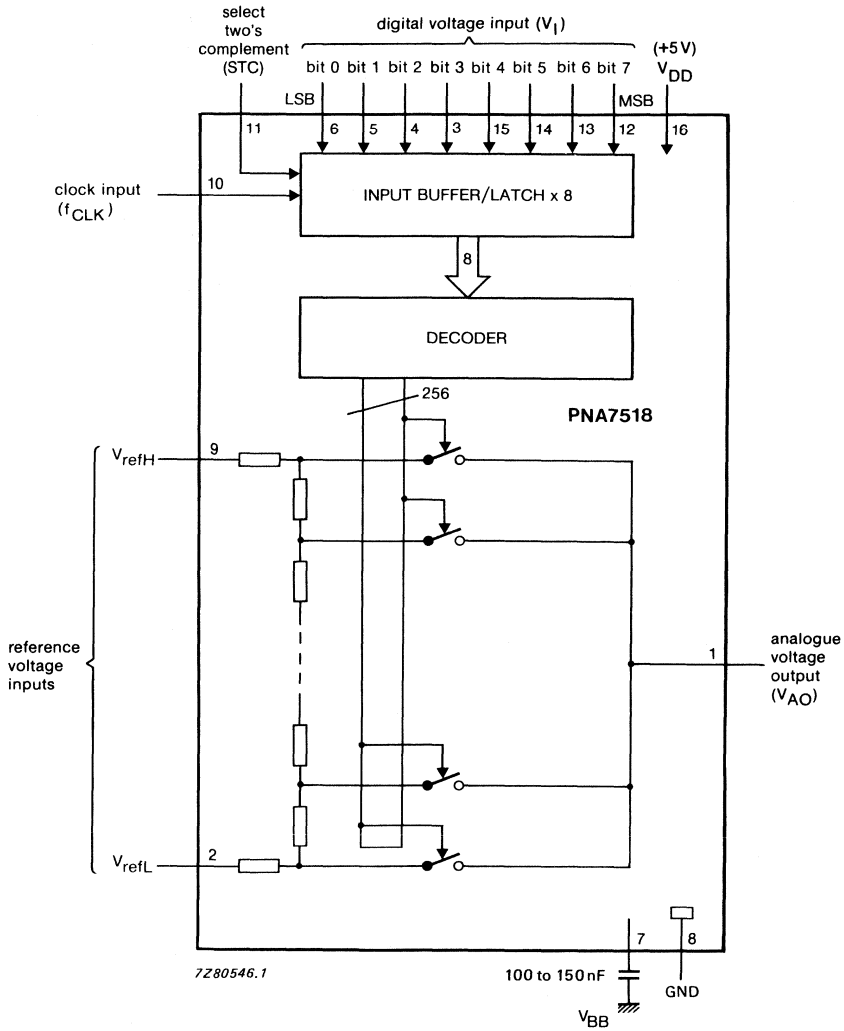


Fig. 1 Block diagram.

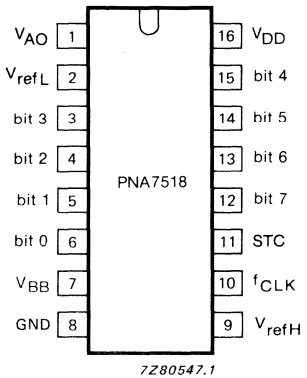


Fig. 2 Pinning diagram.

PINNING

1	V_{AO}	analogue output voltage
2	V_{refL}	reference voltage LOW
3	bit 3	digital voltage inputs (V_I)
4	bit 2	
5	bit 1	
6	bit 0	least-significant bit (LSB)
7	V_{BB}	back bias
8	GND	ground
9	V_{refH}	reference voltage HIGH
10	f_{CLK}	clock input
11	STC	select two's complement
12	bit 7	most-significant bit (MSB)
13	bit 6	digital voltage inputs (V_I)
14	bit 5	
15	bit 4	
16	V_{DD}	positive supply voltage

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,5	7,0	V
Input voltage B0 to B7 and STC	V_I	−0,5	7,0	V
Output voltage	V_{AO}	−0,5	7,0	V
Total power dissipation	P_{tot}	−	800	mW
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Temperature range with back bias	T_{BB}	−10	+ 80	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; C_{BB} = 100 nF; T_{amb} = 0 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4,5	–	5,5	V
Supply current		I_{DD}	–	–	80	mA
Inputs B0 to B7, CLK, and STC						
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2	–	V_{DD}	V
Input leakage current (except STC)		I_{LI}	–	–	10	μA
STC input leakage current		I_{LI}	–	–	100	μA
Reference voltages						
Reference voltage LOW		V_{refL}	0	–	2	V
Reference voltage HIGH		V_{refH}	0	–	2	V
Reference ladder between V_{refL} and V_{refH}		R_{ref}	150	–	300	Ω
Linearity						
Static non-linearity	note 1		–	–	± 0,5	LSB
Clock input						
Clock frequency	T_{amb} = 25 °C; V_{DD} = 5 V	f_{CLK}	10	–	30	MHz
Bandwidth						
Bandwidth at −3 dB	note 2	B	12	–	–	MHz

Notes to the characteristics

1. Measured at R_{AO} = 200 kΩ; V_{refL} = 0 V; V_{refH} = 2 V and f_{CLK} = 28 MHz.
2. Measured at V_{DD} = 5 V; T_{amb} = 25 °C; V_{refL} = 0 V; V_{refH} = 2 V; f_{CLK} = 30 MHz; duty cycle = 0,5; rise and fall time = 3 ns and a 6 pF load at the analogue output. The analogue output signal is scanned by an external sample and hold circuit.

APPLICATION INFORMATION

This section provides additional information to the characteristics. The values are measured on a sampling basis.

Table 1 Application characteristics

parameter	symbol	typ.	unit
Supply current	I_{DD}	50	mA
Power consumption	P	270	mW
Minimum clock frequency	f_{CLK}	10	kHz
Maximum clock frequency	f_{CLK}	45	MHz
Static non-linearity		± 0,25	LSB
Reference ladder	R_{ref}	210	Ω
Bandwidth	B	15	MHz
Set-up time	t_{SU}	3	ns
Input hold time	t_{HD}	4	ns
Propagation delay	t_{PD}	$1 \times t_{CLK} + 30$	ns

Where:

$V_{DD} = 5$ V; $T_{amb} = 25$ °C; $V_{refL} = 0$ V; $V_{refH} = 2{,}0$ V.

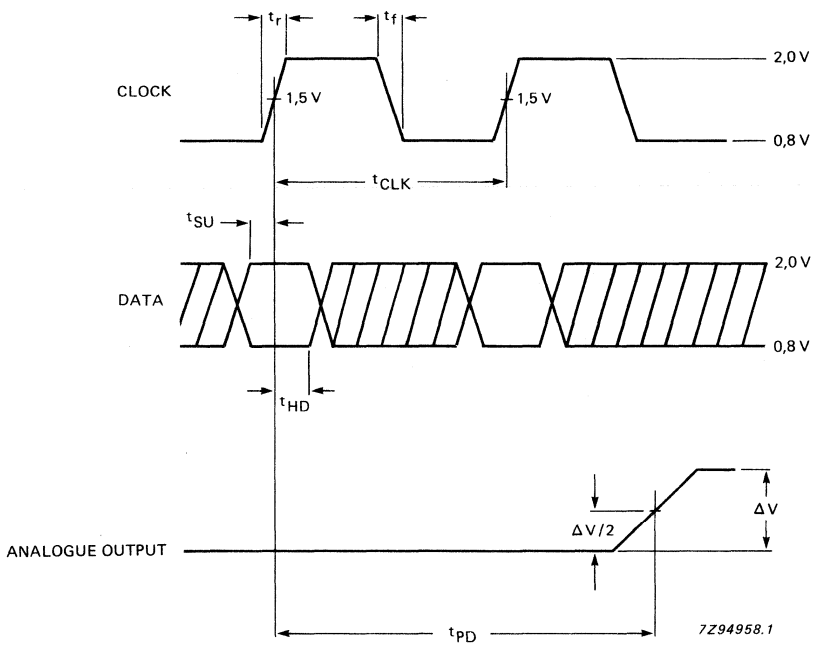


Fig. 3 Switching characteristics.

DEVELOPMENT DATA

UNIVERSAL SYNC GENERATOR

GENERAL DESCRIPTION

The SAA1043 generates the synchronizing waveforms required in all types of video source equipment (video cameras, film-scanners, video games, computer displays and similar applications). The device is programmable to suit standards SECAM 1, SECAM 2, PAL/CCIR, NTSC 1, NTSC 2, and PAL-M; the video game 624 and 524-line standards; and can be synchronized to an external sync signal. Inputs and outputs are CMOS compatible.

Features

- Programmable to eight standards
- Horizontal frequency manipulation for application in non-standard systems
- Oscillator functions with LC or crystal elements
- Additional outputs to simplify camera signal processing
- Can be synchronized to an external sync signal
- Vertical reset for fast vertical lock
- Subcarrier lock in combination with subcarrier coupler SAA1044
- Very low power consumption

QUICK REFERENCE DATA

Supply voltage range (pin 28)	V_{DD}	5,7 to 7,5	V
Supply current (quiescent)	I_{DD}	max. 10	μA
Oscillator frequency	f_{OSCI}	max. 5,1	MHz

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

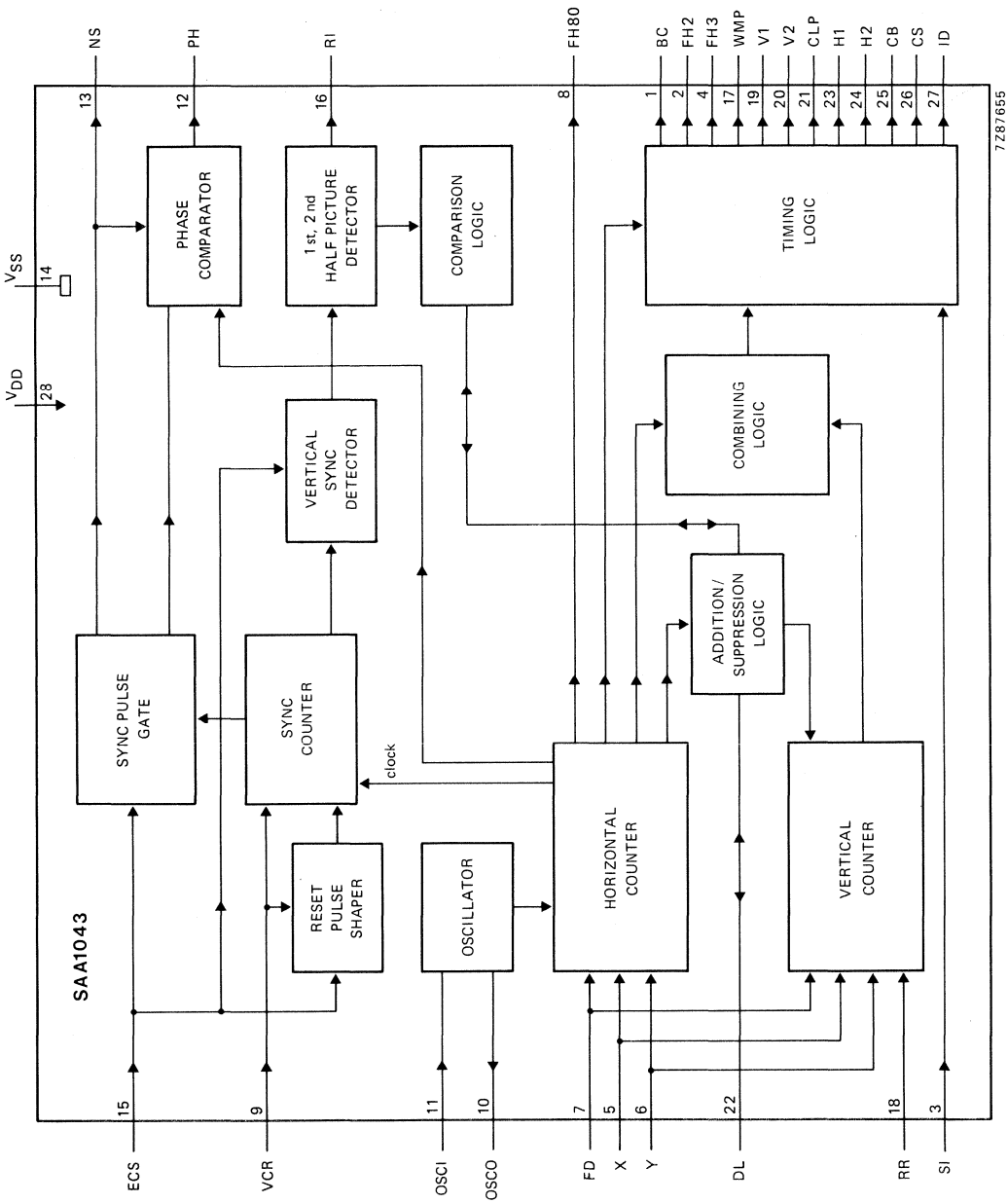


Fig. 1 Block diagram.

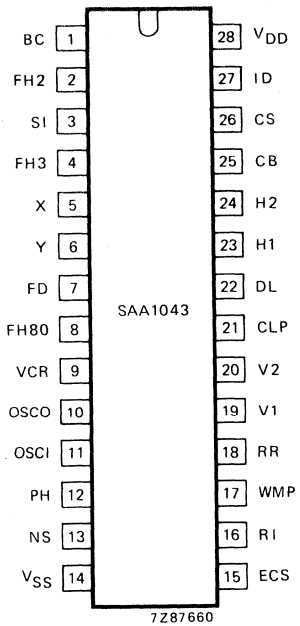


Fig. 2 Pinning diagram.

PINNING

1	BC	burst flag/chroma blanking (SECAM) output
2	FH2	PAL identification output
3	SI	set identification input (SECAM, PAL, PAL-M)
4	FH3	400 Hz (PAL); 360 HZ (NTSC, PAL-M) and $f_H/3$ (SECAM)
5	X	standard programming input
6	Y	standard programming input
7	FD	standard programming input
8	FH80	80 x f_H output (1,25 MHz)
9	VCR	VCR standard input
10	OSCO	oscillator output
11	OSCI	oscillator input
12	PH	phase detector output
13	NS	no-sync detector output
14	V_{SS}	negative supply voltage (ground)
15	ECS	external composite sync input
16	RI	vertical identification output
17	WMP	white measurement pulse output
18	RR	vertical reset input
19	V1	vertical drive output
20	V2	vertical drive output
21	CLP	clamp pulse output
22	DL	2 x f_H input/output
23	H1	horizontal drive output
24	H2	horizontal drive output
25	CB	composite blanking output
26	CS	composite sync output
27	ID	SECAM identification output
28	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Sync pulse generation

Programming of operating standard

The standard required for operation is programmed using the inputs X, Y and FD as shown in Table 1. The FD input selects 525 or 625-line working of the vertical counter (524 or 624-lines for video game standards) and also influences the choice of oscillator frequency as shown in Table 2.

Table 1 Programming of operating standard

standard	FD	X	Y
SECAM 1	0	0	0
SECAM 2	0	0	1
624	0	1	0
PAL/CCIR	0	1	1
NTSC 1	1	0	0
NTSC 2	1	0	1
524	1	1	0
PAL-M	1	1	1

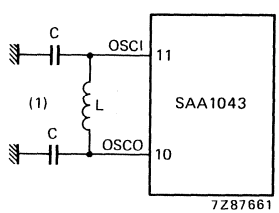
positive logic: 1 = HIGH; 0 = LOW

Oscillator

The built-in oscillator of the SAA1043 functions with an external LC-circuit (Fig. 3) or with a crystal of the parallel resonance type (Fig. 4). For operation in the VCR mode the LC oscillator circuit is recommended. The frequencies required for the operating standards are shown in Table 2.

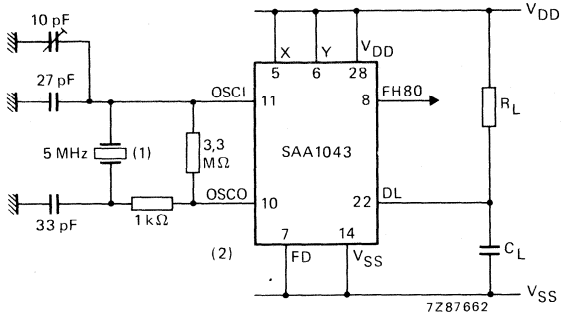
Table 2 Oscillator input frequencies

operating standard	osc. frequency (f_{OSCI}) MHz	vertical divider (FD)	vertical frequency (f_V) Hz	horizontal frequency (f_H) Hz
PAL, SECAM, 624	5,0	0	50	15625
NTSC, PAL-M, 524	5,034964	1	59,94	15734,26
PAL, SECAM, 624	2,5	H2 (pin 24)	50	15625
NTSC, PAL-M, 524	2,51748	H1 (pin 23)	59,94	15734,26



(1) Component values can be calculated from the formula $f_{OSCI} = 1/2\pi\sqrt{LC_v}$ where $C_v = C/2 + C_p$ and C_p = parasitic capacitance of typically 5 pF.

Fig. 3 LC oscillator circuit.



(1) Catalogue number of crystal: 8222 298 40760.

(2) All inputs not shown are at V_{SS}.

Fig. 4 Crystal oscillator circuit showing test set-up for oscillator frequency measurement.

Synchronization to an external sync signal

Use is made of the phase comparator output PH to lock the internally generated sync pulses to an external sync signal. Reset pulses derived at each falling edge of the external sync signal (ECS) reset the the sync counter which is clocked at the internal horizontal frequency by the horizontal counter. At each horizontal scan period the sync counter opens the sync pulse gate and allows the ECS to be applied to the phase comparator where it is compared with the phase of the internally generated horizontal sync pulse. When the two signals are in phase the output PH is in a high impedance state. When a phase difference exists PH is pulled towards V_{DD} or V_{SS} depending on the direction of the error (Fig. 5). The phase-analogue voltage on PH is used to correct the frequency at OSCI via a voltage-controlled oscillator and null the phase error between internal and external signals. Pulses occurring on the ECS outside of the sync pulse gating time (serration and equalization pulses) do not effect the phase comparator.

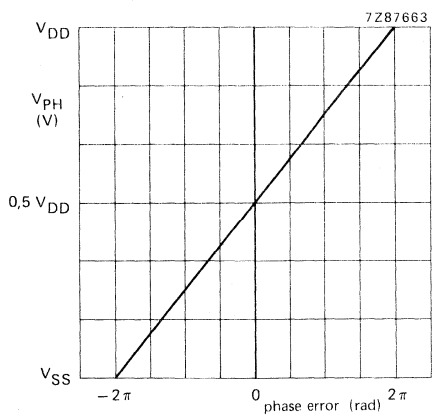


Fig. 5 Phase comparator characteristic.

FUNCTIONAL DESCRIPTION (continued)

Synchronization to an external sync signal (continued)

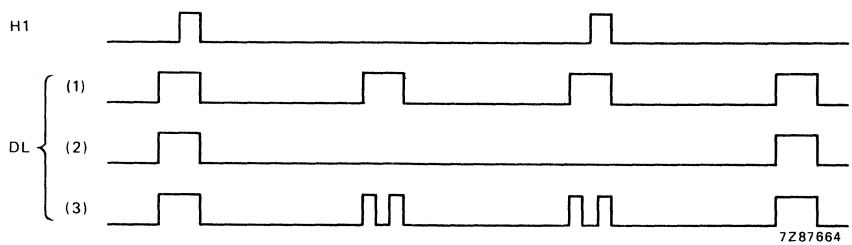
The circuit will lock to standard and non-standard sync signals. With standard signals the resetting of the sync counter is permitted after 3/4 of the horizontal scan period and if one reset pulse is missed the next pulse will reset the counter. With non-standard signals a narrow reset window is imposed to avoid disturbances which would otherwise be visible on the screen during vertical blanking time. The width of this window is $64 - 15{,}2 <$ reset time $< 64 + 15{,}2$ μs. If a reset pulse does not occur within this window the same window timing is specified for the next horizontal scan.

A no-sync signal is generated by the sync pulse gate if the sync counter is not reset from the ECS. The no-sync signal (NS) occurs 6,4 μs after the time of the missing reset pulse.

Detection of the vertical sync in the ECS is performed using a double sampling method which minimizes detection failures. Vertical lock is performed by comparing the internal vertical sync with a pulse derived from the ECS and using the result to modify the period of the vertical counter. This is achieved by manipulating the DL ($2 \times f_H$) input to the vertical counter via the addition/subtraction logic. The DL pulses are added or suppressed to bring the circuit into lock in the shortest possible time; the direction taken is determined by a logic decision based on the half picture in which the ECS derived pulse occurred.

Use in non-standard systems

For systems requiring a non-standard horizontal frequency the number of horizontal scans per picture can be manipulated using the open drain input/output DL. The addition or suppression of pulses during the high ohmic period of DL modifies the vertical counter value. The suppression of two DL pulses per half picture will give one extra horizontal scan and the addition of two DL pulses will remove one horizontal scan from the half picture (see Fig. 6).



(1) Normal waveform at DL; $f_{DL} = 2 \times f_H$.

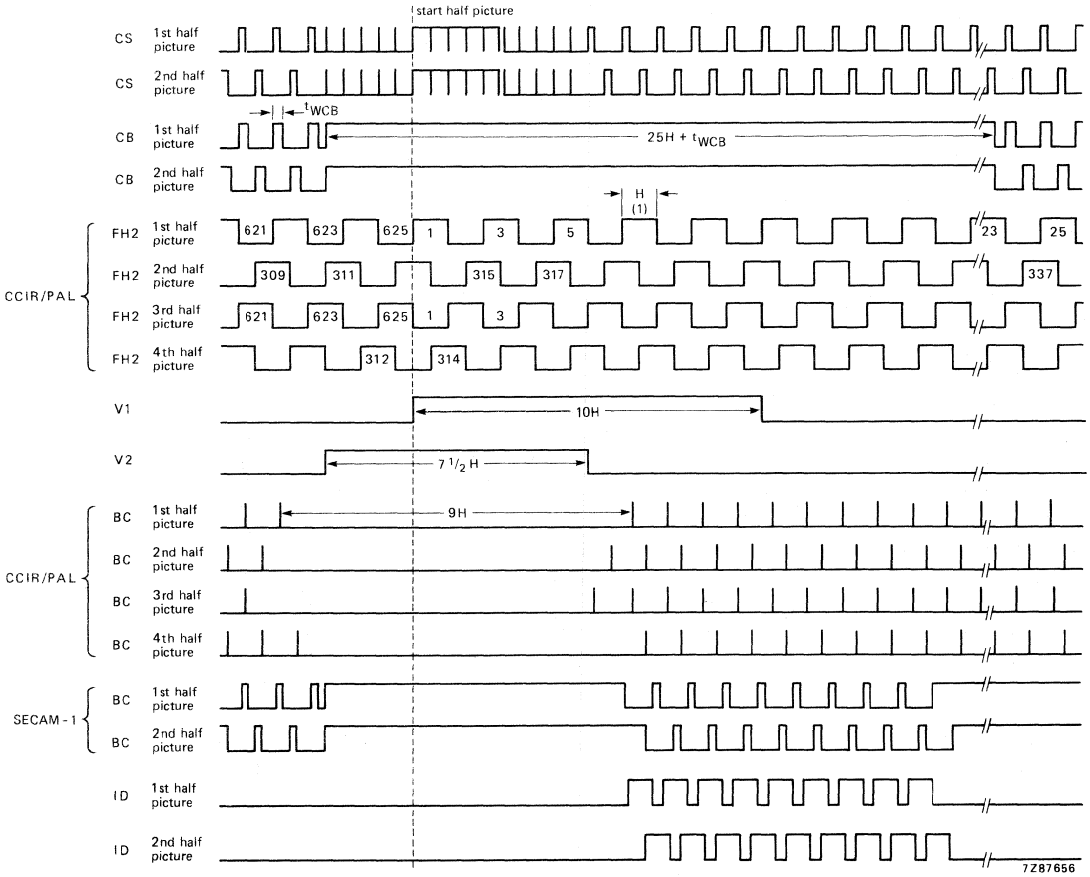
(2) Waveform at DL with two pulses suppressed increases the number of horizontal scans per half picture by 1.

(3) Waveform at DL with two additional pulses decreases the number of horizontal scans per half picture by 1.

Fig. 6 Manipulation of the horizontal frequency for non-standard systems.

Output waveforms

The output waveforms for the different modes of operation are shown in Figs 7 and 8.

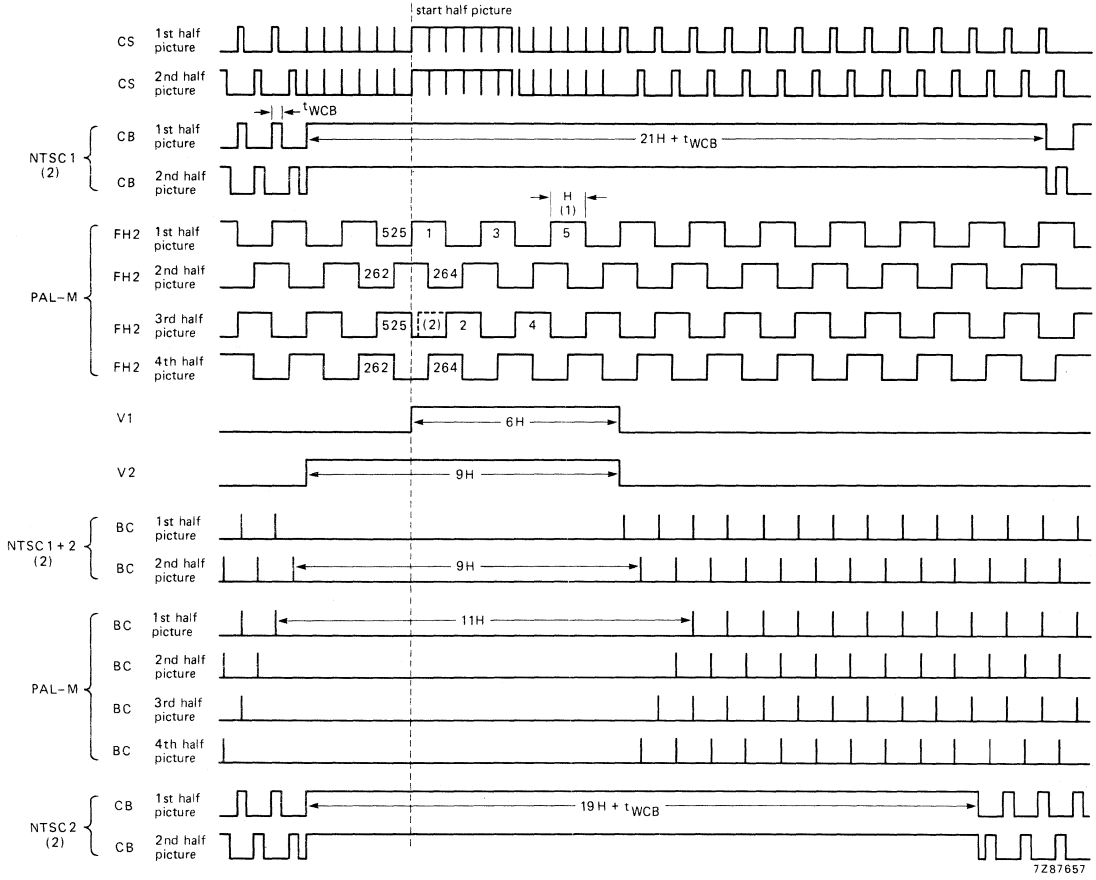


(1) H = 1 horizontal scan.

Fig. 7 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the 1st half picture of PAL/CCIR and are not interlaced (0,5H subtracted from the waveform timing).

FUNCTIONAL DESCRIPTION (continued)

Output waveforms (continued)



(1) H = 1 horizontal scan.

(2) NTSC mode reset; the 4th half picture is identical to the 2nd half picture for NTSC.

Fig. 8 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the 1st half picture of NTSC and are not interlaced (0,5H subtracted from the waveform timing).

WAVEFORM TIMING (Table 3, Figs 9 and 10)

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is shown in Table 3 as the number (n) of oscillations at OSCI. The timings given are derived from n x t_{OSCI} ± 100 ns. One horizontal scan (H) = 320 x t_{OSCI} = $1/f_H$. Note that the number of horizontal scans per half picture can be modified for non-standard systems using input/output DL as shown in Fig. 6.

Table 3 Waveform timing

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
CS							
Horizontal sync pulse width	t_{WSC1}	4,8	4,77	4,77	4,8	µs	24
Equalizing pulse width	t_{WSC2}	2,4	2,38	2,38	2,4	µs	8
Serration pulse width	t_{WSC3}	4,8	4,77	4,77	4,8	µs	24
Duration of pre-equalizing pulses	–	2,5	3	3	2,5	H	
Duration of post-equalizing pulses	–	2,5	3	3	2,5	H	
Duration of serration pulses	–	2,5	3	3,5	2,5	H	
CB							
Horizontal blanking pulse width							
PAL/SECAM/PAL-M	t_{WCB}	12	–	11,12	12	µs	60
NTSC 1	t_{WCB}	–	11,12	–	–	µs	56
NTSC 2	t_{WCB}	–	10,53*	–	–	µs	53
Front porch	t_{PCBCS}	1,6	1,59	1,59	1,6	µs	8
Duration of vertical blanking							
PAL/SECAM/PAL-M		25H+t_{WCB}	–	21H+t_{WCB}	25H+t_{WCB}		
NTSC 1		–	21H+t_{WCB}	–	–		
NTSC 2		–	19H+t_{WCB}	–	–		
BC (PAL)							
Burst key pulse width	t_{WBC}	2,4	2,38	2,38	–	µs	12
Sync to burst delay	t_{PCSBC}	5,6	5,56	5,76	–	µs	28
Burst suppression	–	9	9	11	–	H	
Position of burst suppression: 1st half picture	–	H623 to H6	H523 to H6	H523 to H8	–	–	
2nd half picture	–	H310 to H318	H261 to H269	H260 to H270	–	–	
3rd half picture	–	H622 to H5	H523 to H6	H522 to H7	–	–	
4th half picture	–	H311 to H319	H261 to H269	H259 to H269	–	–	

WAVEFORM TIMING (continued)

Table 3 (continued)

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
BC (SECAM)							
Chroma pulse width	t_{WBC}	–	–	–	7,2	µs	36
Chroma to sync delay	t_{PBCCS}	–	–	–	1,6	µs	8
Duration of vertical blanking: SECAM 1	1st half picture: 25H + t_{WBC} except H320 to H328 2nd half picture: 24,5H + t_{WBC} except H7 to H15						
SECAM 2	1st half picture: 25H + t_{WBC} 2nd half picture: 24,5H + t_{WBC}						
CLP							
Clamp pulse width	t_{WCLP}	2,4	2,38	2,38	2,4	µs	12
Sync to clamp delay	t_{PCSCLP}	2,4	2,38	2,38	2,4	µs	12
DL							
Frequency	f_{DL}	2 x f_H	2 x f_H	2 x f_H	2 x f_H	–	
Pulse width	t_{WDL}	9,6	9,53	9,53	9,6	µs	48
DL to sync delay	t_{PCLCS}	5,6	5,56	5,56	5,6	µs	28
FH80							
Frequency	f_{FH80}	80 x f_H	80 x f_H	80 x f_H	80 x f_H	–	
Sync to FH80 delay	–	0,2	0,2	0,2	0,2	µs	1
H1, H2							
H1 pulse width	t_{WH1}	7,2	7,15	7,15	7,2	µs	36
H2 pulse width	t_{WH2}	7,2	7,15	7,15	7,2	µs	36
H1 to sync delay	t_{PH1CS}	0,8	0,79	0,79	0,8	µs	4
Sync to H2 delay	t_{PCSH2}	0,8	0,79	0,79	0,8	µs	4
Repetition period	–	64	63,56	63,56	64	µs	
V1, V2							
V1 duration	–	10	6	6	10	H	
V2 duration	–	7,5	9	9	7,5	H	
V1 to sync delay	t_{PV1CS}	1,6	1,59	1,59	1,6	µs	8
Sync to V2 delay	t_{PV2CS}	1,6	1,59	1,59	1,6	µs	8
FH2							
Frequency	f_{FH2}	$f_H/2$	$f_H/2$	$f_H/2$	$f_H/2$	–	
Sync to FH2 delay	–	0	0	0	0	µs	
FH3							
Frequency	f_{FH3}	400	360	360	$f_H/3$	–	
Sync to FH3 delay	–	–	–	–	0	µs	

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
WMP							
WMP pulse width	–	2,4	2,38	2,38	2,4	μs	12
Sync to WMP delay	–	34,4	34,16	34,16	34,4	μs	172
Duration of WMP	–	10	9	9	10	H	
Position of WMP							
1st half picture:	–	H163 to H173	H134 to H143	H134 to H143	H163 to H173	– –	
2nd half picture:	–	H475 to H485	H396 to H405	H396 to H405	H475 to H485	– –	
RI							
Frequency	–	$f_V/2$	$f_V/2$	$f_V/2$	$10f_H$	–	
Position of edges	–	H6 and H318	H7 and H269	H7 and H269	–	–	
ID							
ID pulse width	t_{WID}	12,0	11,12	11,12	12,0	μs	60
ID to sync delay	t_{PIDCS}	1,6	1,59	1,59	1,6	μs	8
Position of ID							
1st half picture:	–	H7 to H15	H8 to H22	H8 to H22	H7 to H15	–	
2nd half picture:	–	H320 to H328	H271 to H285	H271 to H285	H320 to H328	– –	

* Horizontal blanking pulse width for NTSC 2 can be 11, 12 μs maximum.

WAVEFORM TIMING (continued)

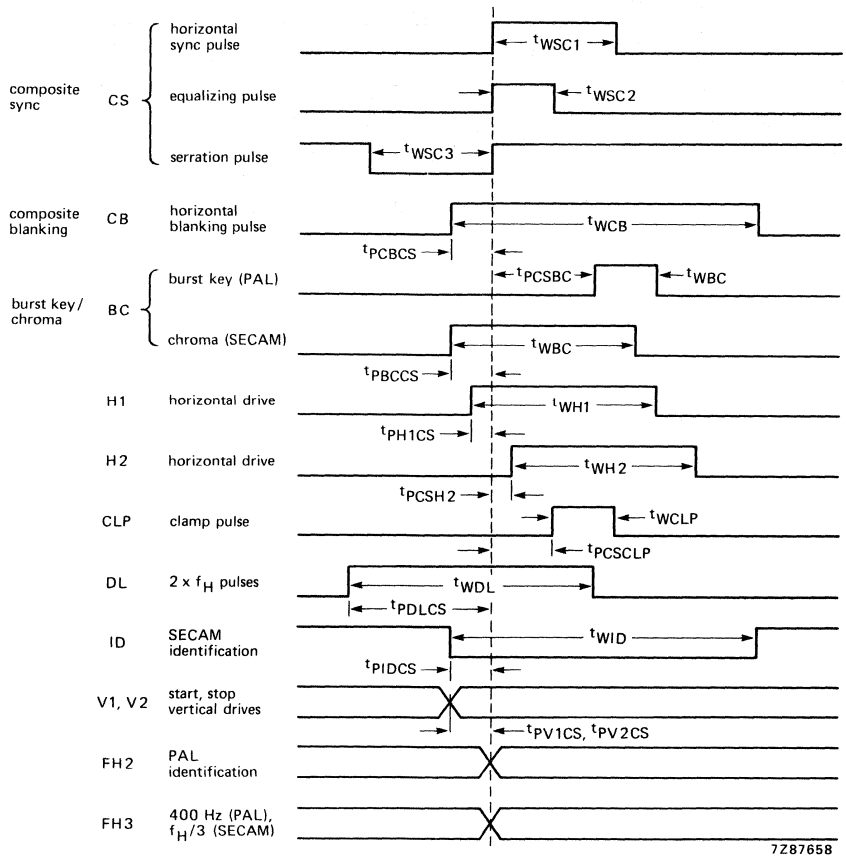


Fig. 9 Waveform timings: PAL/CCIR; SECAM; 624-line modes.

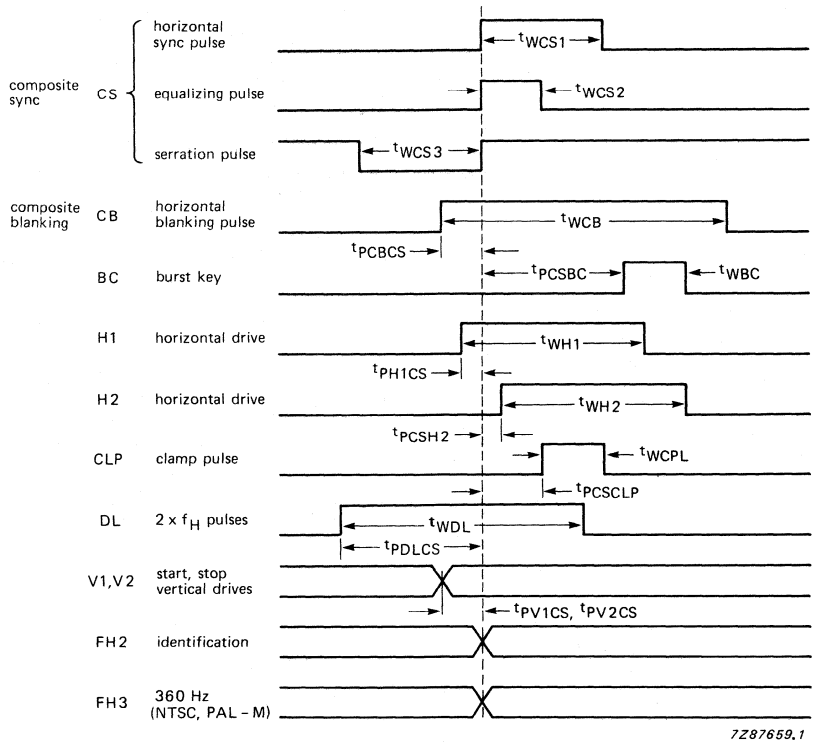


Fig. 10 Waveform timings: NTSC; PAL-M; 524-line modes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to + 15	V
Input voltage range	V_I	−0,5 to (V_{DD} + 0,5)*	V
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)*	V
Output current	$\pm I_O$	max. 10	mA
Power dissipation per output	P_O	max. 100	mW
Total power dissipation per package	P_{tot}	max. 200	mW
Operating ambient temperature range	T_{amb}	−25 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 150	°C

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5,7 to 7,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5,7	–	7,5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °V	I_{IR}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{IR}$	–	–	1	μA
Outputs (except PH and OSCO)					
Output voltage HIGH at $-I_{OH}$ = 0,5 mA	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 0,5 mA	V_{OL}	–	–	0,4	V
Output PH					
Output voltage HIGH at $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V	I_{OR}	–	–	5	μA
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{OR}	–	–	1	μA
Output leakage current at V_O = 0 V; V_{DD} = 7,5 V	$-I_{OR}$	–	–	5	μA
Output leakage current at V_O = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{OR}$	–	–	1	μA
Output OSCO					
Output voltage HIGH at V_{OSCI} = 0 V; $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} - 0,5	–	–	V
Output voltage LOW at V_{OSCI} = V_{DD}; I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V

parameter	symbol	min.	typ.	max.	unit
Input/output DL (open drain)*					
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V	I_{OR}	–	–	5	μA
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{OR}	–	–	1	μA
Load resistance (Fig. 4)					
at V_{DD} = 5,7 V	R_L	1,4	–	–	kΩ
at V_{DD} = 7,5 V	R_L	0,82	–	–	kΩ
Time constant (Fig. 4)					
at V_{DD} = 5,7 V	R_LC_L	–	–	19	ns
at V_{DD} = 7,5 V	R_LC_L	–	–	13	ns
Oscillator frequency (Fig. 4)					
Maximum oscillator frequency at V_{DD} = 5,7 V	f_{OSCI}	5,1	–	–	MHz

* An external pull-up resistor (3,9 kΩ) must be connected between DL and V_{DD}. The time constant R_LC_L must not exceed the values given.

APPLICATION INFORMATION

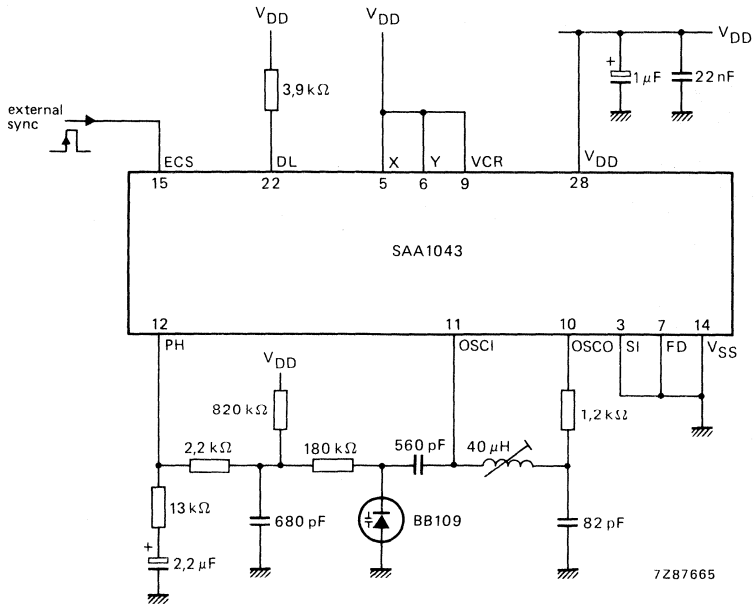


Fig. 11 Synchronizing circuit using passive filter network.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

SUBCARRIER COUPLER

GENERAL DESCRIPTION

The SAA1044 maintains the correct relationship between subcarrier and horizontal scan frequencies when an exact coupling is required. It is for use in combination with sync generator SAA1043 for application in colour video sources (cameras, film-scanners and similar equipments).

Features

- Provides exact relationship between subcarrier and horizontal scan frequencies
- Accommodates all standard frequencies
- Facilitates GENLOCK (general locking) applications

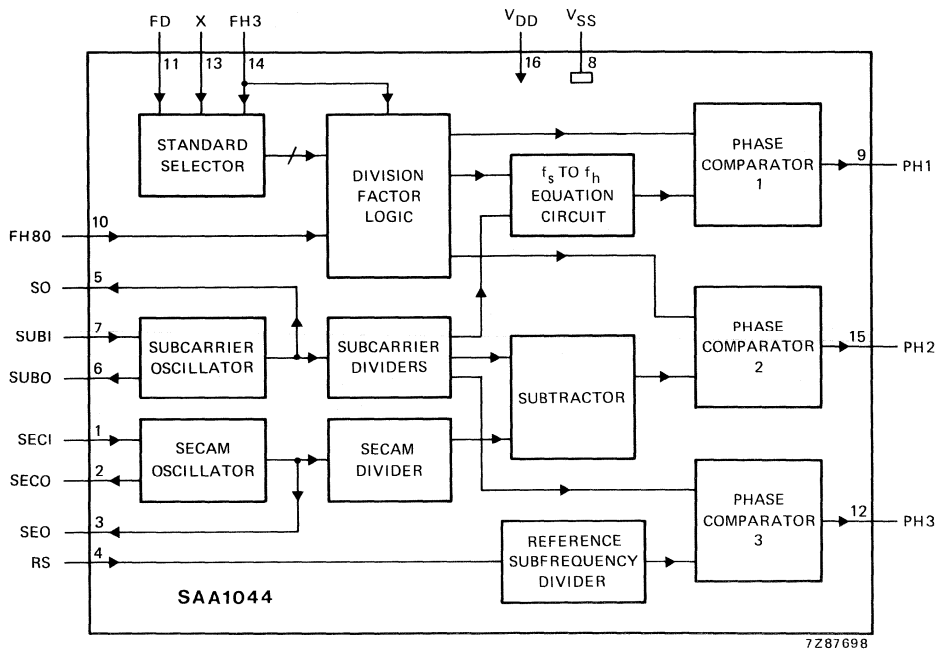


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

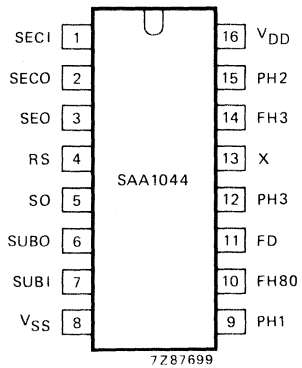


Fig. 2 Pinning diagram.

PINNING

1	SECI	SECAM oscillator input ($272f_H$)
2	SECO	SECAM oscillator output ($272f_H$)
3	SEO	inverted SECAM oscillator output
4	RS	reference subfrequency
5	SO	inverted subcarrier oscillator output
6	SUBO	subcarrier oscillator output
7	SUBI	subcarrier oscillator input
8	V_{SS}	negative supply voltage (ground)
9	PH1	phase comparator 1 output (FH80/SUBI)
10	FH80	1,25 MHz input (from SAA1043)
11	FD	standard programming input
12	PH3	phase comparator 3 output (RS/SUBI)
13	X	standard programming input
14	FH3	standard programming input (from SAA1043)
15	PH2	phase comparator 2 output (SECI/FH80)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Programming of operating standard

The standard required for operation is programmed using the inputs FD, X and FH3 as shown in Table 1.

Table 1 Programming of operating standard

standard	FD	X	FH3	relationship of subcarrier frequency (f_S) to horizontal scan frequency (f_H)
PAL	0	1	400 Hz	$f_S = 283{,}7516f_H$
SECAM	0	0	don't care	$f_S = 282f_H$
PAL-N	1	1	400 Hz	$f_S = 229{,}2516f_H$
PAL-M	1	0	1	$f_S = 227{,}25f_H$
NTSC	1	0	0	$f_S = 227{,}5f_H$

Positive logic: 1 = HIGH; 0 = LOW

Subcarrier/horizontal scan frequency relationship

The input FH80 from SAA1043 is the reference for horizontal scan frequency (f_H). This frequency is reduced by a factor determined by the selected operating standard to give a value of $8f_H$ (PAL, SECAM) or $10f_H$ (PAL-N, PAL-M, NTSC) to phase comparator 1. The subcarrier frequency (f_S) is manipulated to provide a comparable value at the second input to the phase comparator. When the frequencies of the two inputs to phase comparator 1 are equal, the relationship between f_H and f_S is as shown in Table 1.

Phase comparator 1 functions with an exclusive-OR phase detector circuit and provides an output which may be used to control a voltage-controlled oscillator (VCO) via a low-pass filter. The VCO reference can be the subcarrier or the horizontal scan frequency and the filter can be active or passive, depending on application.

A second subcarrier oscillator circuit is provided for SECAM operation. The operating frequency of this is centred on $272f_H$ to give, when $f_S = 282f_H$, comparable values of $5f_H$ at the two inputs to phase comparator 2. A second VCO loop can be used to control the SECAM oscillator frequency.

The high degrees of accuracy and stability required for GENLOCK applications are met by phase comparator 3. This compares the internal subcarrier and external reference frequencies. To adjust the phase over 2π, this comparator has a linear characteristic over 4π. The output signal PH3 has a period time of $f_S/4$ and a duty cycle of between 12,5% and 62,5% giving a sensitivity of 240 mV/rad. Errors due to temperature variation are minimized by symmetrical circuit and chip design.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}		−0,5 to + 15	V
Input voltage range	V_I	−0,5 to	(V_{DD} + 0,5)*	V
Input current	$\pm I_I$	max.	10	mA
Output voltage range	V_O	−0,5 to	(V_{DD} + 0,5)*	V
Output current	$\pm I_O$	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Storage temperature range	T_{stg}		−55 to + 150	°C

HANDLING

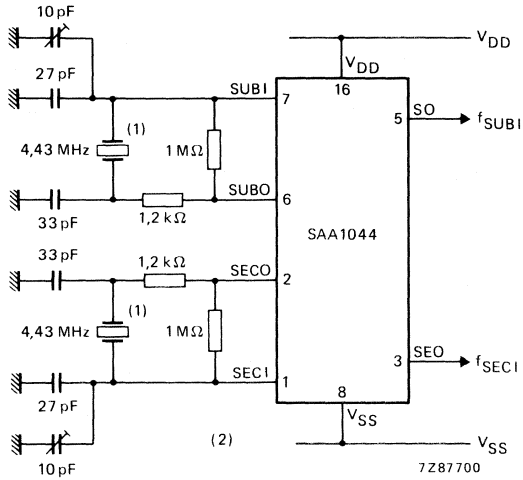
Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5,7 to 7,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

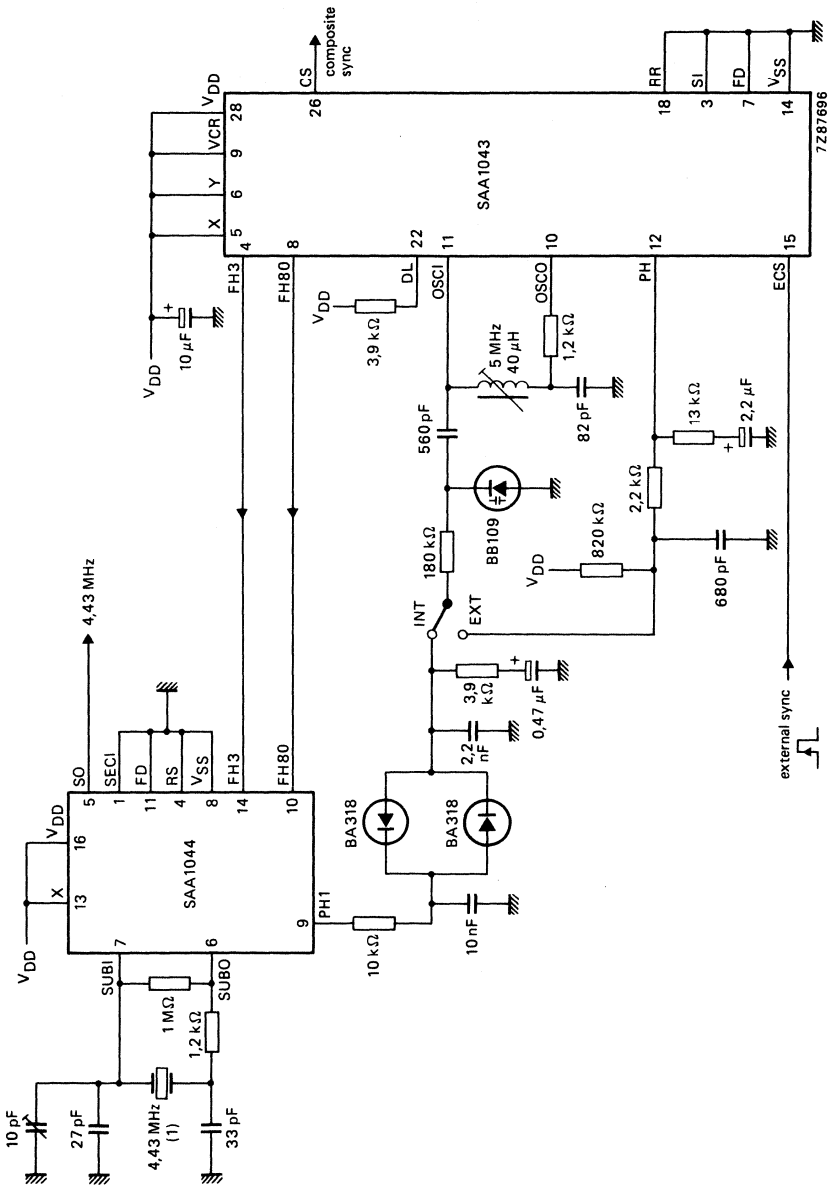
parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5,7	–	7,5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{IR}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{IR}$	–	–	1	μA
Outputs (except SECO and SUBO)					
Output voltage HIGH at $-I_{OH}$ = 0,5 mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW at I_{OL} = 0,5 mA	V_{OL}	–	–	0,4	V
Outputs SECO and SUBO					
Output voltage HIGH at $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Oscillator frequency (Fig. 3)					
Maximum oscillator frequency at V_{DD} = 5,7 V	f_{SUBI} / f_{SECI}	5,1	–	–	MHz



(1) Catalogue number of crystal: 4322 143 04040.
(2) Inputs not shown are don't care.

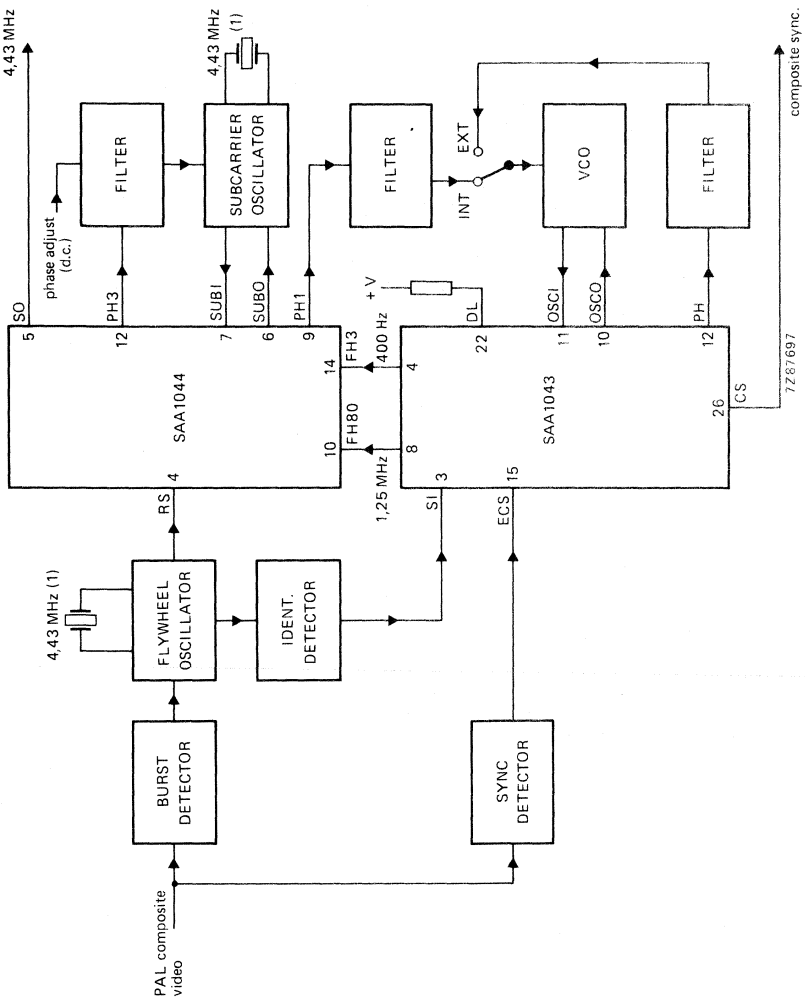
Fig. 3 Test set-up for oscillator frequency measurement.

APPLICATION INFORMATION



(1) Catalogue number of crystal: 4322 143 04040.

Fig. 4 Subcarrier coupling for PAL application; external synchronization is selected with switch in EXT condition.



(1) Catalogue number of crystal: 4322 143 04040.

Fig. 5 Subcarrier coupling for PAL GENLOCK application.

RADIO TUNING PLL FREQUENCY SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

QUICK REFERENCE DATA

Supply voltage ranges	V_{CC1}	3,6 to 12	V
	V_{CC2}	3,6 to 12	V
	V_{CC3}	V_{CC2} to 31	V
Supply currents	$I_{CC1} + I_{CC2}$	typ. 18	mA
	I_{CC3}	typ. 0,8	mA
Input frequency ranges			
at pin FAM	f_{FAM}	512 kHz to 32	MHz
at pin FFM	f_{FFM}	70 to 120	MHz
Maximum crystal input frequency	f_{XTAL}	> 4	MHz
Operating ambient temperature range	T_{amb}	−25 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102H).

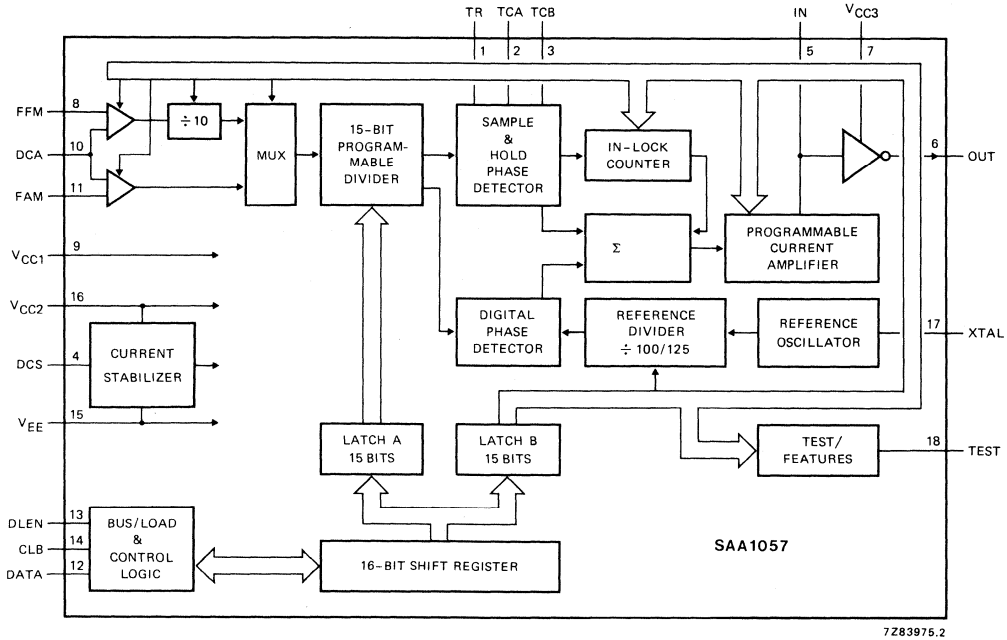


Fig. 1 Block diagram.

GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.
The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

FM — FM/AM selection; '1' = FM, '0' = AM

REFH — reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector)

CP3, CP2, CP1, CP0 — control bits for the programmable current amplifier (see section Characteristics)

SB2 — enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically

SLA — load mode of latch A; '1' = synchronous, '0' = asynchronous

PDM1, PDM0 — phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM — bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on

T3 — test bit; must be programmed always '0'

T2 — test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin

T1 — test bit; must be programmed always '0'

T0 — test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output programmable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

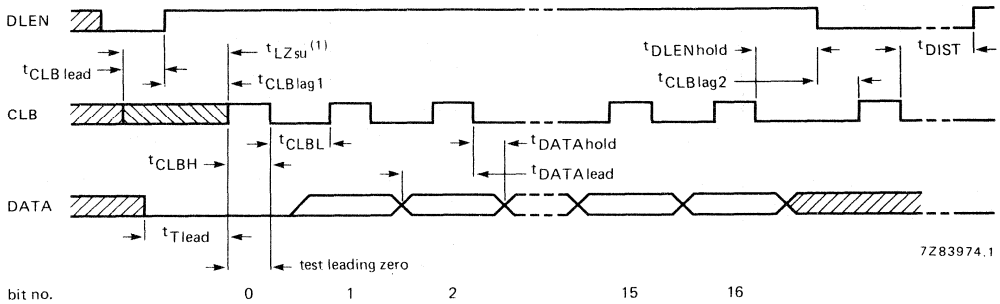


Fig. 2 BUS format.

(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I^2C bus is used for other devices on the same data and clock lines.

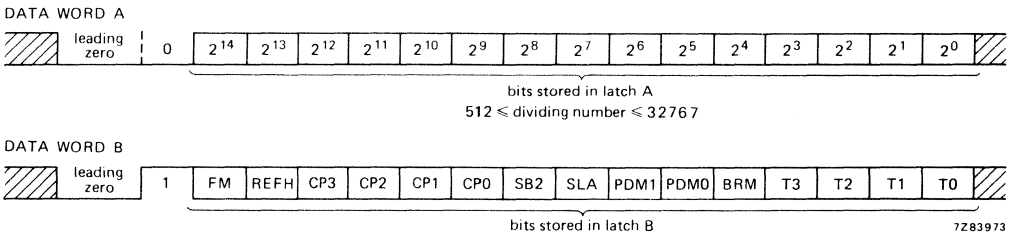


Fig. 3 Bit organization of data words A and B.

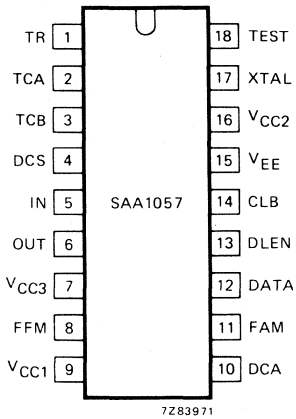


Fig. 4 Pinning diagram.

PINNING

1	TR	resistor/capacitors for sample and hold circuit
2	TCA	
3	TCB	
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	BUS
13	DLEN	
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; logic and analogue part	V_{CC1}; V_{CC2}	−0,3 to 13,2	V
Supply voltage; output amplifier	V_{CC3}	V_{CC2} to + 32	V
Total power dissipation	P_{tot}	max. 800	mW
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Storage temperature range	T_{stg}	−65 to + 150	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltages	V_{CC1}	3,6	5	12	V	
	V_{CC2}	3,6	5	12	V	
	V_{CC3}	V_{CC2}	–	31	V	
Supply currents*						
AM mode	I_{tot}	–	16	–	mA	$I_{tot} = I_{CC1} + I_{CC2}$ in-lock: BRM = '1'; PDM = '0'
FM mode	I_{tot}	–	20	–	mA	
	I_{CC3}	0,3	0,8	1,2	mA	I_{OUT} = 0
Operating ambient temperature	T_{amb}	−25	–	+80	°C	
RF inputs (FAM, FFM)						
AM input frequency	f_{FAM}	512 kHz	–	32	MHz	
FM input frequency	f_{FFM}	70	–	120	MHz	
Input voltage at FAM	$V_{i\ (rms)}$	30	–	500	mV	
Input voltage at FFM	$V_{i\ (rms)}$	10	–	500	mV	
Input resistance at FAM	R_i	–	2	–	kΩ	
Input resistance at FFM	R_i	–	135	–	Ω	
Input capacitance at FAM	C_i	–	3,5	–	pF	
Input capacitance at FFM	C_i	–	3	–	pF	
Voltage ratio allowed between selected and non-selected input	V_s/V_{ns}	–	−30	–	dB	
Crystal oscillator (XTAL)						see note 1
Maximum input frequency	f_{XTAL}	4	–	–	MHz	
Crystal series resistance	R_s	–	–	150	Ω	
BUS inputs (DLEN, CLB, DATA)						
Input voltage LOW	V_{IL}	0	–	0,8	V	
Input voltage HIGH	V_{IH}	2,4	–	V_{CC1}	V	
Input current LOW	$-I_{IL}$	–	–	10	μA	V_{IL} = 0,8 V
Input current HIGH	I_{IH}	–	–	10	μA	V_{IH} = 2,4 V

* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
BUS inputs timing (DLEN, CLB, DATA)						see also Fig. 2 and note 2
Lead time for CLB to DLEN	$t_{CLBlead}$	1	–	–	μs	
Lead time for DATA to the first CLB pulse	t_{Tlead}	0,5	–	–	μs	
Set-up time for DLEN to CLB	$t_{CLBlag1}$	5	–	–	μs	
CLB pulse width HIGH	t_{CLBH}	5	–	–	μs	
CLB pulse width LOW	t_{CLBL}	5	–	–	μs	
Set-up time for DATA to CLB	$t_{DATAlead}$	2	–	–	μs	
Hold time for DATA to CLB	$t_{DATAhold}$	0	–	–	μs	
Hold time for DLEN to CLB	$t_{DLENhold}$	2	–	–	μs	
Set-up time for DLEN to CLB load pulse	$t_{CLBlag2}$	2	–	–	μs	
Busy time from load pulse to next start of transmission	t_{DIST}	5	–	–	μs	next transmission after word 'B' to other device
Busy time						or
asynchronous mode	t_{DIST}	0,3	–	–	ms	next transmission to SAA1057 after word 'A' (see also note 5)
synchronous mode	t_{DIST}	1,3	–	–	ms	
Sample and hold circuit (TR, TCA, TCB)						see also notes 3; 4
Minimum output voltage	V_{TCA}, V_{TCB}	–	1,3	–	V	
Maximum output voltage	V_{TCA}, V_{TCB}	–	–	V_{CC2}–0,7	V	
Capacitance at TCA (external)	C_{TCA}	–	–	2,2	nF	REFH = '1'
	C_{TCA}	–	–	2,7	nF	REFH = '0'
Discharge time at TCA	t_{dis}	–	–	5	μs	REFH = '1'
	t_{dis}	–	–	6,25	μs	REFH = '0'
Resistance at TR	R_{TR}	100	–	–	Ω	external
Voltage at TR during discharge	V_{TR}	–	0,7	–	V	
Capacitance at TCB	C_{TCB}	–	–	10	nF	external
Bias current into TCA, TCB	I_{bias}	–	–	10	nA	in-lock

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Programmable current amplifier (PCA)						
Output current of the dig. phase detector	$\pm I_{dig}$	–	0,4	–	mA	
Current gain of PCA						
CP3 CP2 CP1 CP0						
P1 0 0 0 0	G_{P1}	–	0,023	–		$V_{CC2} \geqslant 5$ V (only for P1)
P2 0 0 0 1	G_{P2}	–	0,07	–		
P3 0 0 1 0	G_{P3}	–	0,23	–		
P4 0 1 1 0	G_{P4}	–	0,7	–		
P5 1 1 1 0	G_{P5}	–	2,3	–		
Ratio between the output current of S/H into PCA and the voltage on C_{TCB}	S_{TCB}	–	1,0	–	μA/V	
Offset voltage on TCB	ΔV_{TCB}	–	–	1	V	in-lock
Output amplifier (IN,OUT)						
Input voltage	V_{IN}	–	1,3	–	V	in-lock; equal to internal reference voltage
Output voltages						
minimum	V_{OUT}	–	–	0,5	V	$-I_{OUT}$ = 1 mA
maximum	V_{OUT}	$V_{CC3}-2$	–	–	V	I_{OUT} = 1 mA
maximum	V_{OUT}	$V_{CC3}-1$	–	–	V	I_{OUT} = 0,1 mA
Maximum output current	$\pm I_{OUT}$	5	–	–	mA	V_{OUT} = ½ V_{CC3}
Test output (TEST)*						
Output voltage LOW	V_{TL}	–	–	0,5	V	
Output voltage HIGH	V_{TH}	–	–	12	V	
Output current OFF	I_{Toff}	–	–	10	μA	V_{TH}
Output current ON	I_{Ton}	150	–	–	μA	V_{TL}
Ripple rejection**						
at f_{ripple} = 100 Hz						
$\Delta V_{CC1}/\Delta V_{OUT}$		–	77	–	dB	
$\Delta V_{CC2}/\Delta V_{OUT}$		–	70	–	dB	
$\Delta V_{CC3}/\Delta V_{OUT}$		–	60	–	dB	$V_{OUT} \leqslant V_{CC3}-3$ V

* Open collector output.

** Measured in Fig. 6.

NOTES

1. Pin 17 (XTAL) can also be used as input for an external clock.
   The circuit for that is given in Fig. 5. The values given in Fig. 5 are a typical application example.

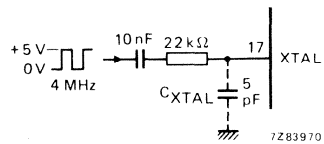


Fig. 5 Circuit configuration showing external 4 MHz clock.

2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically ½ V_{CC2}+0,3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ V_{CC2}+0,3 V.
4. Crystal oscillator frequency f_{XTAL} = 4 MHz.
5. The busy-time after word "A" to another device which has more clock pulses than the SAA1057 (> 17) must be the same as the busy-time for a next transmission to the SAA1057.
   When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time, 5 μs will be sufficient.

APPLICATION INFORMATION

Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.
For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

Synchronous/asynchronous operation

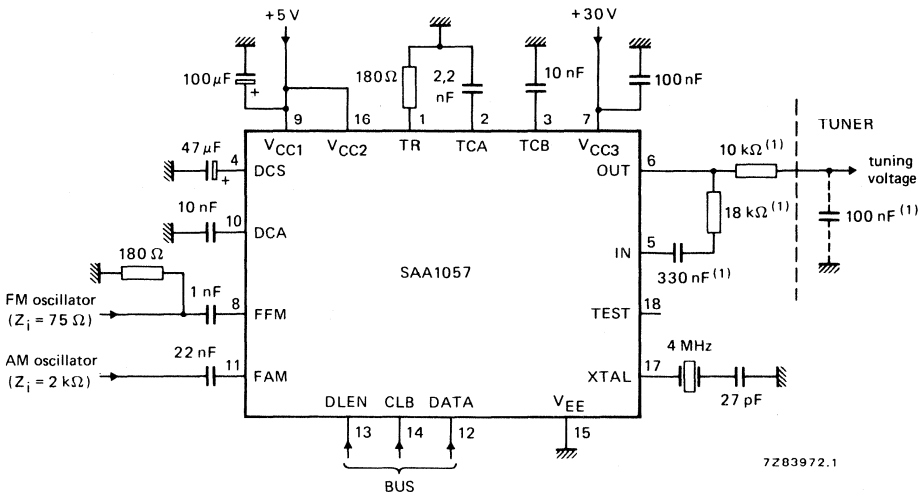
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').

Transient times of the bus signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100 ns. Otherwise the signal-to-noise ratio of the tuning voltage is reduced.



(1) Values depend on the tuner diode characteristics.

Fig. 6 Application example of the SAA1057PLL frequency synthesizer module.

LED DISPLAY/INTERFACE CIRCUIT

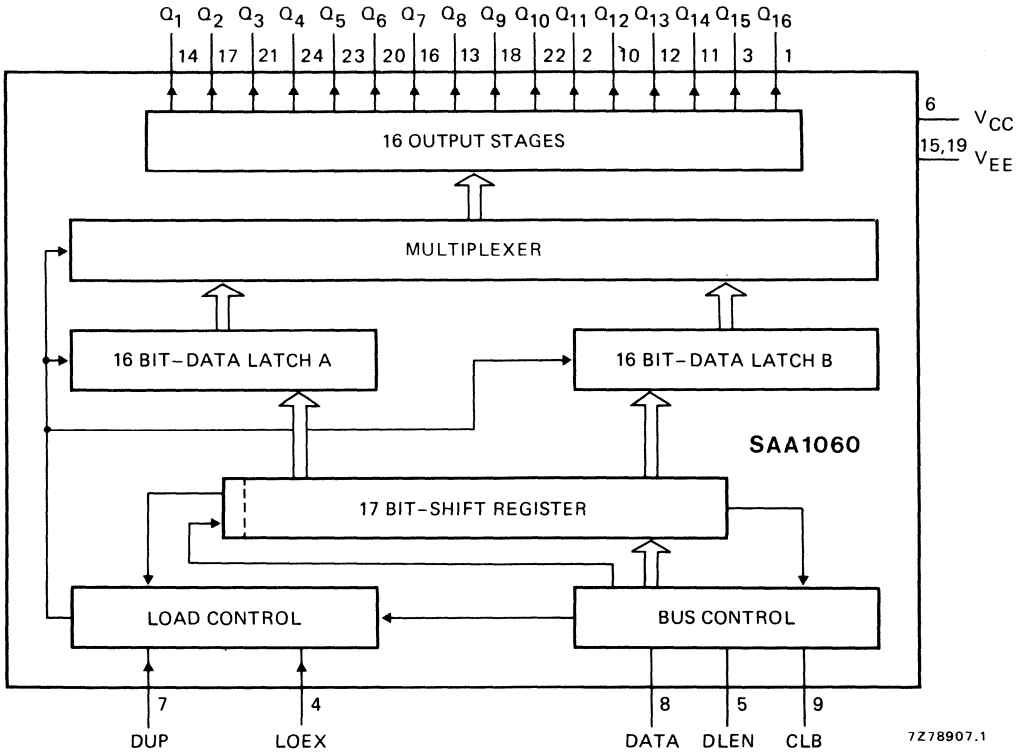


Fig. 1 Block diagram.

Features

- Driving 7, 14, 16-segment displays.
- Driving linear displays, bar graph displays for analogue functions.
- Serial to parallel decoder.
- Bus control for the selection of 18-bit words.
- 2 x 16-bit latch.
- Duplex operation for two modes of output: static (16 bit) or dynamic (2 x 16 bit).
- Data transfer control.
- 2 outputs for higher output current (80 mA).

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4 to 6 V
Operating ambient temperature range	T_{amb}		−20 to + 80 °C
Maximum input frequency	f_I	typ.	50 kHz
Supply current	I_{CC}	typ.	60 mA
Output current	I_Q	<	40 mA
Output current (Q_8 and Q_{16} only)	I_Q	<	80 mA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

The integrated circuit SAA1060 is primarily designed to drive the display unit of a digital tuning system. It can also be used as a 16-bit serial to parallel decoder. Since the device has no decoder (this is handled by a microcomputer), it has many applications:

- driving 7-segment displays
- driving 14-segment displays
- driving linear displays, e.g. pointer, bar graph
- static output of switch-functions
- digital to analogue converter, with external R-2R network
- extension of the number of outputs for microprocessors or microcomputers.

Data transmission is initiated by means of a burst of clock pulses (CLB), a data line enable signal (DLEN) and the data signal (DATA). The bus control circuit distinguishes between interference and valid data by checking word length (17 bits) and the leading zero. This allows different bus information to be supplied on the same bus lines for other circuits (e.g. SAA1056 with 16 bits).

The last bit (bit 17) of the data word contains the information which of the two internal latches will be loaded. The input LOEX determines if the latched data of selected latches is presented directly to the outputs, or synchronized with the data select signal DUP.

The output stages are n-p-n transistors with open collectors. The current capability is designed for the requirements of duplex operation. Two of the outputs (Q_8 and Q_{16}) are arranged for double current, so that 2 x 2 segments can be connected in parallel.

OPERATION DESCRIPTION

Data inputs (DLEN, DATA)

The SAA1060 processes serially the 18-bit data words synchronized with the clock burst (CLB) and applied to the data input DATA. A command will be accepted only when the data line enable input (DLEN) is HIGH (see Fig. 3).

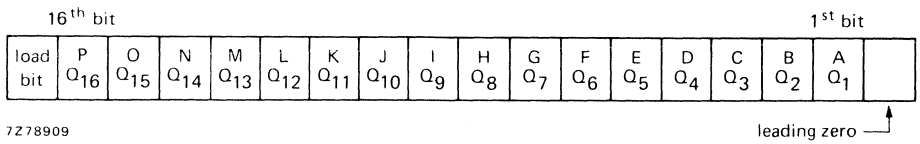


Fig. 2 Organization of a data word.

Condition for 17th bit:
0 = load data latch B
1 = load data latch A

The loading of the accepted information in one of the data latches is done by the 19th clock pulse, when DLEN is LOW.

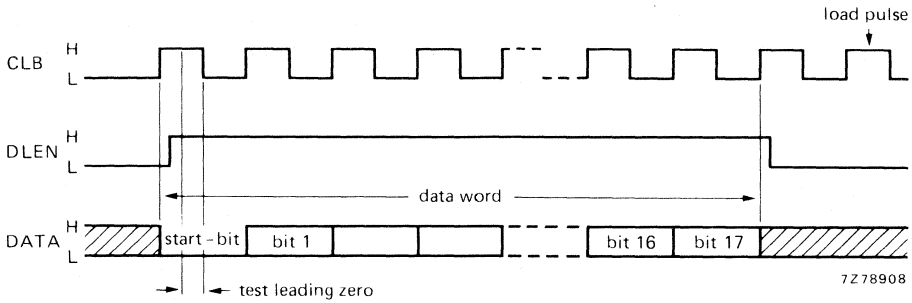


Fig. 3 Pulse diagram of the 16-bit data transmission.

Each data word must start with a leading zero. The SAA1060 checks the data word for the correct length (18 bits) and also for the leading zero.
The actual data is switched directly to the appropriate outputs. For switching on a segment, a '0' (LOW) is necessary at the appropriate data bit.

Data selection input (DUP)

The logic states at input DUP determine which of the two latch contents can be found on the output.

0 = latch A contents
1 = latch B contents

Load control input (LOEX)

Input LOEX determines the operation mode in which the device is able to work.

0 = duplex mode, i.e. output synchronized with the duplex signal
1 = d.c. mode, i.e. output direct from the by DUP selected data latch.

When operating in duplex mode at 50 Hz, the time between two data words to be transmitted must be > 21 ms.

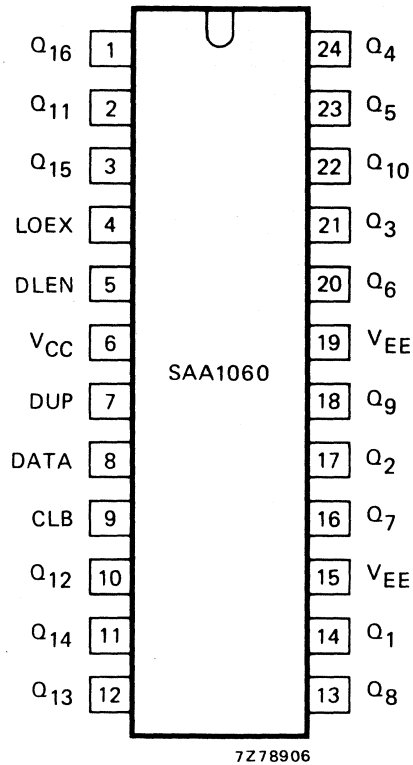


Fig. 4 Pinning diagram.

RATINGS (V_{EE} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}	−0,3 to + 7	V
Total power dissipation	P_{tot}	max. 900	mW
Operating ambient temperature range	T_{amb}	−20 to + 80	°C
Storage temperature range	T_{stg}	−25 to + 125	°C

CHARACTERISTICS

V_{EE} = 0; T_{amb} = 25 °C; unless otherwise specified

	V_{CC} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{CC}	4	5	6	V	
Supply current	5	I_{CC}	–	60	–	mA	
Inputs DATA, CLB, DLEN, LOEX							
input voltage HIGH	5	V_{IH}	2	–	5	V	
input voltage LOW	5	V_{IL}	–	–	1	V	
input current LOW	5	$-I_{IL}$	–	–	20	μA	V_I = 0
maximum input frequency	5	f_I	–	50	–	kHz	
Input DUP							
input voltage HIGH	5	V_{IH}	0,8	–	12	V	
input voltage LOW	5	V_{IL}	–6	–	0,4	V	
input current HIGH	5	I_{IH}	0,01	–	12	mA	
maximum input frequency	5	f_I	–	50	–	kHz	
Outputs Q_1 to Q_7, Q_9 to Q_{15}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	I_{QH} = 0
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 40 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	60	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	20	40	mA	
Outputs Q_8 and Q_{16}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	I_{QH} = 0
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 80 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	120	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	40	80	mA	

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

LCD DISPLAY/INTERFACE CIRCUIT

GENERAL DESCRIPTION

The SAA1062A is designed to drive a Liquid Crystal Display (LCD) of a digital tuning system. It contains a shift register with programmable length (18 or 21 bits), latches, both synchronized or static, exclusive-OR segment drivers (17 or 20 bits), an l.f. oscillator and a backplane driver for the LCD. The circuit is designed to be driven by a 3 bus structure from a microcomputer and can also be used as a programmable 17 or 20 bits serial-to-parallel decoder. It is also capable of storing 40 bits of information.

Features

- Driving 7 to 20-segment displays.
- Driving linear displays.
- Serial to parallel decoder of digital signals.
- Bus control for the selection of 18/21-bit words.
- 17/20-bit latch.
- A.C. segment drive.
- On-chip oscillator.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	4,2 to 5,5	V
Operating ambient temperature range	T_{amb}	−20 to + 70	°C
Maximum input frequency	f_i	typ. 50	kHz
Supply current	I_{CC}	typ. 3,5	mA
Output current (Q_1 to Q_{20})	I_Q	> 60	μA

PACKAGE OUTLINES

SAA1062A : 28-lead DIL; plastic (SOT-117).
SAA1062AT: 28-lead mini-pack; plastic (SO-28; SOT-136A).

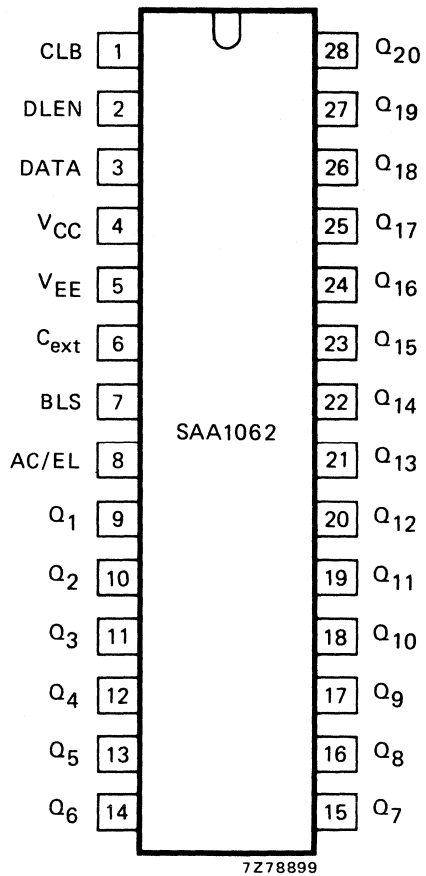


Fig. 1 Pinning diagram.

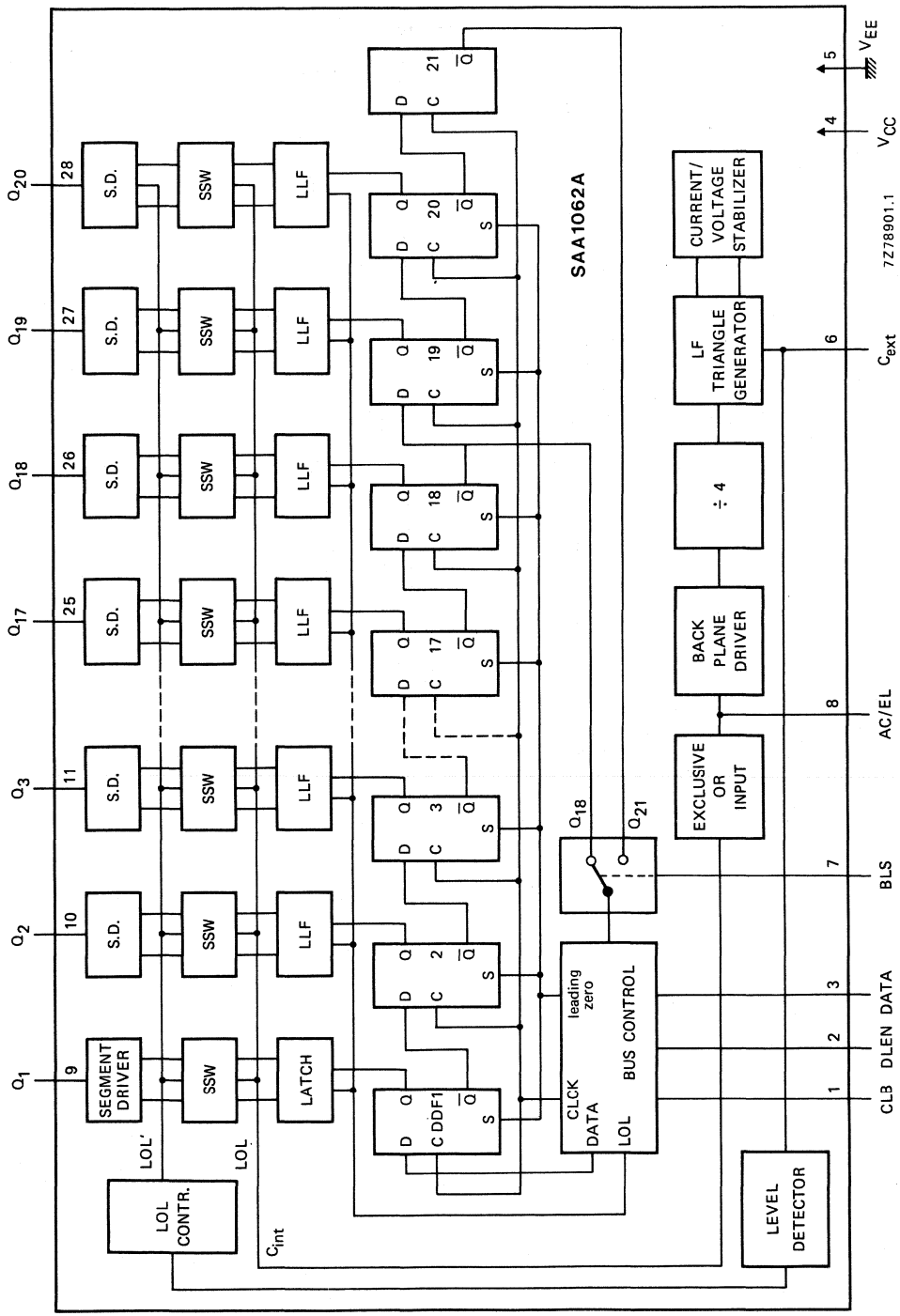


Fig. 2 Block diagram.

OPERATION DESCRIPTION

The input information for this device consists of a data bus with 18 or 21 bits words, an external clock synchronized with the data bus and an enable signal. The organization of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is made whether these signals are valid for the device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal is HIGH, during the first HIGH period of the clock signal. During the HIGH period of DLEN, the length control determines if the clock signal consists of the programmed number of pulses (18 or 21). This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device from accepting inferferences on the signal lines. While leading zero is detected, the shift register is set and for a proper leading zero the following data is shifted into this register. The Q_n position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input are correct. Incorrect length of the information is detected by checking the value of the last bit of the programmed register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOL).

This pulse enables the load control circuit to load the contents of the register into the output latch immediately. On the first edge of the backplane driver signal "AC out/EL in" following on this "LOL" pulse, the new information of this latch is transferred to the output driver which also contains a latch. With this ability it is possible to load the device with 20 bits and also to transfer this data to the segment outputs. Furthermore, the SR can be reloaded by a second complete load procedure without a load enable clock pulse. This causes the SR to contain 20 bits and the output latches another 20 bits of information.

The output driver also contains an EXCLUSIVE-OR which is driven by the backplane driver signal and the latch output. The segment driver output signal is in phase with the output of the backplane driver when the input data is HIGH ("1") and 180^{o} out-of-phase when the input data is LOW ("0").

In the static or slave mode, the backplane output can be used as input by connecting pin 6 to ground or V_{CC}. The IC now can operate as a static driver or as a synchronized slave.

The l.f. oscillator consists of a triangle generator of the I-2I principle. It only needs an external capacitor to fix the frequency. As both amplitude and current are temperature compensated, this frequency is more or less independent of pn temperature. An internal switching signal of this generator is divided by 4 to attain a symmetrical output for the backplane driver (pin 8) of nominal 60 Hz for an external capacitor of 22 nF.

The backplane driver is able to drive a 40 bits display.

The bit length of the shift register is programmed with BLS (Bit Length Selector) (pin 7). If BLS is kept LOW the DATA bit length is 20; for BLS open or HIGH a DATA bit length of 17 is selected.

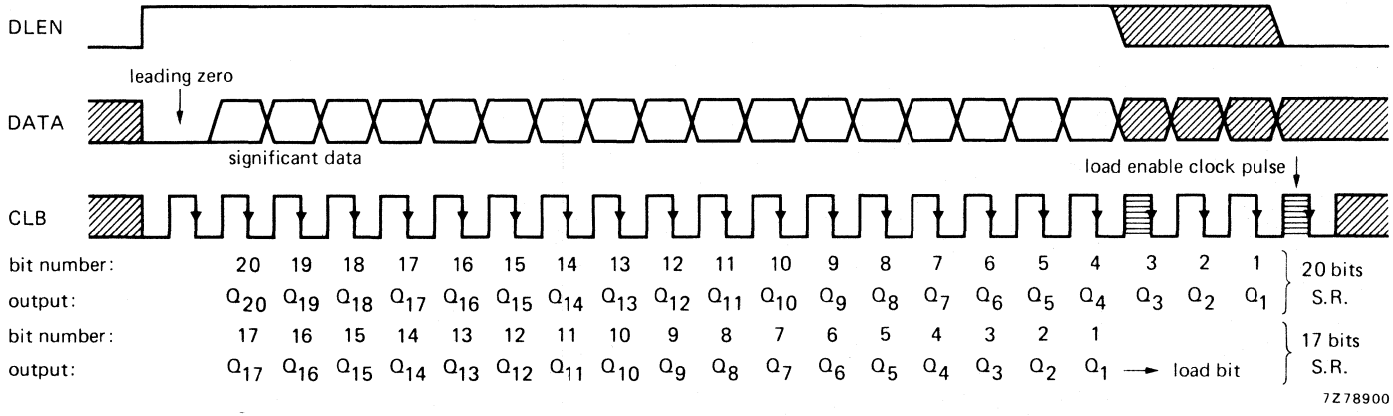


Fig. 3 Organization of 18 and 21 bit words; DATA = LOW means segment 'on'.

RATINGS (V_{EE} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	6 V
Total power dissipation at T_{amb} = 100 °C derate linearly with 0,02 W/°C	P_{tot}	max.	500 mW
Operating ambient temperature range	T_{amb}		−25 to + 125 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

CHARACTERISTICS

V_{EE} = 0; V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		condition
Supply voltage	V_{CC}	4,2	5	5,5	V	
Supply current	I_{CC}	–	3,5	–	mA	
Inputs CLB, DLEN, DATA, BLS						
input voltage HIGH	V_{IH}	1,6	–	V_{CC}	V	
input voltage LOW	V_{IL}	−1	–	+ 0,8	V	
maximum input frequency	f_I	–	50	–	kHz	
Input C_{ext}						
input voltage HIGH	V_{IH}	4,6	–	–	V	static mode
input voltage LOW	V_{IL}	−0,1	–	0,4	V	sync. slave mode
input current HIGH	I_{IH}	–	–	180	μA	
input current LOW	I_{IL}	–	–	−40	μA	
Input AC/EL (in slave mode)						
input voltage HIGH	V_{IH}	2,7	–	V_{CC}	V	
input voltage LOW	V_{IL}	−0,4	–	2,3	V	
Output C_{ext} (oscillator mode)						
oscillator frequency	f_{osc}	120	240	360	Hz	C = 22 nF
Output stage backplane (AC/EL)						
output current sink/source	I_O	2,4	–	–	mA	
Output Q_1 to Q_{20}						
output current sink/source	I_O	60	–	–	μA	
d.c. rest voltage between pin 8 (AC/EL) and one of the segment drivers (see Fig. 4)						
segment 'on' situation		–	–	25	mV	
segment 'off' situation		–	–	25	mV	

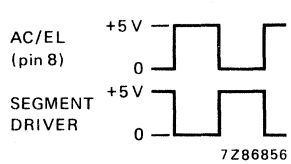


Fig. 4 AC/EL and segment driver pulses.
The d.c. voltage for segment 'on' is about 5 V.

FLUORESCENT DISPLAY/INTERFACE CIRCUIT

GENERAL DESCRIPTION

The SAA1063 is designed to drive the display unit of a digital tuning system. It contains a 17-bit shift register, latches, display multiplexers and output stages, capable of driving 4½ decades of a 7 segment fluorescent display in duplex mode. The decoding for the display is carried out in the data input (microcomputer).

Features

- Driving 4½ decades of a seven segment display in duplex mode.
- Microcomputer compatible.
- 17-bit shift register.
- D.C. and duplex operation.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4 to 5,5	V
Operating ambient temperature range	T_{amb}		−20 to +80	°C
Maximum input frequency	f_i	min.	50	kHz
Supply current	I_{CC}	typ.	20	mA
Output current	I_Q	max.	1,5	mA
Maximum output voltage swing	V_{Qmax}	min.	34,5	V

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A)

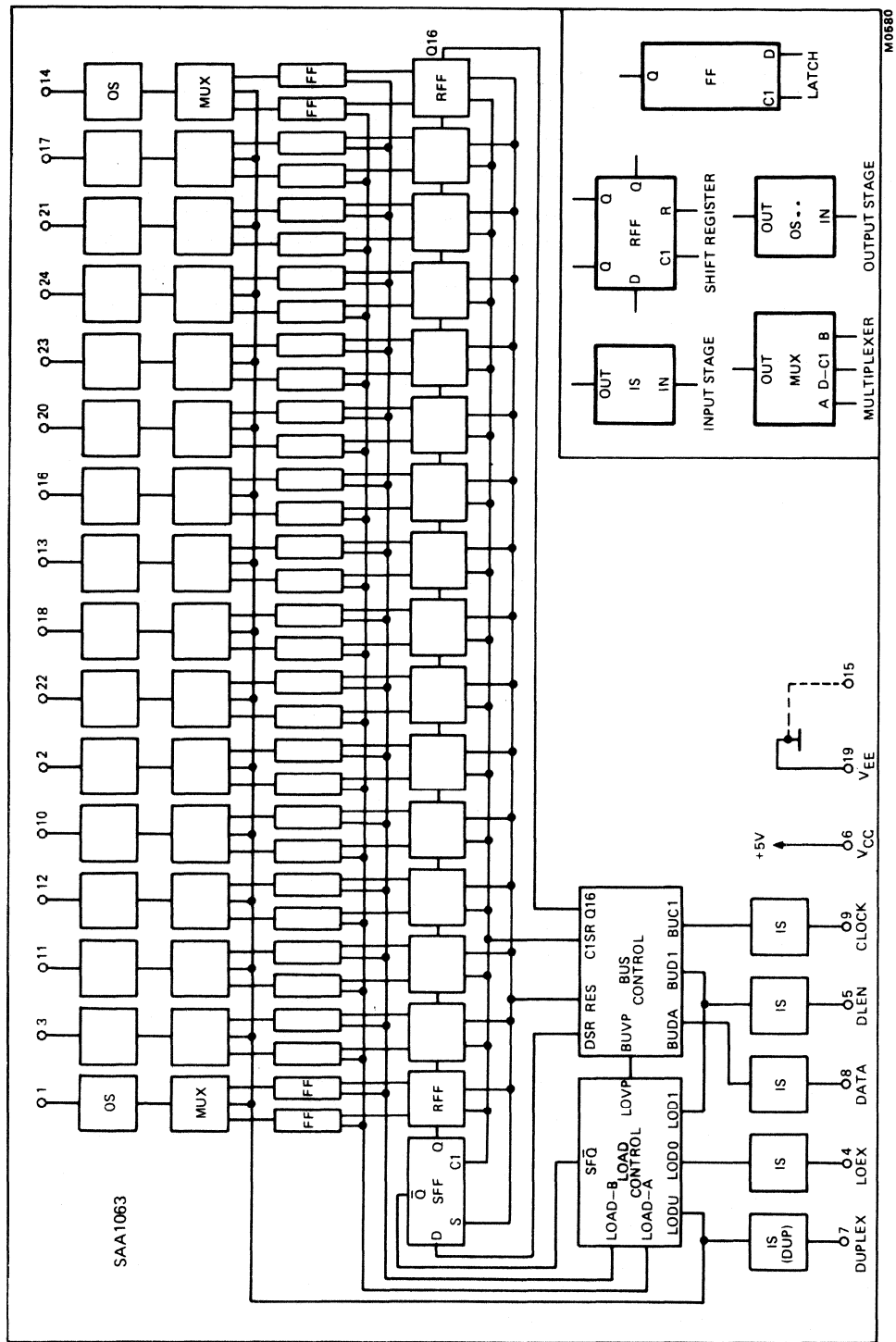


Fig. 1 Block diagram.
Insert indicates structure of logic elements.

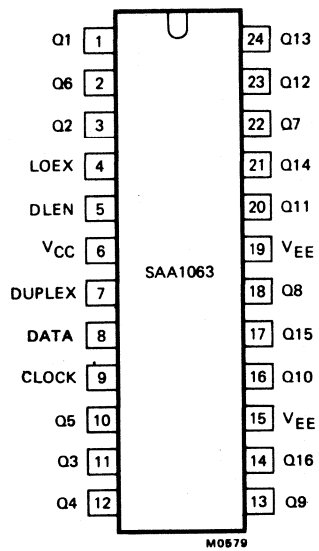


Fig. 2 Pinning diagram.

PINNING

1.	Q1		13.	Q9	segment drive outputs
2.	Q6	segment drive outputs	14.	Q16	
3.	Q2		15.	V_{EE}	ground
4.	LOEX	mode selection	16.	Q10	
5.	DLEN	bus enable	17.	Q15	segment drive outputs
6.	V_{CC}	+5 V power supply	18.	Q8	
7.	DUPLEX	duplex input	19.	V_{EE}	ground
8.	DATA	data input	20.	Q11	
9.	CLOCK	bus clock input	21.	Q14	
10.	Q5		22.	Q7	segment drive outputs
11.	Q3	segment drive outputs	23.	Q12	
12.	Q4		24.	Q13	

OPERATION DESCRIPTION

The input information for this device consists of a data bus with 17 bit words, an external clock synchronized with the data bus and an enable signal. The data format of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is taken as to whether these signals are valid for this device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal HIGH, during the first HIGH period of the clock signal. During the HIGH period of the DLEN signal, the length control determines if the clock signal consists of 18 pulses. This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device accepting interference on the signal lines. If leading zero is detected the shift register is reset and then the data is written into this register. The reset position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input is correct. Incorrect length of the information is detected by checking the value of the last bit of the register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOVP). This pulse enables the load control circuit to load the contents of the register into one of the two latches. When the load bit of the data word is HIGH the register contents are loaded into latch A; when this load bit is LOW the register contents are loaded into latch B. When the data information is accepted this load bit is written into the first bit of the shift register.

In duplex mode the load pulse is synchronised by the duplex signal, to avoid current transients in the output stages during the loading of the latches. The duplex mode operates in one of two mode conditions. When LOEX (pin 4) is LOW the duplex mode condition is selected; when LOEX is HIGH the d.c. mode condition is selected. The output stages are switched to the contents of latch A and latch B respectively.

When the duplex input (pin 7) is LOW the contents of latch A can be found on the output, when this input is HIGH the contents of latch B are found on the output.

In the duplex mode condition the output stages are capable of driving 32 duplexed segments of a fluorescent display. However, in the d.c. mode condition the output stages can only drive 16 segments of the display and two SAA1063 devices are required to drive a 4½ decade display unit.

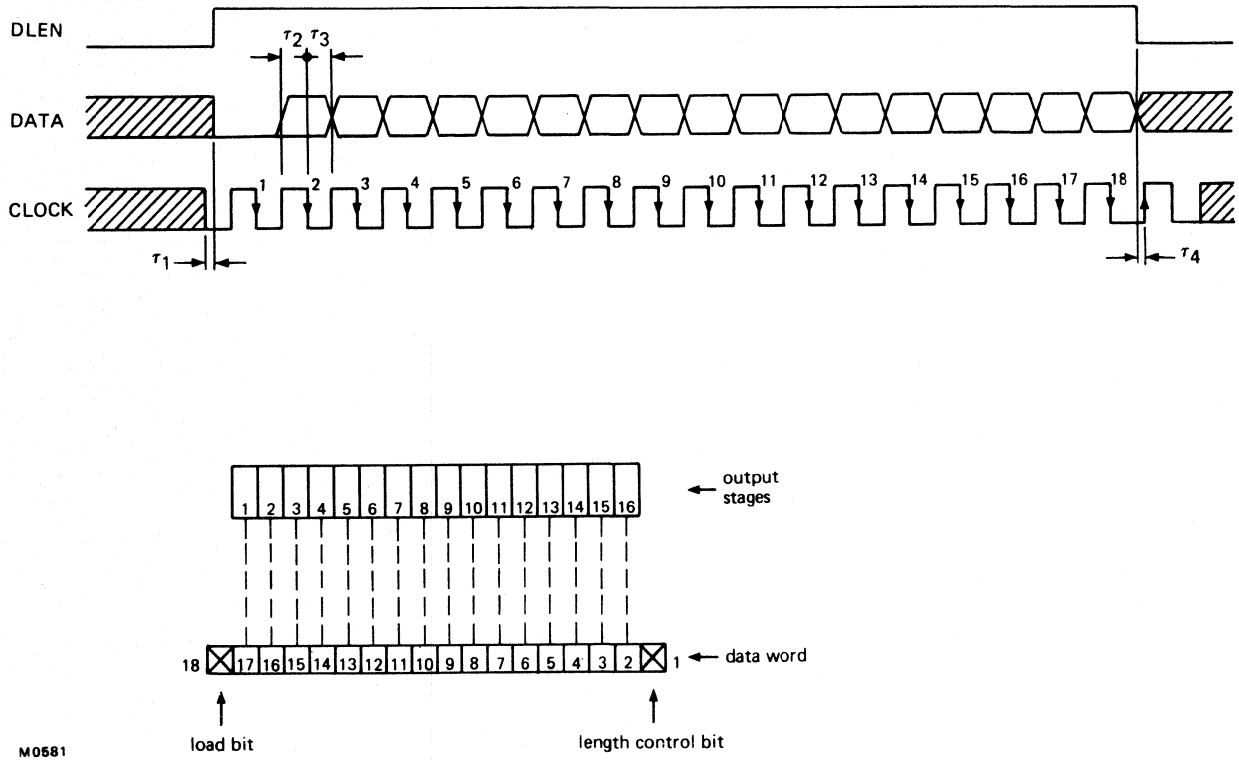


Fig. 3 Organisation of 18-bit data word.

Notes

1. The display segment is blanked by a HIGH data bit.
2. In duplex mode the period between the two data words must be greater than 21 ms.
3. Shaded timing periods are 'don't care' levels.
4. $\tau_1 > 4\ \mu s$ if a continuous clock is used. τ_2 and $\tau_3 > 4\ \mu s$. $\tau_4 > 2\ \mu s$.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	6	V
Total power dissipation at T_{amb} = 80 °C	P_{tot}	max.	900	mW
Operating ambient temperature range	T_{amb}		−20 to +80	°C
Storage temperature range	T_{stg}		−55 to +125	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.		conditions
Supply voltage	V_{CC}	4	5	5,5	V	
Supply current	I_{CC}	–	20	–	mA	
Inputs LOEX, DLEN, DATA, CLOCK						
input voltage HIGH	V_{IH}	2	–	5	V	
input voltage LOW	V_{IL}	0	–	0,8	V	
input current	$-I_{IH}$	–	–	20	μA	(V_I = 0 V)
max. input frequency	f_i	50	–	–	kHz	
DUPLEX						
input voltage HIGH	V_{IH}	0,8	–	20	V	
input voltage LOW	V_{IL}	−6	–	0,4	V	
input current HIGH	I_{IH}	0,01	–	12	mA	
input frequency	f_i	–	50	–	Hz	
Outputs Q1 to Q16						
output voltage HIGH	$-V_{OH}$	30	–	–	V	$I_O < 0{,}7$ μA
output voltage LOW	V_{OL}	4,5	–	–	V	I_O = 1 mA
output current	I_{OL}	–	–	1,5	mA	

4-DIGIT LED-DRIVER WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I²L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I²C bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{CC}	4,5	5	15	V
Supply current all outputs OFF	V_{CC} = 5 V	I_{CC}	–	9,5	–	mA
Total power dissipation 24-lead DIL (SOT-101B)		P_{tot}	–	–	1000	mW
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

PACKAGE OUTLINE

SAA1064P: 24-lead DIL; plastic (with internal heat spreader) (SOT-101B).

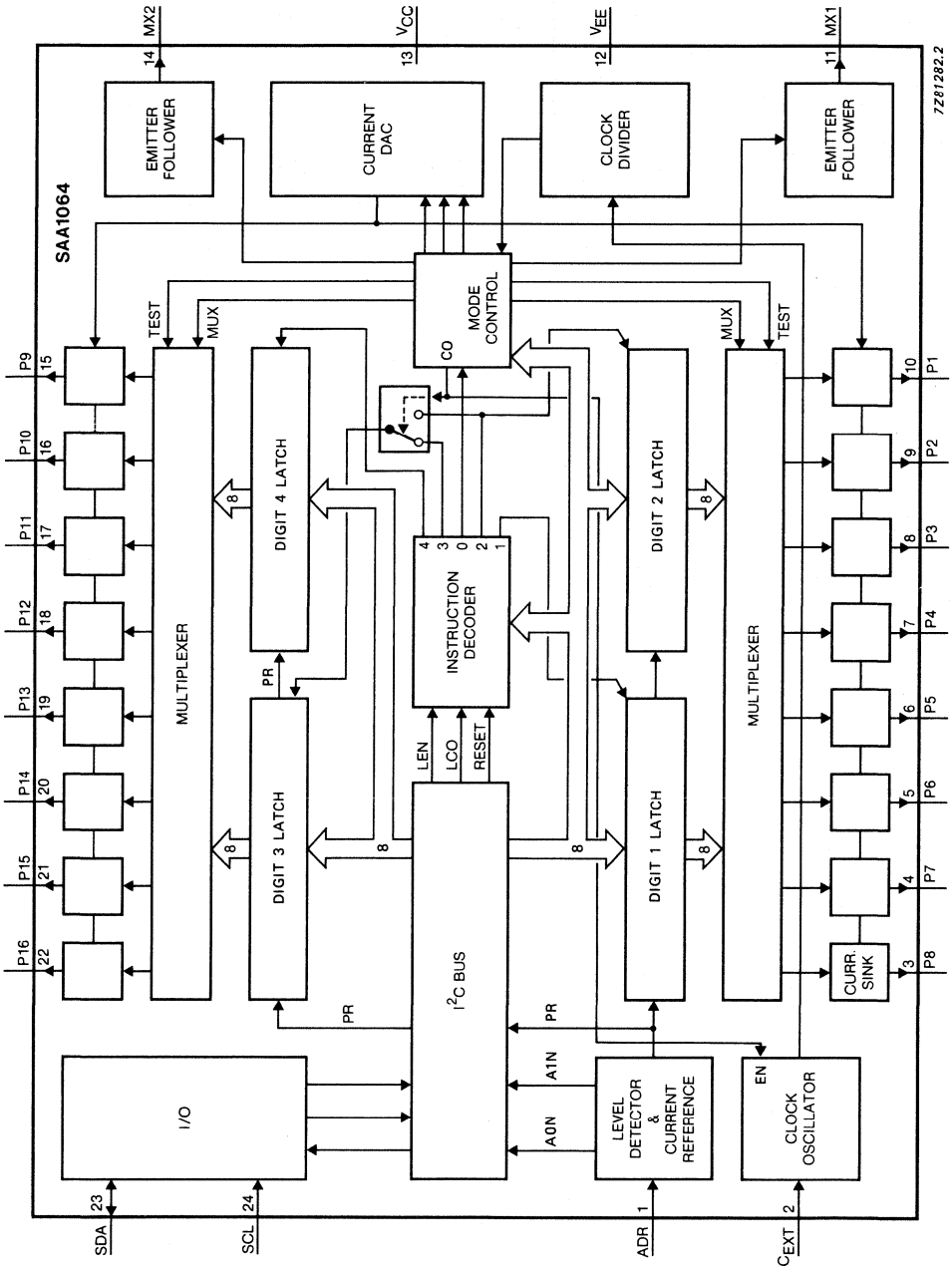


Fig. 1 Block diagram.

PINNING

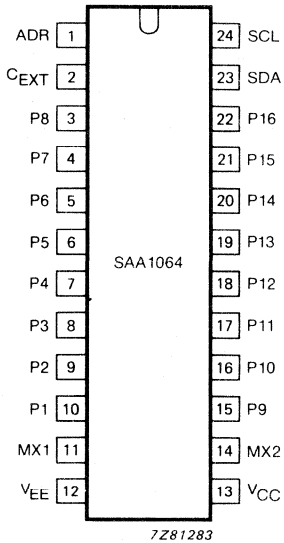


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

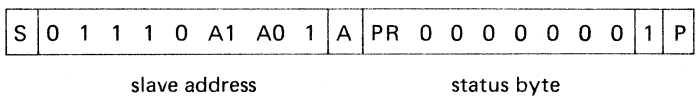


Fig. 3a I²C bus format; READ mode.

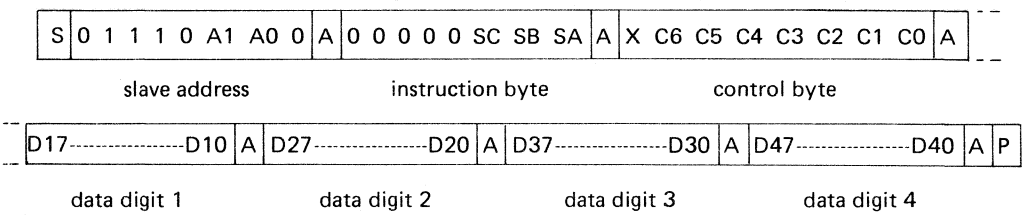


Fig. 3b I²C bus format; WRITE mode.

S = start condition
P = stop condition
A = acknowledge
X = don't care

A1, A0 = programmable address bits
SC SB SA = subaddress bits
C6 to C0 = control bits
PR = POWER RESET flag

Address pin ADR

Four different slave addresses can be chosen by connecting ADR either to V_{EE}, 3/8 V_{CC}, 5/8 V_{CC} or V_{CC}. This results in the corresponding valid addresses HEX 70, 72, 74 and 76 for writing and 71, 73, 75 and 77 for reading. All other addresses cannot be acknowledged by the circuit.

Status byte

Only one bit is present in the status byte, the POWER RESET flag. A logic 1 indicates the occurence of a power failure since the last time it was read out. After completion of the READ action this flag will be set to logic 0.

Subaddressing

The bits SC, SB and SA form a pointer and determine to which register the data byte following the instruction byte will be written. All other bytes will then be stored in the registers with consecutive subaddresses. This feature is called Auto-Increment (AI) of the subaddress and enables a quick initialization by the master.
The subaddress pointer will wrap around from 7 to 0.
The subaddresses are given as follows:

SC	SB	SA	sub-address	function
0	0	0	00	control register
0	0	1	01	digit 1
0	1	0	02	digit 2
0	1	1	03	digit 3
1	0	0	04	digit 4
1	0	1	05	reserved, not used
1	1	0	06	
1	1	1	07	

Control bits (see Fig. 4)

The control bits C0 to C6 have the following meaning:

C0 = 0	static mode, i.e. continuous display of digits 1 and 2
C0 = 1	dynamic mode, i.e. alternating display of digit 1 + 3 and 2 + 4
C1 = 0/1	digits 1 + 3 are blanked/not blanked
C2 = 0/1	digits 2 + 4 are blanked/not blanked
C3 = 1	all segment outputs are switched-on for segment test*
C4 = 1	adds 3 mA to segment output current
C5 = 1	adds 6 mA to segment output current
C6 = 1	adds 12 mA to segment output current

Data

A segment is switched ON if the corresponding data bit is logic 1. Data bits D17 to D10 correspond with digit 1, D27 to D20 with digit 2, D37 to D30 with digit 3 and D47 to D40 with digit 4.
The MSBs correspond with outputs P8 and P16, the LSBs with P1 and P9. Digit numbers 1 to 4 are equal to their subaddresses (hex) 1 to 4.

* At a current determined by C4, C5 and C6.

SDA, SCL

The SDA and SCL I/O meet the I²C bus specification. For protection against positive voltage pulses on these inputs voltage regulator diodes are connected to V_{EE}. This means that normal line voltage should not exceed 5,5 volt. Data will be latched on the positive-going edge of the acknowledge related clock pulse.

Power-on reset

The power-on reset signal is generated internally and sets all bits to zero, resulting in a completely blanked display. Only the POWER RESET flag is set.

External Control (C_{EXT})

With a capacitor connected to pin 2 the multiplex frequency can be set (see Fig. 5). When static this pin can be connected to V_{EE} or V_{CC} or left floating since the oscillator will be switched off.

Segment outputs

The segment outputs P1 to P16 are controllable current-sink sources. They are switched on by the corresponding data bits and their current is adjusted by control bits C4, C5 and C6.

Multiplex outputs

The multiplex outputs MX1 and MX2 are switched alternately in dynamic mode with a frequency derived from the clock-oscillator. In static mode MX1 is switched on. The outputs consist of an emitter-follower, which can be used to drive the common anodes of two displays directly provided that the total power dissipation of the circuit is not exceeded. If this occurs external transistors should be connected to pins 11 and 14 as shown in Fig. 5.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 13)		V_{CC}	−0,5	18	V
Supply current (pin 13)		I_{CC}	−50	200	mA
Total power dissipation SOT-101 24-lead DIL		P_{tot}		1000	mW
SDA, SCL voltages		$V_{23,\ 24\text{-}12}$	−0,5	5,9	V
Voltages A0-MX1 and MX2-P16		$V_{1\text{-}11,\ V14\text{-}22}$	−0,5	V_{CC} + 0,5	V
Input/output current all pins	outputs OFF	± I	−	10	mA
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−65	+ 125	°C

THERMAL RESISTANCE

From crystal to ambient
24-lead DIL $R_{th\ cr\text{-}a}$ 35 K/W

CHARACTERISTICS

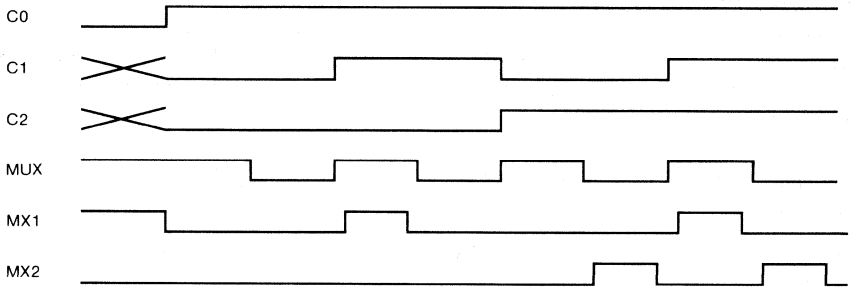
V_{CC} = 5 V; T_{amb} = 25 °C; voltages are referenced to ground (V_{EE} = 0 V); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 13)		V_{CC}	4,5	5,0	15	V
Supply current	all outputs OFF V_{CC} = 5 V	I_{CC}	7,0	9,5	14,0	mA
Power dissipation	all outputs OFF	P_d	–	50	–	mW
SDA; SCL bus (pins 23 and 24)						
Input voltages		$V_{23,24}$	0	–	5,5	V
Logic input voltage LOW		$V_{IL(L)}$	–	–	1,5	V
Logic input voltage HIGH		$V_{IH(L)}$	3,0	–	–	V
Input current LOW	$V_{23,24} = V_{EE}$	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{23,24} = V_{CC}$	I_{IH}	–	–	10	μA
SDA						
Logic output voltage LOW	I_O = 3 mA	$V_{OL(L)}$	–	–	0,4	V
Output sink current		I_O	3	–	–	mA
Address input (pin 1)						
Input voltage programmable address bits:						
A0 = 0; A1 = 0		V_1	V_{EE}	–	$3/16V_{CC}$	V
A0 = 1; A1 = 0		V_1	$5/16V_{CC}$	$3/8V_{CC}$	$7/16V_{CC}$	V
A0 = 0; A1 = 1		V_1	$9/16V_{CC}$	$5/8V_{CC}$	$11/16V_{CC}$	V
A0 = 1; A1 = 1		V_1	$13/16V_{CC}$	–	V_{CC}	V
Input current LOW	$V_1 = V_{EE}$	I_1	–	–	−10	μA
Input current HIGH	$V_1 = V_{CC}$	I_1	–	–	10	
External control (C_{EXT}) pin 2						
Switching level input						
Input voltage LOW		V_{IL}	–	–	V_{CC}−2,5	V
Input voltage HIGH		V_{IH}	V_{CC}−1,5	–	–	V
nput current	V_2 = 2 V	I_2	−140	−160	−180	μA
	V_2 = 4 V	I_2	140	160	180	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Segment outputs (P8 to P1; pins 3 to 10) (P9 to P16; pins 15 to 22)						
Output voltages	I_O = 15 mA	V_O	–	–	0,5	V
Output current HIGH	$V_O = V_{CC}$ = 15 V	I_O	–	–	± 10	μA
Output current LOW control bits HIGH C4, C5 and C6	V_O = 5 V	I_O	17,85	21	25	mA
Contribution of:						
control bit C4		I_O	2,55	3,0	4,0	mA
control bit C5		I_O	5,1	6,0	7,0	mA
control bit C6		I_O	10,2	12,0	14,0	mA
Relative segment 1 output accuracy with respect to highest value when:						
I_3 to I_{10} and I_{15} to I_{22} = 3 mA		ΔI_O	–	–	5	%
I_3 to I_{10} and I_{15} to I_{22} = 21 mA		ΔI_O	–	–	7	%
Multiplex 1 and 2 (pins 11 and 14)						
Output voltage (when ON)	I_O = 50 mA	V_O	V_{CC} 1,5	–	–	V
Output current HIGH (when ON)	V_O = 2 V	$I_{11}; I_{14}$	50	–	*	mA
Output current LOW (when OFF)	V_O = 2 V	$-I_{11}; -I_{14}$	50	70	100	mA
Output period	$C_{2\text{-}12}$ = 2,7 nF	T_{MPX}	5	–	10	ms
	$C_{2\text{-}12}$ = 820 pF	T_{MPX}	–	1,25	–	ms
	$C_{2\text{-}12}$ = 390 pF	T_{MPX}	–	666	–	μs
Output duty factor			48,4	–	–	%

* Value to be fixed.



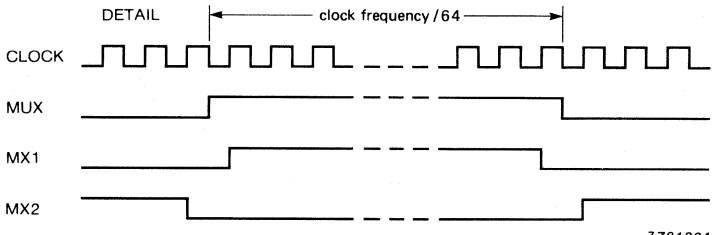


Fig. 4 Timing diagram.

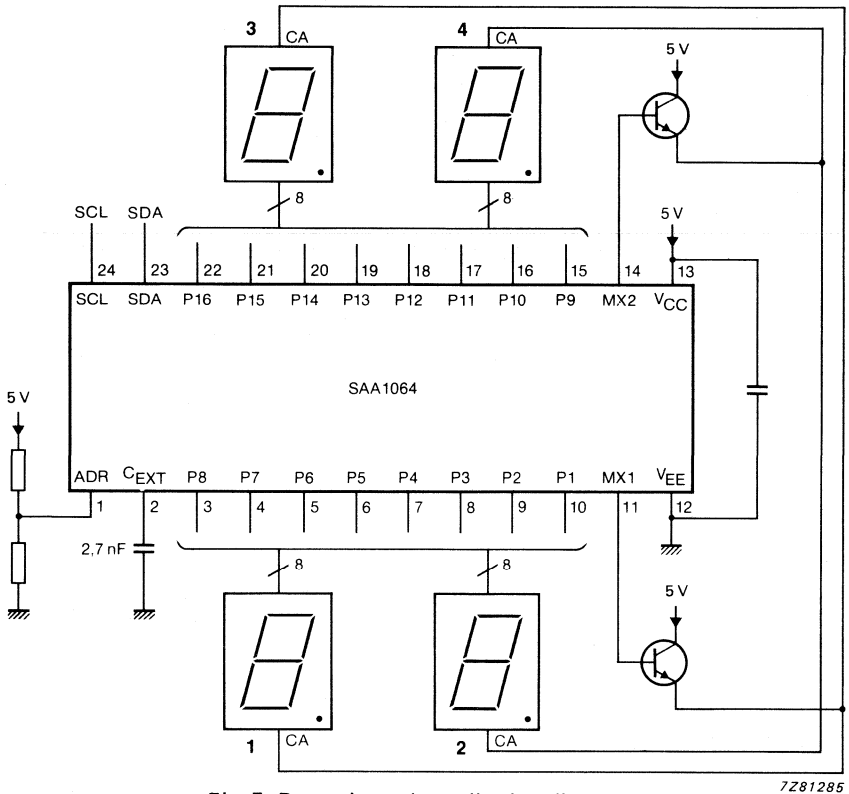


Fig. 5 Dynamic mode application diagram.

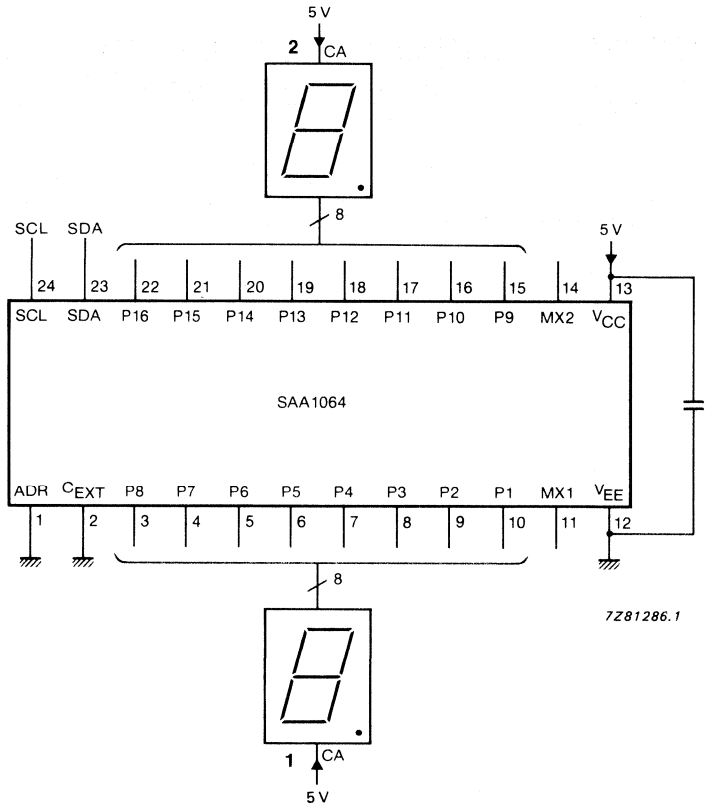


Fig. 6 Static mode application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

MICROPROCESSOR CONTROLLED STEREO SOUND GENERATOR FOR SOUND EFFECTS AND MUSIC SYNTHESIS

GENERAL DESCRIPTION

The SAA1099 is a monolithic integrated circuit designed for generation of stereo sound effects and music synthesis.

Features

- Six frequency generators
  - eight octaves per generator
  - 256 tones per octave
- Two noise generators
- Six noise/frequency mixers
- Twelve amplitude controllers
- Two envelope controllers
- Two 6-channel mixers/current sink analogue output stages
- TTL input compatible
- Readily interfaces to 8-bit microcontroller
- Minimal peripheral components
- Simple output filtering

Applications

- Consumer games systems
- Home computers
- Electronic organs
- Arcade games
- Toys
- Chimes/alarm clocks

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_{DD}	typ.	5 V
Supply current (pin 18)	I_{DD}	typ.	70 mA
Reference current (pin 6)	I_{ref}	typ.	250 μA
Total power dissipation	P_{tot}		500 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102M).

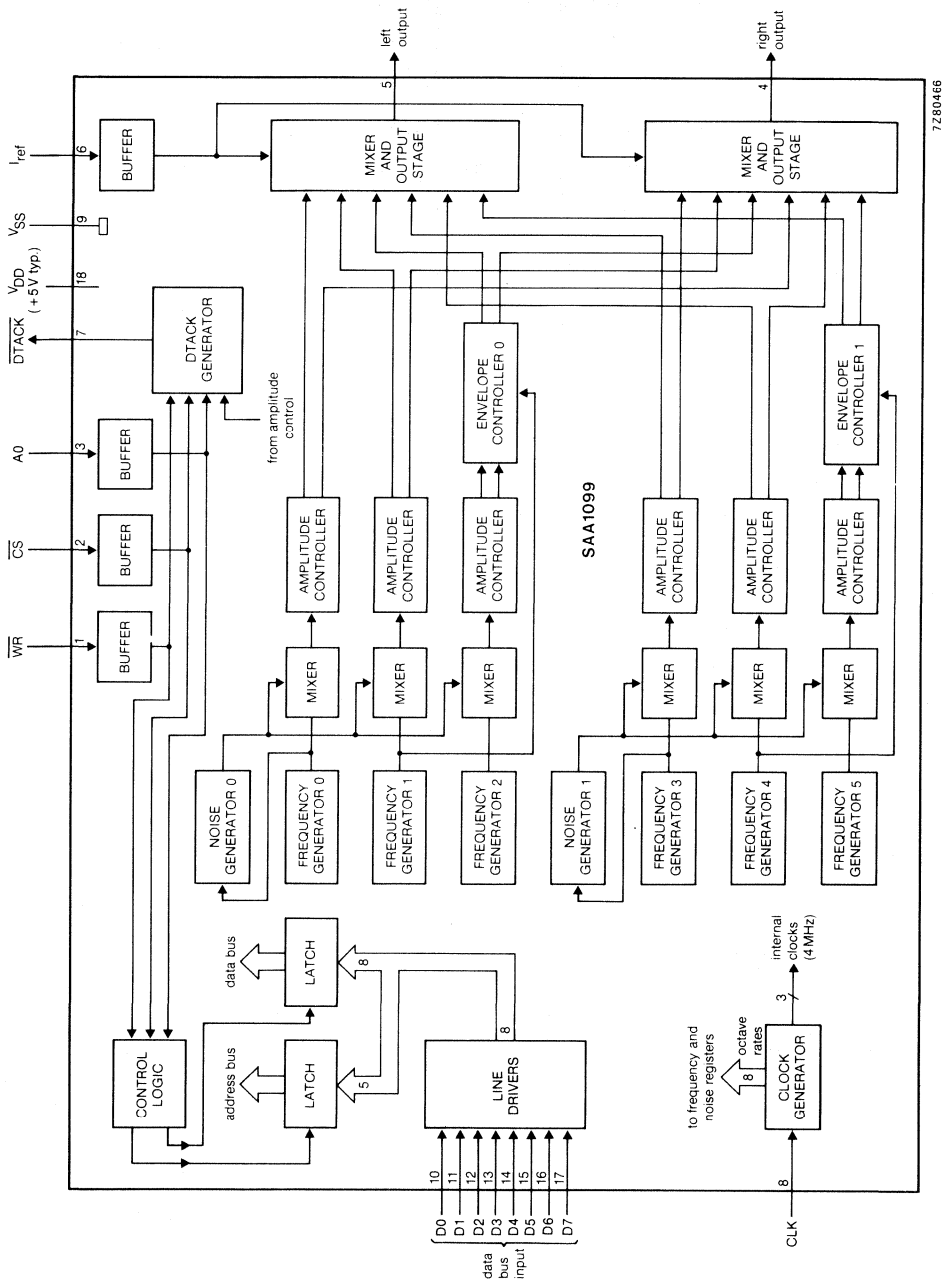


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

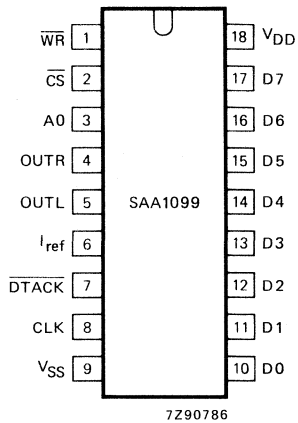


Fig. 2 Pinning diagram.

PIN DESIGNATION

1	$\overline{WR}$	**Write Enable**: active LOW input which operates in conjunction with $\overline{CS}$ and A0 to allow writing to the internal registers.
2	$\overline{CS}$	**Chip Select**: active LOW input to identify valid $\overline{WR}$ inputs to the chip. This input also operates in conjunction with $\overline{WR}$ and A0 to allow writing to the internal registers.
3	A0	**Control/Address select**: input used in conjunction with $\overline{WR}$ and $\overline{CS}$ to load data to the control register (A0 = 0) or the address buffer (A0 = 1).
4	OUTR	**Right channel output**: a 7-level current sink analogue output for the 'right' component. This pin requires an external load resistor.
5	OUTL	**Left channel output**: a 7-level current sink analogue output for the 'left' component. This pin requires an external load resistor.
6	I_{ref}	**Reference current supply**: used to bias the current sink outputs.
7	$\overline{DTACK}$	**Data Transfer Acknowledge**: open drain output, active LOW to acknowledge successful data transfer. On completion of the cycle $\overline{DTACK}$ is set to inactive.
8	CLK	**Clock**: input for an externally generated clock at a nominal frequency of 8 MHz.
9	V_{SS}	**Ground**: 0 V.
10-17	D0-D7	**Data**: Data bus input.
18	V_{DD}	**Power supply**: + 5 V typical.

FUNCTIONAL DESCRIPTION

The following sections provide a detailed functional description of the SAA1099 as shown in the block diagram, Fig. 1.

Frequency generators

Six frequency generators can each select one of 8 octaves and one of 256 tones within an octave. A total frequency range of 31 Hz to 7,81 kHz is available. The outputs may also control noise or envelope generators. All frequency generators have an enable bit which switches them on and off, making it possible to preselect a tone and to make it inaudible when required. The frequency generators may be synchronized using the frequency reset bit.

The frequency ranges per octave are:

Octave	Frequency range
0	31 Hz to 61 Hz
1	61 Hz to 122 Hz
2	122 Hz to 244 Hz
3	245 Hz to 488 Hz
4	489 Hz to 977 Hz
5	978 Hz to 1,95 kHz
6	1,96 kHz to 3,91 kHz
7	3,91 kHz to 7,81 kHz

Noise generators

The two noise generators both have a programmable output. This may be a software controlled noise via one of the frequency controlled generators or one of three pre-defined noises. There is no tone produced by the frequency generator when it is controlling the noise generator. The noise produced is based on double the frequency generator output, i.e. a range of 61 Hz to 15,6 kHz.

In the event of a pre-defined noise being chosen, the output of noise generator 0 can be mixed with frequency generator 0, 1 and 2; and the output of noise generator 1 can be mixed with frequency generator 3, 4 and 5. In order to produce an equal level of noise and tone outputs (when both are mixed) the amplitude of the tone is increased. The three pre-defined noises are based on a clock frequency of 7,8 kHz, 15,6 kHz or 31,25 kHz.

Noise/frequency mixers

Six noise/frequency mixers each with four selections

- Channel off
- Frequency only
- Noise only
- Noise and frequency

Each mixer channel has one of the frequency generator outputs fed to it, three channels use noise generator 0 and the other three use noise generator 1.

Amplitude controllers

Each of the six channel outputs from the mixer is split up into a right and left component giving effectively twelve amplitude controllers. An amplitude of 16 possible levels is assigned to each of the twelve signals. With this configuration a stereo effect can be achieved by varying only the amplitude component. The moving of a sound from one channel to the other requires, per tone, only one update of the amplitude register contents.

When an envelope generator is used, the amplitude levels are restricted. The number of levels available is then reduced to eight. This is achieved by disabling the least significant bit (LSB) of the amplitude control.

Envelope controllers

Two of the six tone generators are under envelope control. This applies to both the left and right outputs from the tone generator.
The envelope has the following eight possible modes:

- Amplitude is zero
- Single attack
- Single decay
- Single attack-decay (triangular)
- Maximum amplitude
- Continuous attack
- Continuous decay
- Continuous attack-decay

The timing of the envelope controllers is programmable using one of the frequency generators (see Fig. 1). When the envelope mode is selected for a channel its control resolution is halved for that channel from 16 levels to 8 levels by rounding down to the nearest even level.
There is also the capability of controlling the 'right' component of the channel with inverse of the 'left' component, which remains as programmed.

A direct enable permits the start of an envelope to be defined, and also allows termination of an envelope at any time. The envelope rate may be controlled by a frequency channel (see Fig. 1), or by the microprocessor writing to the address buffer register. If the frequency channel controlled is OFF (NE = FE = 0) the envelope will appear at the output, which provides an alternative 'non-square' tone capability. In this event the frequency will be the envelope rate, which provided the rate is from the frequency channel, will be a maximum of 1 kHz. Higher frequencies of up to 2 kHz can be obtained by the envelope resolution being halved from 16 levels to 8 levels. Rates quoted are based on the input of a 8 MHz clock.

Six-channel mixers/current sink analogue output stages

Six channels are mixed together by the two mixers allowing each one to control one of six equally weighted current sinks, to provide a seven level analogue output.

Command/control select

In order to simplify the microprocessor interface the command and control information is multiplexed. To select a register in order to control frequencies, amplitudes, etc. the command-register has to be loaded. The contents of this register determines to which register the data is written in the next control-cycle. If a continuous update of the control-register is necessary, only the control-information has to be written (the command-information does not change).
If the command/control select (A0) is logic 0, the byte transfer is control; if A0 is logic 1, the byte transfer is command.

Interface to microprocessor

The SAA1099 is a data bus based I/O peripheral. Depending on the value of the command/control signal (A0) the $\overline{CS}$ and $\overline{WR}$ signals control the data transfer from the microprocessor to the SAA1099. The data-transfer-acknowledge ($\overline{DTACK}$) indicates that the data transfer is completed. When, during the write cycle, the microprocessor recognizes the $\overline{DTACK}$, the bus cycle will be completed by the processor.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_{DD}	−0,3 to	+ 7,5	V
Maximum input voltage	V_I	−0,3 to	+ 7,5	V
at V_{DD} = 4,5 to 5,5 V	V_I	−0,5 to	+ 7,5	V
Maximum output current	I_O	max.	10	mA
Total power dissipation	P_{tot}		500	mW
Storage temperature range	T_{stg}	−55 to	+ 125	°C
Operating ambient temperature range	T_{amb}	0 to	+ 70	°C
Electrostatic handling*	V_{es}	−1000 to	+ 1000	V

* Equivalent to discharging a 250 μF capacitor through a 1 kΩ series resistor.

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	70	100	mA
Reference current (note 1)	I_{ref}	100	250	400	μA
INPUTS					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	−0,5	–	0,8	V
Input leakage current	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	10	pF
OUTPUTS					
$\overline{DTACK}$ (open drain; note 2)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Voltage on pin 7 (OFF state)	V_{7-9}	−0,3	–	6,0	V
Output capacitance (OFF state)	C_O	–	–	10	pF
Load capacitance	C_L	–	–	150	pF
Output leakage current (OFF state)	$-I_{LO}$	–	–	10	μA
Audio outputs (pins 4 and 5)					
With fixed I_{ref} (note 3)					
One channel on	I_{01}/I_{ref}	90	–	120	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	110	%
With I_{ref} = 250 μA; R_L = 1,5 kΩ (± 5%)					
One channel on	I_{01}/I_{ref}	90	–	110	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	105	%
Output current one channel on	I_{01}	225	–	275	μA
Output current six channels on	I_{06}	1,3	–	1,6	mA
With resistor supplying I_{ref} (note 4)					
Output current one channel on	I_{01}	150	–	350	μA
Output current six channels on	I_{06}	0,9	–	1,9	mA
Load resistance	R_L	600	–	–	Ω
D.C. leakage current all channels off	$-I_{LO}$	–	–	10	μA
Maximum current difference between left and right current sinks (note 5)	$\pm I_{Omax}$	–	–	15	%
Signal-to-noise ratio (note 6)	S/N	–	tbf	–	dB

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; timing measurements taken at 2,0 V for a logic 1 and 0,8 V for a logic 0 unless otherwise specified (see waveforms Figs 3 and 4)

parameter	symbol	min.	typ.	max.	unit
Bus interface timing (see Fig. 3)					
A0 set-up time to $\overline{CS}$ fall	t_{ASC}	0	–	–	ns
$\overline{CS}$ LOW to $\overline{WR}$ fall	t_{CSW}	30	–	–	ns
A0 set-up time to $\overline{WR}$ fall	t_{ASW}	50	–	–	ns
$\overline{WR}$ LOW time	t_{WL}	100	–	–	ns
Data bus valid to $\overline{WR}$ rise	t_{BSW}	100	–	–	ns
$\overline{DTACK}$ fall delay from $\overline{WR}$ fall (note 7)	t_{DFW}	0	–	85	ns
A0 hold time from $\overline{WR}$ HIGH	t_{AHW}	0	–	–	ns
$\overline{CS}$ hold time from $\overline{WR}$ HIGH	t_{CHW}	0	–	–	ns
Data bus hold time from $\overline{WR}$ HIGH	t_{DHW}	0	–	–	ns
$\overline{DTACK}$ rise delay from $\overline{WR}$ HIGH	t_{DRW}	0	–	100	ns
Bus cycle time (note 8)	t_{CY}	$4t_{CLK}$	–	–	
Bus cycle time (note 9)	t_{CY}	$16t_{CLK}$	–	–	
Clock input timing (see Fig. 4)					
Clock period	t_{CLK}	120	125	255	ns
Clock LOW time	t_{LOW}	55	–	–	ns
Clock HIGH time	t_{HIGH}	55	–	–	ns

Notes to the characteristics

1. Using an external constant current generator to provide a nominal I_{ref} or external resistor connected to V_{DD}.
2. This output is short-circuit protected to V_{DD} and V_{SS}.
3. Measured with I_{ref} a constant value between 100 and 400 μA; load resistance (R_L) allowed to match E12 (5%) in all applications via:

$$R_L = 0{,}6\ [I_{ref}]^{-1} - 16\ [I_{ref}]^{-0{,}5} \pm 12\%$$

4. Measured with R_{ref} = 10 kΩ (± 5%) connected between I_{ref} and V_{DD}; R_L = 1,5 kΩ (± 5%); OUTR and OUTL short-circuit protected to V_{SS}.
5. Left and right outputs must be driven with identical configuration.
6. Sample tested value only.
7. This timing parameter only applies when no wait states are required; otherwise parameter is invalid.
8. The minimum bus cycle time of four clock periods is for loading all registers except the amplitude registers.
9. The minimum bus cycle time of 16 clock periods is for loading the amplitude registers. In a system using $\overline{DTACK}$ it is possible to achieve minimum times of 500 ns. Without $\overline{DTACK}$ the parameter given must be used.

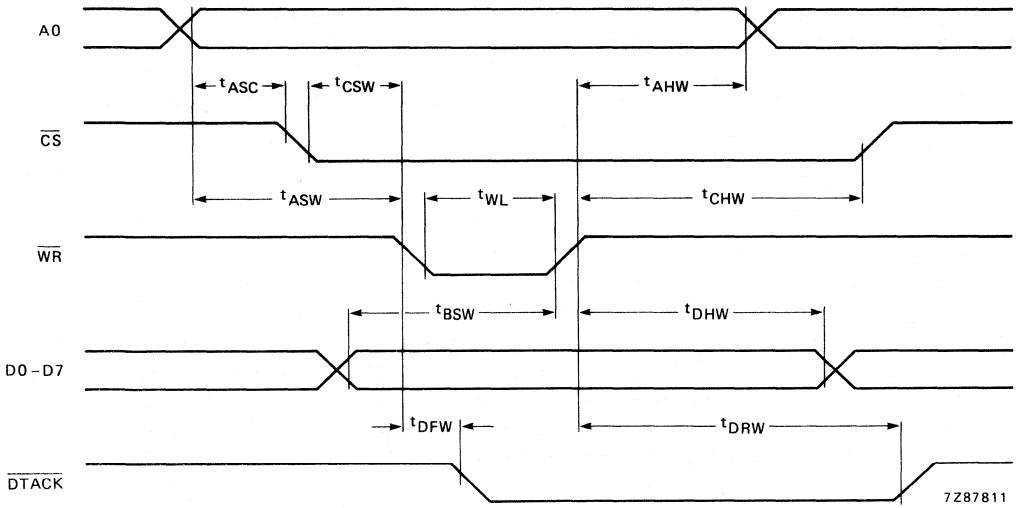


Fig. 3 Bus interface waveforms.

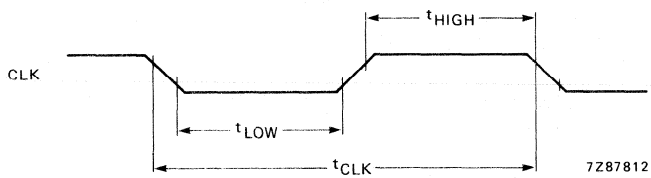


Fig. 4 Clock input waveform.

DEVELOPMENT DATA

APPLICATION INFORMATION

Device operation

The SAA1099 uses pulse width modulation to achieve amplitude and envelope levels. The twelve signals are mixed in an analogue format (6 'left' and 6 'right') before leaving the chip. The amplitude and envelope signals chop the output at a minimum rate of 62,5 kHz, compared with the highest tone output of 7,81 kHz. Simple external low-pass filtering is used to remove the high frequency components.

Rates quoted are based on the input of a 8 MHz clock.

A data bus based write only structure is used to load the on-board registers. The data bus is used to load the address for a register, and subsequently the data to that register. Once the address is loaded multiple data loads to that register can be performed.

The selection of address or data is made by the single address bit A0, as shown in register maps Table 1 and Table 2.

The bus control signals $\overline{WR}$ and $\overline{CS}$ are designed to be compatible with a wide range of microprocessors, a $\overline{DTACK}$ output is included to optimise the interface with an S68000 series microprocessor. In most bus cycles $\overline{DTACK}$ will be returned immediately, this applies to all register address load cycles and all except amplitude data load cycles. With respect to amplitude data, a number of wait cycles may need to be performed, depending on the time since the previous amplitude load. $\overline{DTACK}$ will indicate the number of required waits.

Register description (see Tables 2 and 3)

The amplitudes are assigned with 'left' and 'right' components in the same byte, on a channel by channel basis. The spare locations that are left between blocks of registers is to allow for future expansion, and should be written as zero's. The tone within an octave is defined by eight bits and the octave by three bits. Note that octaves are paired (0/1, 2/3 etc.). The frequency and noise enables are grouped together for ease of programming. The controls for noise 'colour' (clock rate) are grouped in one byte.

The envelope registers are positioned in adjacent locations. There are two types of envelope controls, direct acting controls and buffered controls. The direct acting controls always take immediate effect, and are:

- Envelope enable (reset)
- Envelope resolution (16/8 level)

The buffered controls are acted upon only at the times shown in Fig. 5 and control selection of:

- Envelope clock source
- Waveform type
- Inverted/non-inverted 'right' component

Table 1 External memory map

select	data bus inputs								operations
A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	D7	D6	D5	D4	D3	D2	D1	D0	data for internal registers
1	X	X	X	A4	A3	A2	A1	A0	internal register address

Where X = don't care state.

Table 2 Internal register map

register address	data bus inputs D7	D6	D5	D4	D3	D2	D1	D0	operations
00	AR03	AR02	AR01	AR00	AL03	AL02	AL01	AL00	amplitude 0 right channel; left channel
01	1	1	1	1	1	1	1	1	amplitude 1 right/left
02	2	2	2	2	2	2	2	2	amplitude 2 right/left
03	3	3	3	3	3	3	3	3	amplitude 3 right/left
04	4	4	4	4	4	4	4	4	amplitude 4 right/left
05	5	5	5	5	5	5	5	5	amplitude 5 right/left
06	X	X	X	X	X	X	X	X	
07	X	X	X	X	X	X	X	X	
08	F07	F06	F05	F04	F03	F02	F01	F00	frequency of tone 0
09	1	1	1	1	1	1	1	1	frequency of tone 1
0A	2	2	2	2	2	2	2	2	frequency of tone 2
0B	3	3	3	3	3	3	3	3	frequency of tone 3
0C	4	4	4	4	4	4	4	4	frequency of tone 4
0D	F57	F56	F55	F54	F53	F52	F51	F50	frequency of tone 5
0E	X	X	X	X	X	X	X	X	
0F	X	X	X	X	X	X	X	X	
10	X	012	011	010	X	002	001	000	octave 1; octave 0
11	X	032	031	030	X	022	021	020	octave 3; octave 2
12	X	052	051	050	X	042	041	040	octave 5; octave 4
13	X	X	X	X	X	X	X	X	
14	X	X	FE5	FE4	FE3	FE2	FE1	FE0	frequency enable
15	X	X	NE5	NE4	NE3	NE2	NE1	NE0	noise enable
16	X	X	N11	N10	X	X	N01	N00	noise generator 1; noise generator 0
17	X	X	X	X	X	X	X	X	
18	E07	X	E05	E04	E03	E02	E01	E00	envelope generator 0
19	E17	X	E15	E14	E13	E12	E11	E10	envelope generator 1
1A	X	X	X	X	X	X	X	X	
1B	X	X	X	X	X	X	X	X	
1C	X	X	X	X	X	X	RST	SE	frequency reset (all channels) sound enable (all channels)
1D	X	X	X	X	X	X	X	X	
1E	X	X	X	X	X	X	X	X	
1F	X	X	X	X	X	X	X	X	

Where:
All don't cares (X) should be written as zero's.
00 to 1F block of registers repeats eight times in the block between addresses 00 to FF (full internal memory map).

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Table 3 Register description

bit	description
ARn3; ARn2; ARn1; ARn0 (n = 0,5)	4 bits for amplitude control of right channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
ALn3; ALn2; ALn1; ALn0 (n = 0,5)	4 bits for amplitude control of left channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
Fn7 to Fn0 (n = 0,5)	8 bits for frequency control of the six frequency generators 0 0 0 0 0 0 0 0 lowest frequency 1 1 1 1 1 1 1 1 highest frequency
On2; On1; On0 (n = 0,5)	3 bits for octave control 0 0 0 lowest octave (31 Hz to 61 Hz) 0 0 1 (61 Hz to 122 Hz) 0 1 0 (122 Hz to 244 Hz) 0 1 1 (245 Hz to 488 Hz) 1 0 0 (489 Hz to 977 Hz) 1 0 1 (978 Hz to 1,95 kHz) 1 1 0 (1,96 kHz to 3,91 kHz) 1 1 1 highest octave (3,91 kHz to 7,81 kHz)
FEn (n = 0,5)	frequency enable bit (one tone per generator) FEn = 0 indicates that frequency 'n' is off
NEn (n = 0,5)	noise enable bit (one tone per generator) NEn = 0 indicates that noise 'n' is off
Nn1; Nn0 (n = 0,1)	2 bits for noise generator control. These bits select the noise generator rate (noise 'colour') Nn1 Nn0 clock frequency 0 0 31,3 kHz 0 1 15,6 kHz 1 0 7,6 kHz 1 1 61 Hz to 15,6 kHz (frequency generator 0/3)

bit	description
En7; En5 to En0 (n = 0,1)	7 bits for envelope control En0 0 left and right component have the same envelope 1 right component has inverse of envelope that is applied to left component En3 En2 En1 0 0 0 zero amplitude 0 0 1 maximum amplitude 0 1 0 single decay 0 1 1 repetitive decay 1 0 0 single triangular 1 0 1 repetitive triangular 1 1 0 single attack 1 1 1 repetitive attack En4 0 4 bits for envelope control (maximum frequency = 977 Hz) 1 3 bits for envelope control (maximum frequency = 1,95 kHz) En5 0 internal envelope clock (frequency generator 1 or 4) 1 external envelope clock (address write pulse) En7 0 reset (no envelope control) 1 envelope control enabled
SE	SE sound enable for all channels (reset on power-up to 0) 0 all channels disabled 1 all channels enabled
RST	Reset signal to all frequency generators 0 all generators enabled 1 all generators reset and synchronized

Note

All rates given are based on the input of a 8 MHz clock.

APPLICATION INFORMATION (continued)

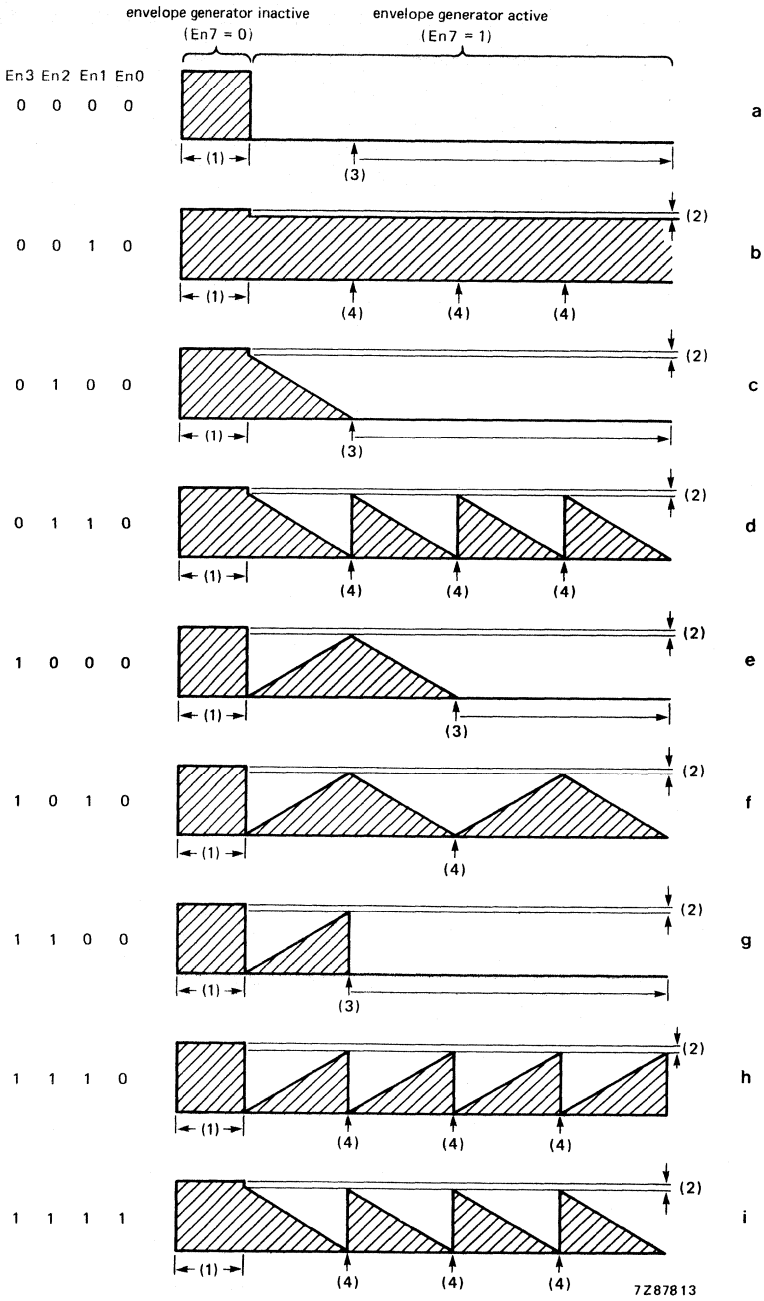


Fig. 5 Envelope waveforms.

DEVELOPMENT DATA

Notes to Fig. 5

(1) The level at this time is under amplitude control only (En7 = 0; no envelope).

(2) When the generator is active (En7 = 1) the maximum level possible is 7/8ths of the amplitude level.

(3) After position (3) the buffered controls will be acted upon when loaded.

(4) At positions (4) the buffered controls will be acted upon if already loaded.

(5) Waveforms 'a' to 'h' show the left channel (En0 = 0; left and right components have the same envelope).
Waveform 'i' shows the right channel (En0 = 1; right component inverse of envelope applied to left).

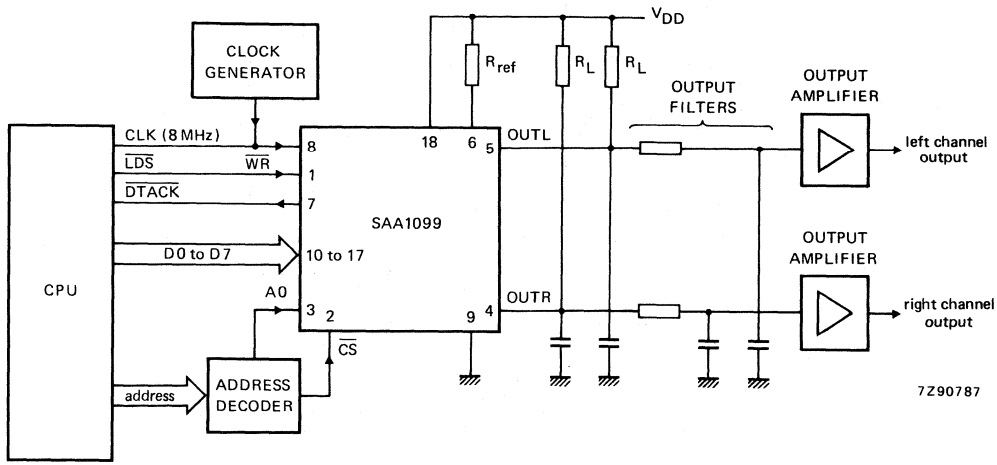


Fig. 6 Typical application circuit diagram.

PCM-AUDIO ERROR-CORRECTOR-1 (ECO-1)

GENERAL DESCRIPTION

The SAA1131 forms part of the error correction system for PCM-audio in 8 mm cassette video recorders. It includes the main timing and control section of the system. Other ICs in the system are the second error-corrector ECO-2 (SAA1132), the analog/digital interface ADI (SAA1133), the ident-word interface IDI (SAA1136) and RAM storage.

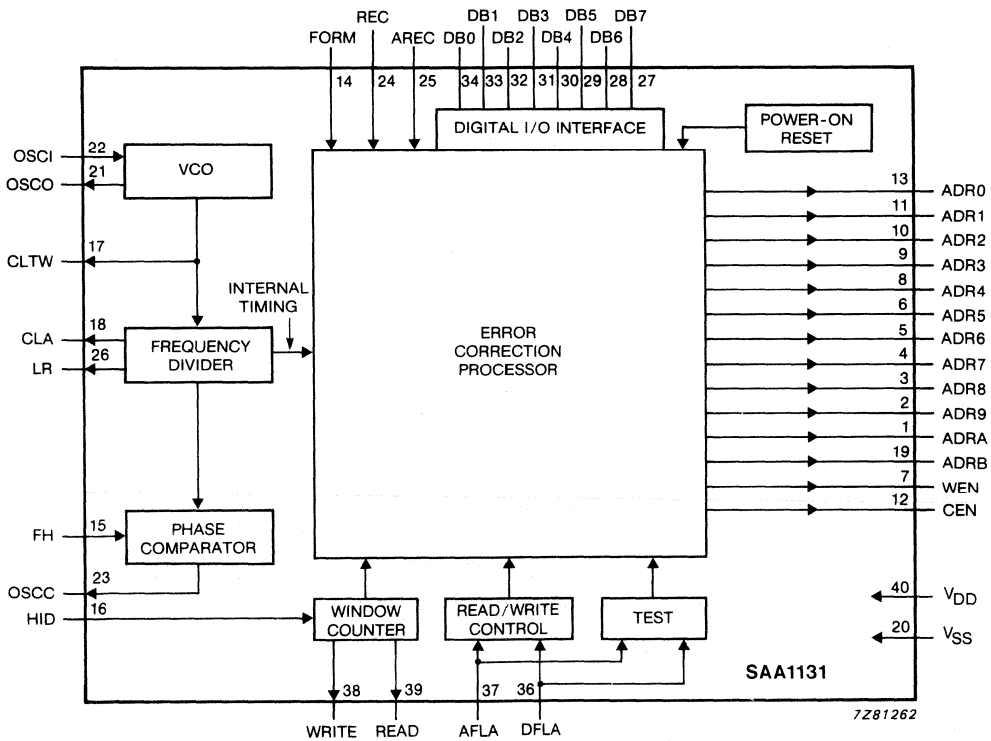


Fig. 1 Block diagram.

PACKAGE OUTLINES

SAA1131P: 40-lead DIL; plastic (SOT-129).
SAA1131T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

PINNING

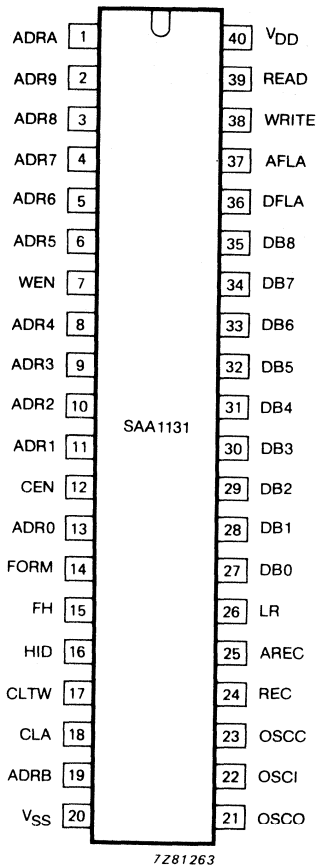


Fig. 2 Pinning diagram.

Power supplies

V_{DD} positive supply voltage (+ 5 V)

V_{SS} ground (0 V)

Inputs (TTL)

FORM format input. Determines system mode: "1" = CCIR, "0" = NTSC

FH line frequency, typ. 15,625 kHz (CCIR) or 15,750 kHz (NTSC)

HID head identification signal, typ. 25 Hz (CCIR) or 30 Hz (NTSC)

REC, AREC mode-select inputs:

AREC	REC	mode
0	0	playback
0	1	record
1	0	special after-record mode
1	1	not allowed

Inputs (CMOS)

OSCI	oscillator input, typ. 11,50 MHz (CCIR) or 11,58 MHz (NTSC)

Input/outputs (TTL-input/3-state push-pull output)

DB0 to DB8	data bus connections, I/O state is determined internally

Input/outputs (CMOS-input/3-state push-pull output)

DFLA and AFLA are 'input' during READ and 'output' during WRITE

DFLA	data present indicator, typ. 720 kHz (CCIR) or 750 kHz (NTSC)
AFLA	READ: first byte indicator WRITE: data output window

Outputs (CMOS push-pull)

ADR0 to ADRA	address outputs to RAMs
WEN	write enable to RAMs
CEN, ADRB	chip enable to RAMs
CLTW	clock to ECO-2, typ. 11,50 MHz (CCIR) or 11,58 MHz (NTSC)
CLA	system clock, typ. 1,44 MHz (CCIR) or 1,45 MHz (NTSC)
OSCO	oscillator output, typ. 11,50 MHz (CCIR) or 11,58 MHz (NTSC)
LR	system data bus control, typ. 31,25 kHz (CCIR) or 31,45 kHz (NTSC) LR HIGH time = LR LOW time = 23 CLA cycles
READ	mode-select to ECO-2, typ. 50 Hz (CCIR) or 60 Hz (NTSC)
WRITE	mode-select to ECO-2, typ. 50 Hz (CCIR) or 60 Hz (NTSC)

Outputs (3-state push-pull)

OSCC	phase comparator output

FUNCTIONAL DESCRIPTION

Timing and control

The VCO is locked to the line frequency (FH) via a divider and phase comparator network. The VCO frequency, divided by 736, is compared with the incoming FH signal and the resulting difference signal fed back via pin OSCC to the external oscillator circuit at pins OSCI, OSCO. The divider circuit provides internal timing signals, system clocks CLA (92FH) and CLTW (736FH) and the audio sample control LR (2FH) for the system data bus.

The RAM-control functions of addressing, enable and write and the system processes of audio sampling, encode, decode, read and write are all synchronized to the HID input (25 or 30 Hz). The start of each process sequence is controlled by a window counter.

The system bus, which performs the data transport in the system, interfaces directly with the I/O pins DB0 to DB8. Data from and to the bus is used internally for the encode/decode process and in the read/write mode the bus is used to transfer an address from or to ECO-2.

The read/write control block communicates with ECO-2 via pins AFLA and DFLA. Under the control of the window counter, AFLA and DFLA are inputs during the read mode and outputs during the write mode.

The system operating modes of playback, record and after-record are selected by the input signals REC and AREC, and that of CCIR or NTSC by the FORM input.

Audio sampling

Audio sampling is a continuous process performed at four times the line frequency. In the recording mode data is transferred from the ADI to one of the RAMs, and in the playback mode from a RAM to the ADI. When 1250 samples (CCIR) or 1050 samples (NTSC) have been written into or read from one RAM the system toggles to another RAM, toggling is synchronized to the rising edge of the HID signal.

Encoding

The encoding process for recording mode is started at a time determined by the window counter and is synchronized by the HID signal. Data is read from a RAM in a predetermined interleaved sequence to generate P and Q parity information. The PQ generator provides 2 parity bytes (P & Q) which are written back to corresponding addresses in the RAM. The process continues until all P and Q bits have been generated but is interrupted for audio sampling.

Decoding

The decoding process for playback mode is also controlled by the window counter and synchronized by the HID signal. Data is read from one RAM and checked for reliability. Erroneous data is replaced with possible error-correction data which is written into the RAM at the 'faulty' locations. The decoding process runs through the data three times before it is automatically stopped. The process is interrupted for audio sampling.

Write

The write process follows encoding of data in the recording mode. Encoded data is transferred from the RAM into ECO-2. Before and after the data transfer a clock-run-in and a clock-run-out cycle is activated; the transfer is controlled by the AFLA and DFLA signals generated in ECO-1. During the write process the WRITE signal is HIGH.

Read

This process is started before the decoding of data in the playback mode. Data collected in ECO-2 is transferred into one of the RAMs. After the read cycle the received data will be corrected, if necessary, during the decoding process. The transfer is controlled by the AFLA and DFLA signals that are now generated in ECO-2. During the read process the READ signal is HIGH making ECO-1 and the RAMs ready to receive data. The process is interrupted for audio sampling.

Ident-words

The system can be upgraded for ID-words by the inclusion of IDI (SAA1134). The transfers of ident-words (read or write) are controlled by ECO-1 and IDI.

Mode selection for system configuration

System options can include an ident-word interface (IDI, SAA1134) and a 4K x 1-bit flag RAM. To accommodate the particular system configuration, the AFLA and DFLA pins must be pulled HIGH or LOW when they are in the high impedance OFF-state. The pull-up/pull-down resistors are to be 33 kΩ.

condition of pin when in high impedance OFF-state		system includes	
AFLA	DFLA	IDI	flag RAM
LOW	LOW	no	no
HIGH	LOW	yes	no
LOW	HIGH	yes	yes
HIGH	HIGH	not allowed	

Initialization

At power-on all ECO-1 memory elements are reset and the signals READ and WRITE are both HIGH to constitute a reset signal to ECO-2.

Test mode

ECO-1 is put into the test mode when REC and AREC are both HIGH and a pulse is applied to the FORM input. In this condition AFLA and DFLA must be kept at "0" to maintain normal operation.

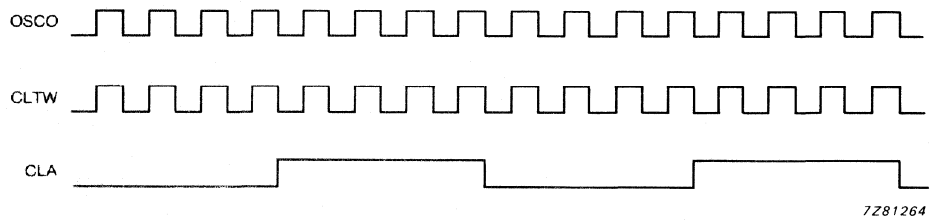


Fig. 3 Relationship between oscillator output (OSCO), clock output to ECO-2 (CLTW) and system clock (CLA).

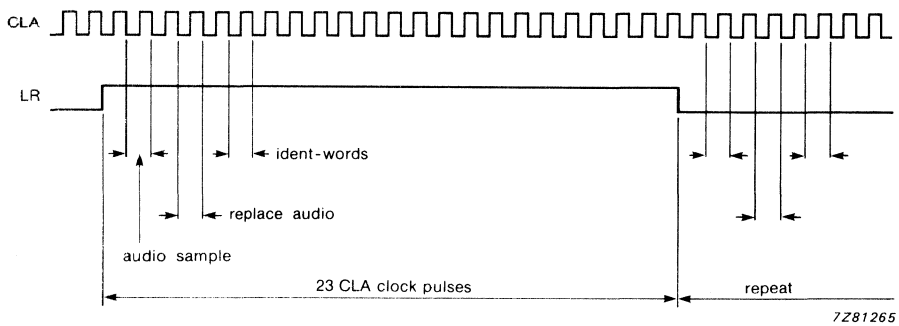


Fig. 4 Relationship between system clock (CLA) and system data bus control (LR).

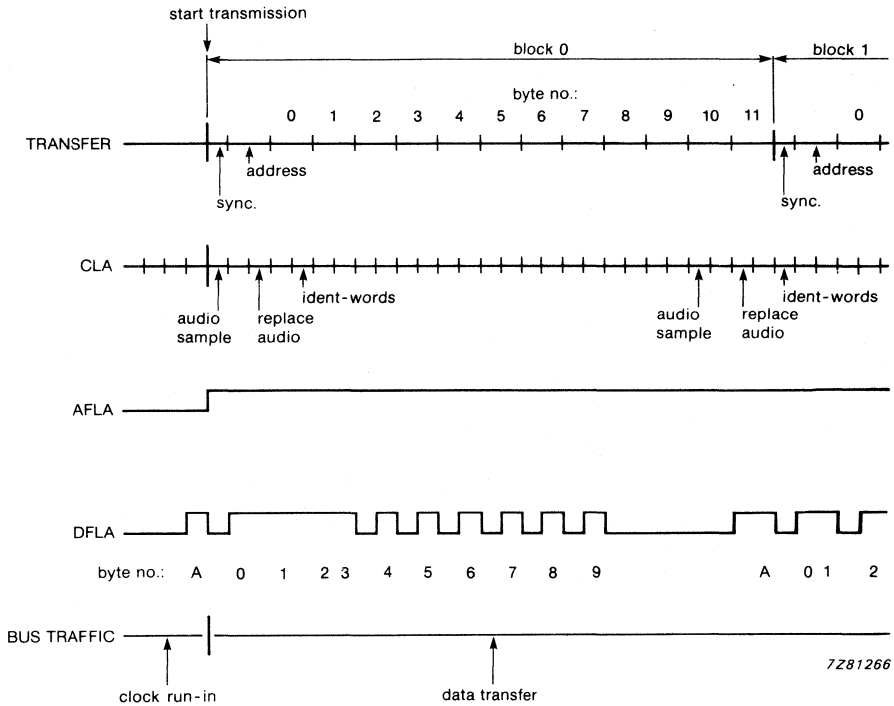


Fig. 5 Data transfer during WRITE from ECO-1 to ECO-2.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	pin 40	$V_{DD} = V_{40-20}$	−0,5	7,0	V
Supply current	pin 40	I_{DD}	–	50	mA
Supply current	pin 20	I_{SS}	–	50	mA
Input voltage range		V_I	−0,5	V_{DD} + 0,5*	V
Input current		I_I	–	± 10	mA
Output current		I_O	–	± 10	mA
Power dissipation per output		P_O	–	70	mW
Total power dissipation	SAA1131P	P_{tot}	–	500	mW
	SAA1131T	P_{tot}	–	300	mW
Storage temperature range		T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

T_{amb} = −20 to + 70 °C; V_{DD} = 4,75 to 5,25 V; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 40	V_{DD}	4,75	5,0	5,25	V
Supply current	pin 40; $V_I = V_{DD}$ or V_{SS} for all inputs; I_O = 0 mA for all outputs	I_{DD}	–	–	100	μA
Input OSCI						
Input voltage HIGH		V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0,3 x V_{DD}	V
Inputs FORM, REC, AREC, HID, FH						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V

* V_{DD} + 0,5 V not to exceed 7,0 V.

parameter	conditions	symbol	min.	typ.	max.	unit
Input/outputs AFLA, DFLA						
Input voltage HIGH		V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0,3 x V_{DD}	V
Output voltage HIGH	$-I_O$ = # mA	V_{OH}	V_{DD} –0,5	–	–	V
Output voltage LOW	$+I_O$ = # mA	V_{OL}	–	–	0,4	V
3-state OFF-state leakage current		V_{OZ}	–	–	10	μA
Input/outputs DB0-DB8						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V
Output voltage HIGH	$-I_{OH}$ = # mA	V_{OH}	V_{DD} –0,5	–	–	V
Output voltage LOW	$+I_{OL}$ = # mA	V_{OL}	–	–	0,4	V
3-state OFF-state leakage current		I_{OZ}	–	–	10	μA
Outputs ADR0-ADRB LR, CEN, WEN, READ, WRITE, CLA, CLTW						
Output voltage HIGH	$-I_{OH}$ = # mA	V_{OH}	V_{DD} –0,5	–	–	V
Output voltage LOW	$+I_{OL}$ = # mA	V_{OL}	–	–	0,4	V
Output OSCO						
Output voltage HIGH	$-I_{OH}$ = # mA	V_{OH}	V_{DD} –0,5	–	–	V
Output voltage LOW	$+I_{OL}$ = # mA	V_{OL}	–	–	0,4	V
Output OSCC						
Output voltage HIGH	$-I_{OH}$ = # mA	V_{OH}	V_{DD} –0,5	–	–	V
Output voltage LOW	$+I_{OL}$ = # mA	V_{OL}	–	–	0,4	V
3-state OFF-state leakage current		I_{OZ}	–	–	10	μA

DEVELOPMENT DATA

Values not yet available.

A.C. CHARACTERISTICS (Fig. 6)

T_{amb} = −20 to + 70 °C; V_{DD} = 4,75 to 5,25 V; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Frequency	pins 21 and 22	f_{OSC}	–	–	12,5	MHz
System clock CLA						
Frequency		f_{CLA}	–	–	2,1	MHz
CLA HIGH time		t_{WH}	200	–	–	ns
CLA LOW time		t_{WL}	200	–	–	ns
Inputs REC, AREC, HID, FH, FORM						
Set-up time		t_{su}	10	–	–	ns
Hold time		t_h	20	–	–	ns
Outputs						
WEN LOW time		t_{WL}	200	–	–	ns
WEN to CEN, ADR0-ADRB output hold time	C_L = 50 pF	t_{OH}	25	–	200	ns
CLA to WEN output delay time	C_L = 50 pF	t_{OD}	10	–	30	ns
CLA to DB0-DB8, AFLA, DFLA, READ, WRITE output delay time	C_L = 50 pF	t_{OD}	20	–	250	ns

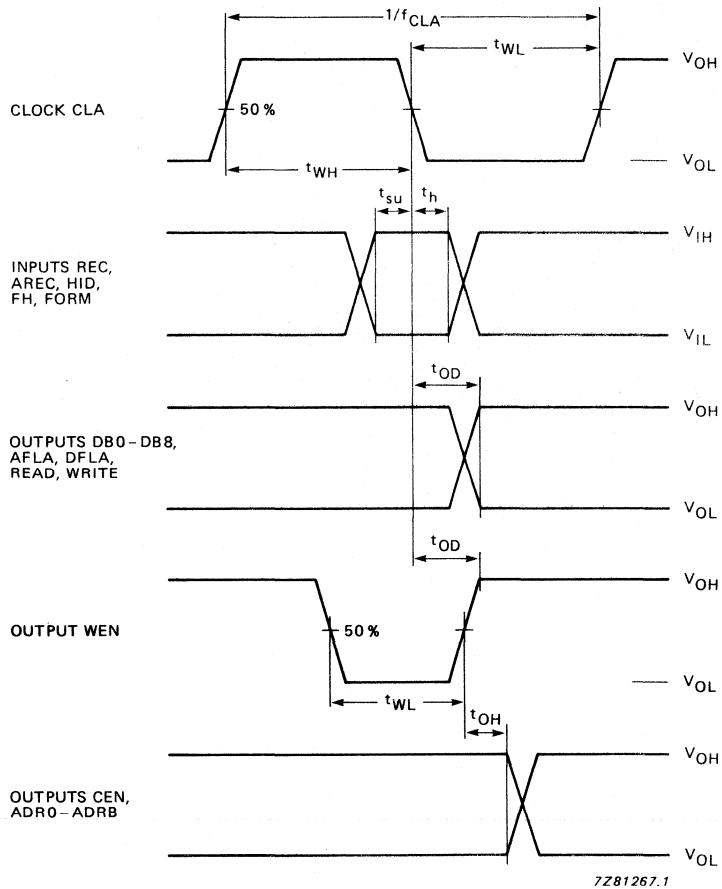


Fig. 6 Waveforms showing the input set-up and hold times, clock (CLA) to output propagation delays and output transition times (all levels are CMOS).

PCM-AUDIO ERROR-CORRECTOR-2 (ECO-2)

GENERAL DESCRIPTION

The SAA1132 forms part of the error correction system for PCM-audio in 8 mm cassette video recorders. It includes the interface between recording tape, the error-corrector ECO-1 (SAA1131) and the system RAMs. Other ICs in the system are the analog/digital interface (SAA1133) and the ident-word interface (SAA1136).

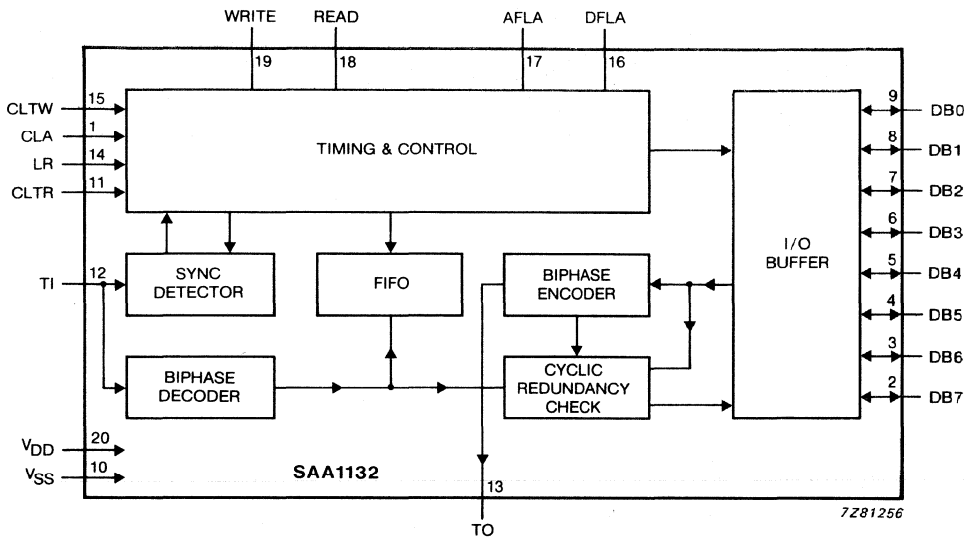


Fig. 1 Block diagram.

PACKAGE OUTLINES

SAA1132P: 20-lead DIL; plastic (SOT-146).
SAA1132T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PINNING

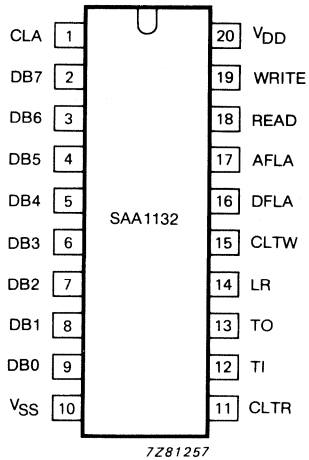


Fig. 2 Pinning diagram.

Power supplies

V_{DD}	positive supply voltage (+ 5 V)
V_{SS}	ground (0 V)

Inputs (TTL)

READ	mode-select input from ECO-1, typ. 50 Hz (CCIR) or 60 Hz (NTSC)
WRITE	mode-select input from ECO-1, typ. 50 Hz (CCIR) or 60 Hz (NTSC)

Inputs (CMOS)

CLA	system clock input from ECO-1, typ. 1,44 MHz (CCIR) or 1,45 MHz (NTSC)
CLTR	clock input derived from tape, typ. 11,50 MHz (CCIR) or 11,58 MHz (NTSC)
TI	data from tape, typ. 5,75 Mbits/s (CCIR) or 5,79 Mbits/s (NTSC)
LR	system data bus control from ECO-1, typ. 31,25 kHz (CCIR) or 31,45 kHz (NTSC)
CLTW	clock from ECO-1, typ. 11,50 MHz (CCIR) or 11,58 MHz (NTSC)

Input/outputs (TTL-input/3-state push-pull output)

DB0 to DB7	data bus connections, 'input' in READ, 'output' in WRITE
DFLA	data present indicator, typ. 720 kHz (CCIR) or 750 kHz (NTSC)
AFLA	READ: first byte indicator WRITE: data output window

Outputs (CMOS push-pull)

TO	data to tape

FUNCTIONAL DESCRIPTION

Write

In the WRITE mode, data is received in byte format from ECO-1 and the RAMs via the data bus and is transferred to the tape in serial format. The control signals for this process are WRITE, AFLA, DFLA and LR with clocks CLTW and CLA where CLTW = 8CLA = 736FH (FH = line frequency).

When WRITE goes HIGH, the output from pin TO comprises logic "1s" in biphase-M format as shown in Fig. 3. The time for data to be fed from the bus to ECO-2 is indicated by the signal DFLA and conditioned by the status of LR (see data sheet SAA1131, ECO-1). The serial output from pin TO is performed when AFLA is HIGH.

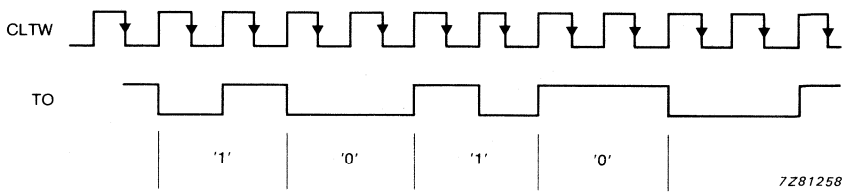


Fig. 3 Biphase-M format.

The circuit generates two check bytes (CRC) during 11 bytes of data, thus one block of information at ECO-2 comprises 3 synchronization bits, 11 data bytes and 2 check bytes. The synchronization format is shown in Fig. 4.

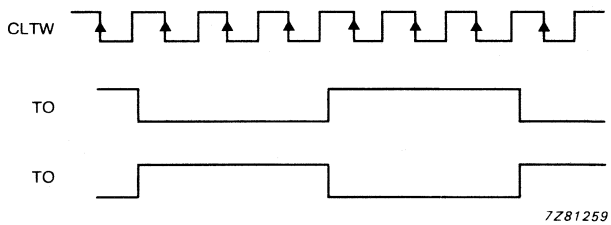


Fig. 4 Synchronization format.

When all blocks of information have been received from the data bus, the signals DFLA and AFLA both go LOW. Following the completion of the serial data transport to the tape, the circuit provides logic "1s" from TO until the WRITE signal goes LOW.

If WRITE and READ are both LOW, the internal clocks are stopped to reduce power consumption.

Note

The condition READ = WRITE = HIGH resets all memory elements except input/output buffers and therefore should be avoided.

FUNCTIONAL DESCRIPTION (continued)

Read

During READ, data is received from the tape in serial format and transferred to ECO-1 and the RAMs in byte format via the data bus. The control signals for this process are READ, AFLA, DFLA and LR with clocks CLTR (derived from data on the tape) and CLA.

When READ is HIGH, tape data is decoded and stored in an internal buffer which can contain a complete block of information. Synchronization of the information is performed using 3 synchronization bits. The circuit generates two check bytes (CRC) during 11 bytes of data from the tape and these are compared with check bytes received from the tape. If the check bytes are equal the data in the buffer is sent to the data bus. The signal DFLA indicates that data is available and AFLA indicates the first byte of the information block (Fig. 5).

Differences between input and output data rates are accommodated by an internal FIFO register. Data transport to the data bus is faster than that from the tape (except when the bus is busy with other processes), also the read-clock CLTR can be faster than the write-clock CLTW. The FIFO assures correct data transport up to a 10% difference in clock rates in all circuit conditions.

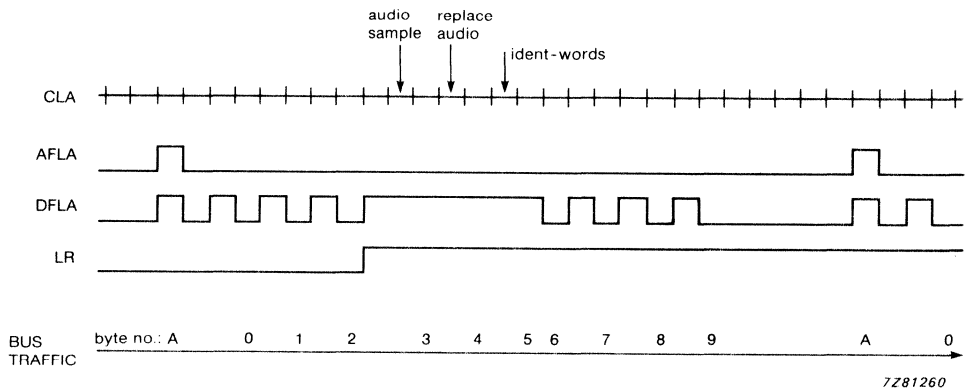


Fig. 5 ECO-2 to ECO-1 data transfer during READ.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	pin 20	$V_{DD} = V_{20-10}$	−0,5	7,0	V
Supply current	pin 20	I_{DD}	–	50	mA
Supply current	pin 10	I_{SS}	–	50	mA
Input voltage range		V_I	−0,5	V_{DD}+0,5*	V
Input current		I_I	–	± 10	mA
Output current		I_O	–	± 10	mA
Power dissipation per output		P_O	–	70	mW
Total power dissipation	SAA1132P	P_{tot}	–	500	mW
	SAA1132T	P_{tot}	–	300	mW
Storage temperature range		T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

T_{amb} = −20 to + 70 °C; V_{DD} = 4,75 to 5,25 V; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 20	V_{DD}	4,75	5,0	5,25	V
Supply current	pin 20; $V_I = V_{DD}$ or V_{SS} for all inputs; I_O = 0 mA for all outputs	I_{DD}	–	–	10	μA
Inputs LR, CLA, CLTR, CLTW, TI						
Input voltage HIGH		V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0,3 x V_{DD}	V
Inputs READ, WRITE						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V

* V_{DD} + 0,5 V not to exceed 7,0 V.

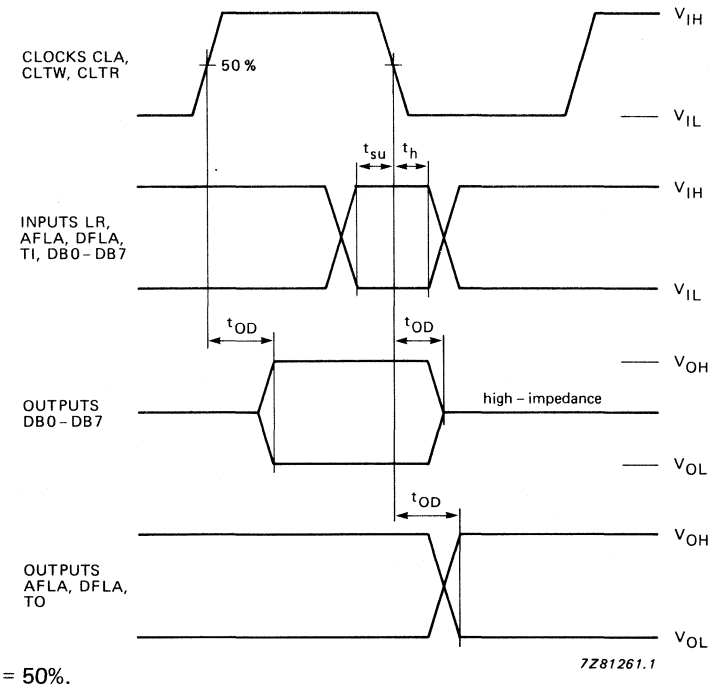
parameter	conditions	symbol	min.	typ.	max.	unit
Input/outputs AFLA, DFLA, DB0 to DB7						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V
Output voltage HIGH	$-I_{OH}$ = 3 mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW	+ I_{OL} = # mA	V_{OL}	–	–	0,4	V
3-state OFF-state leakage current		I_{OZ}	–	–	10	μA
Output TO						
Output voltage HIGH	$-I_{OH}$ = # mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW	+ I_{OL} = # mA	V_{OL}	–	–	0,4	V

A.C. CHARACTERISTICS

T_{amb} = −20 to + 70 °C; V_{DD} = 4,75 to 5,25 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Inputs					
Write clock CLTW frequency	f_{CLTW}	–	–	12,5	MHz
Read clock CTLR frequency	f_{CTLR}	–	–	f_{CLTW} + 10%	
System clock CLA frequency	f_{CLA}	–	–	2,1	MHz
LR, AFLA, DFLA, DB0-DB7, to CLA set-up time	t_{su}	20	–	–	ns
TI to CLTR set-up time	t_{su}	20	–	–	ns
LR, AFLA, DFLA, DB0-DB7, to CLA hold time	t_h	10	–	–	ns
TI to CLTR hold time	t_h	10	–	–	ns
Outputs					
CLA to AFLA, DFLA, DB0-DB7 output delay time	t_{OD}	20	–	100	ns
CLTW to TO output delay time	t_{OD}	–	–	60	ns

Values not yet available.



(1) CMOS: V_M = 50%.
TTL: V_M = 1,3 V.

Fig. 6 Waveforms showing the input set-up and hold times for LR, DFLA, DB0-DB7 to CLA; and clock-to-output propagation delays for CLA to AFLA, DFLA, DB0-DB7, and for CLTW to TO (DB0-DB7 input levels are TTL, all other levels are CMOS).

DEVELOPMENT DATA

PCM-AUDIO ANALOG/DIGITAL INTERFACE (ADI)

GENERAL DESCRIPTION

The SAA1133 forms part of the audio processing system for PCM-audio in 8 mm cassette video recorders. It provides digital compression and expansion, substitutes incorrect audio samples, and performs analog-to-digital and digital-to-analog conversion. Other ICs in the system are error-corrector-1 ECO-1 (SAA1131), error-corrector-2 ECO-2 (SAA1132), the ident-word interface IDI (SAA1136) and RAM storage.

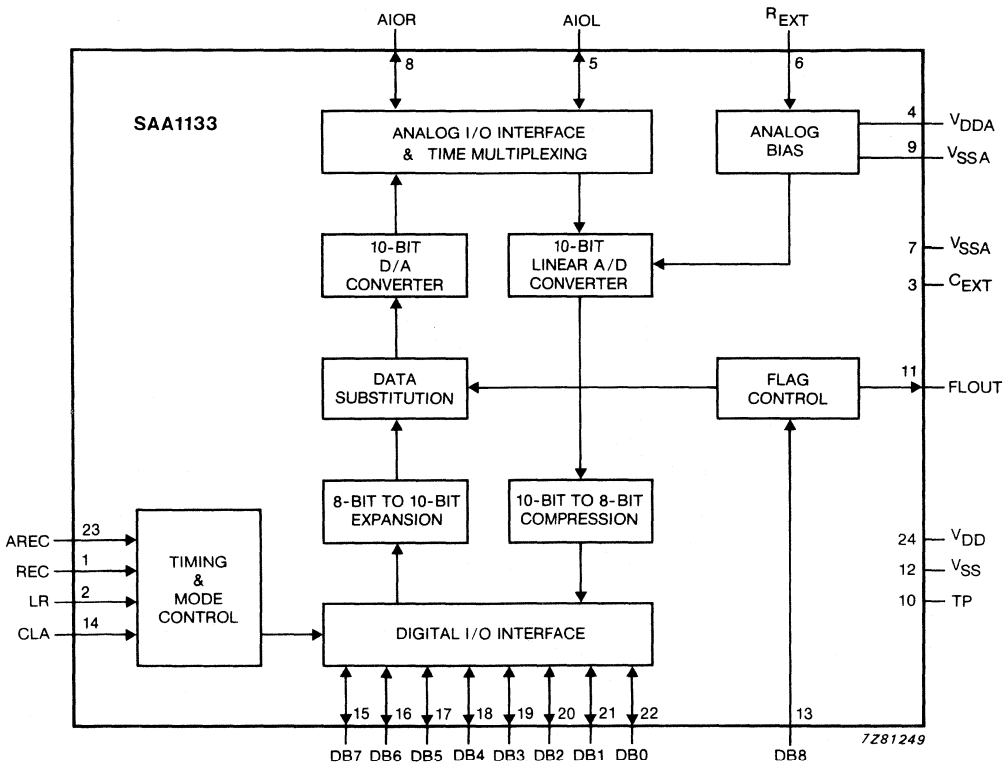


Fig. 1 Block diagram.

PACKAGE OUTLINE

SAA1133P: 24-lead DIL; plastic (SOT-101B).
SAA1133T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PINNING

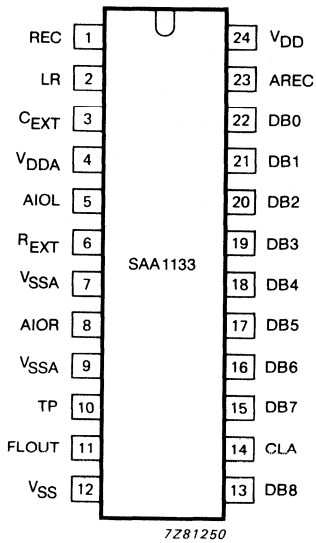


Fig. 2 Pinning diagram.

Power supplies

V_{DD} positive supply voltage (+ 5 V) for digital circuits
V_{DDA} positive supply voltage (+ 5 V) for analog circuits

For normal operation V_{DD} and V_{DDA} are connected to the same supply.

V_{SS} ground (0 V) for digital circuits
V_{SSA} ground (0 V) for analog circuits

For normal operation pins 3, 7, 9 and 12 should all be connected to the same ground plane (pins 3 and 7 have no internal connection but should be connected to the ground plane for screening purposes)

Inputs (CMOS)

CLA system clock, typ. 1,44 MHz (CCIR) or 1,45 MHz (NTSC) (92 x line frequency)

REC, AREC mode-select inputs;

AREC	REC	mode
0	0	playback (DAC-mode)
0	1	record (ADC-mode)
1	0	special after-record mode (DAC-mode)
1	1	not allowed

When the ADI is switched into playback mode, the first valid sample arrives at an analog output pin after two complete LR cycles (DB8 is HIGH). When the ADI is switched into record or after-record mode the first valid sample is available at DB0-DB7 after one complete LR cycle.

LR	system data bus control, typ. 31,25 kHz (CCIR) or 31,45 kHz (NTSC). LR HIGH time = LOW time = 23 CLA cycles
TP	test pin. Must be held LOW for normal operation
DB8	fault flag input from data bus

Input/outputs (TTL-input/3-state push-pull output)

DB0 (lsb) to DB7 (msb)	data but connections. I/O state is determined by REC and AREC. The processing delay between digital I/O and analog I/O is two LR cycles in playback mode and one LR cycle in record modes

Input/outputs (analog)

AIOL	analog I/O left channel
AIOR	analog I/O right channel
	I/O state is determined by REC and AREC. Both pins have d.c. bias levels of $0{,}6 \times V_{DD}$. Max. a.c. signal (peak-to-peak value) = 1,3 V
C_{EXT}	this pin is to be connected to ground via a 100 μF smoothing capacitor

Analog bias connection

R_{EXT}	this pin is to be connected to ground via a 27 kΩ 1% resistor

Output (CMOS push-pull)

FLOUT	fault flag output signal (playback mode) derived from the status of DB8. In record mode FLOUT = HIGH

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Data format

Digital audio samples are transferred to and from the ADI via the data bus in 8-bit, two's complement format (i.e. −128/+ 127). Analog-to-digital and digital-to-analog conversion is performed using 10-bit offset-binary converters. In the record mode data is compressed from 10 to 8 bits and in the playback mode it is expanded from 8 to 10 bits according to the conversion algorithm shown in Fig. 3.

Samples from the left (AIOL) and right (AIOR) audio channels are transferred in a time-multiplex sequence on the data bus. Left/right identification is given by the status of LR: when LR = HIGH, left samples are transferred.

Data bus timing (Figs 4 and 5)

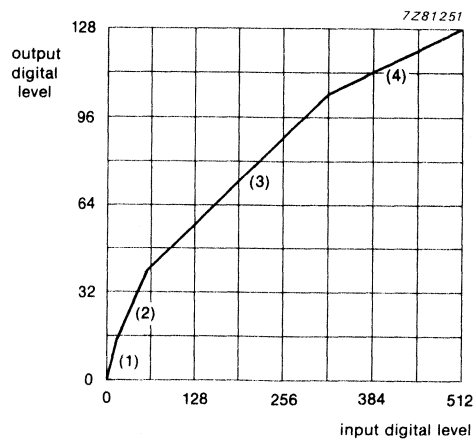
A transition of LR is used as reference for data bus timing. LR is defined with respect to the falling edge of clock CLA. The status of the data bus depends on the mode of operation selected by the system inputs REC and AREC. The modes are:

Playback mode	data is clocked into the ADI via DB7-DB0 on the *second* falling edge of CLA following a transition of LR
Record mode	data is available at DB7-DB0 during the CLA HIGH period that precedes the *second* falling edge of CLA following a transition of LR. For all other conditions DB7 to DB0 are in the high impedance OFF-state
After-record mode	data is available at DB7-DB0 during the CLA HIGH period that precedes the *fourth* falling edge of CLA following a transition of LR. For all other conditions DB7 to DB0 are in the high impedance OFF-state.

input range X = absolute value at input (9 bits)	conversion Y = absolute value at output (7 bits)
$16 \leqslant X < 64$	$Y = [X/2] + 8$
$64 \leqslant X < 320$	$Y = [X/4] + 24$
$320 \leqslant X < 511$	$Y = [X/8] + 64$

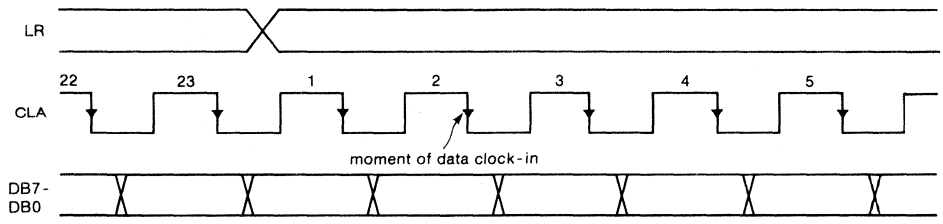
(a) conversion algorithm

slope (see Fig. 3b)	encoding law	input digital level	output digital level
(1)	10 bits to 10 bits	0 to 15	0 to 15
(2)	10 bits to 9 bits	16 to 63	16 to 39
(3)	10 bits to 8 bits	64 to 319	40 to 103
(4)	10 bits to 7 bits	320 to 511	104 to 127

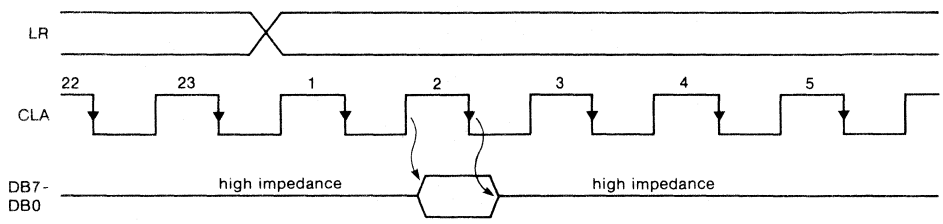


(b) conversion specification

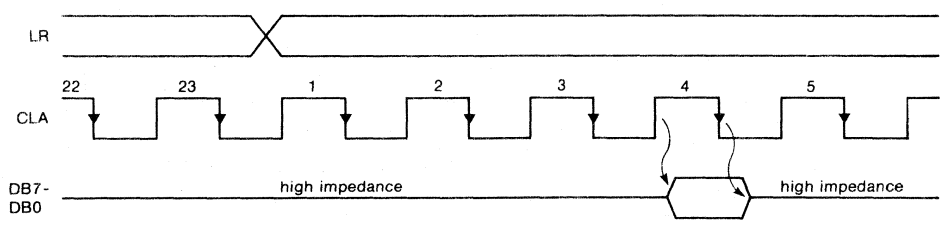
Fig. 3 8-bit non-linear PCM converter algorithm.



(a) playback mode: clocking-in of data



(b) recording mode: data output timing



(c) after-record mode: data output timing

Fig. 4 Data timing in playback, record and after-record modes.

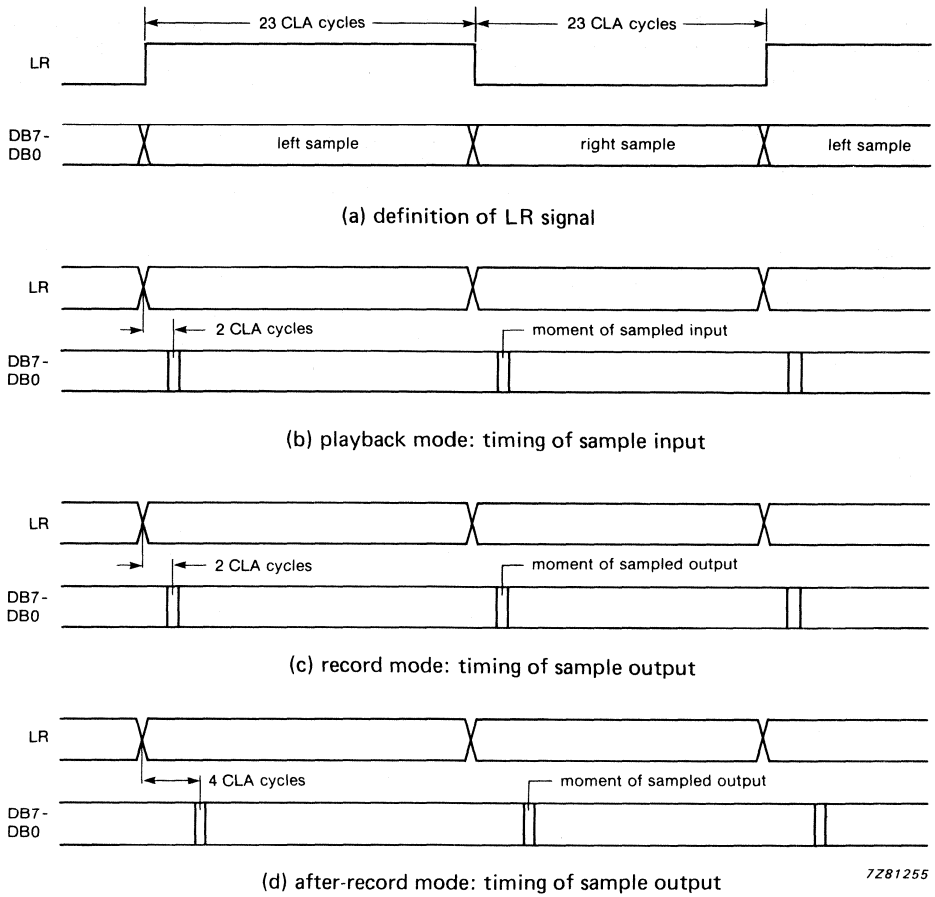


Fig. 5 Bus timing in playback, record and after-record modes.

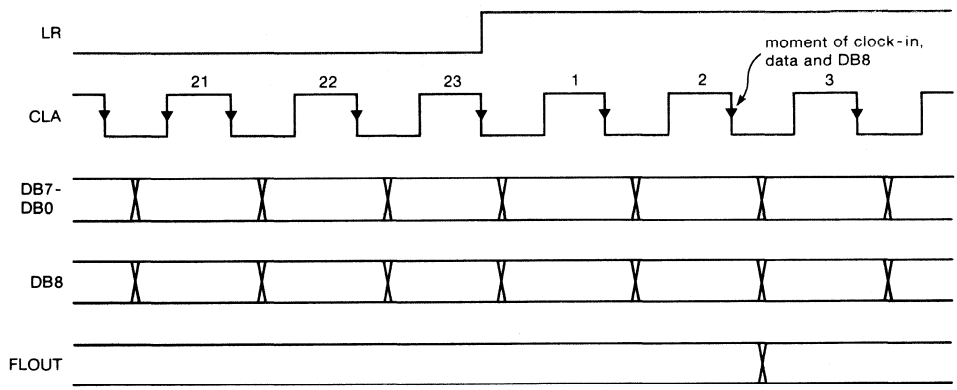
Data substitution (Fig. 6)

Data substitution occurs in the playback mode when an incorrect data sample is received. Indication of an incorrect sample is given by the fault flag DB8 which is clocked into the ADI with each data sample. The fault flag is available at the FLOUT output until the next DB8 bit is clocked-in 23 CLA cycles later.

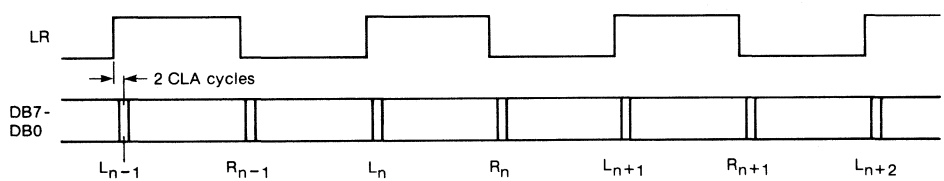
When an incorrect sample occurs between two correct samples, the substitution value is obtained by linear interpolation of the two correct sample values. Referring to Fig. 6b, assuming L_n to be the incorrect sample and L_{n-1}, $L_n + 1$ the correct samples, the substitution value for L_n is $(L_{n-1} + L_n + 1)/2$.

When a correct sample is followed by two incorrect samples, the first incorrect sample is substituted by the value of the preceding correct sample. Referring again to Fig. 6b, assuming L_{n-1} to be a correct sample and L_n, $L_n + 1$ the incorrect samples, L_n is substituted with the value of L_{n-1}.

After a sample has undergone data substitution it is then handled as a correct sample. The substitution process is performed with 10-bit expanded data.



(a) fault flag and data timing



(b) positioning of data samples

7Z81252

Fig. 6 Fault flag and data timing in playback mode.

Digital-to-analog conversion

Resolution	10 bits
Total accuracy	10 lsb
Differential linearity	1 lsb
Monotonicity	guaranteed over full range
Reference voltage	1,3 V

Analog-to-digital conversion

Conversion time	< 16 μs
Sample and hold settling time	< 4 μs

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	pin 24	$V_{DD} = V_{24\text{-}12}$	−0,5	+ 7	V
Supply current	pin 24	I_{DD}	–	50	mA
Supply voltage range	pin 4	$V_{DDA} = V_{24\text{-}12}$	−0,5	+ 7	V
Supply current	pin 4	I_{DDA}	–	50	mA
Supply current	pin 12	I_{SS}	–	70	mA
Supply current	pin 7	I_{SSA}	–	70	mA
Input voltage range		V_I	−0,5	V_{DD} + 0,5*	V
Input current		I_I	–	± 10	mA
Output current		I_O	–	± 10	mA
Total power dissipation		P_{tot}	–	200	mW
Storage temperature range		T_{stg}	−55	+ 150	°C

* V_{DD} + 0,5 V not to exceed 7,0 V.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

T_{amb} = −20 to + 70 °C; V_{DD} = 4,75 to 5,25 V; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 24	V_{DD}	4,75	5,0	5,25	V
Supply current	pin 24; $V_I = V_{DD}$ or V_{SS} for all inputs; I_O = 0 mA for all outputs					
quiescent current		I_{DD}	–	–	10	μA
active current		I_{DD}	–	–	700	μA
Supply current	pin 4	I_{DDA}	–	–	5	mA
Input leakage current	all inputs	I_I	–	–	10	μA
Input capacitance	all inputs	C_I	–	–	7	pF
Inputs LR, CLA REC, AREC						
Input voltage HIGH		V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0,3 x V_{DD}	V
Input DB8						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V
Input/outputs DB0 to DB7						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V
Output voltage HIGH	$-I_{OH}$ = 2,3 mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW	I_{OL} = 2,6 mA	V_{OL}	–	–	0,4	V
3-state OFF-state leakage current		I_{OZ}	–	–	10	μA
Input/outputs AIOR, AIOL						
Inputs (record mode)	R_I = 20 kΩ					
input voltage						
low		V_{IL}	2,24	2,36	2,48	V
intermediate		V_{II}	2,86	3,01	3,16	V
high		V_{IH}	3,48	3,66	3,84	V

D.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input/outputs 1 AIOR, AIOL (continued)						
Outputs (playback mode)	I_O = 0,3 mA					
output voltage						
low		V_{OL}	2,24	2,36	2,48	V
intermediate		V_{OI}	2,86	3,01	3,16	V
high		V_{OH}	3,48	3,66	3,84	V
Output load						
resistance		R_L	3,3	–	–	kΩ
inductance		L_L	–	–	10	μH
capacitance		C_L	–	–	10	μF
Output FLOUT						
Output voltage HIGH	$-I_{OH}$ = 2,3 mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW	I_{OL} = 2,6 mA	V_{OL}	–	–	0,4	V

A.C. CHARACTERISTICS

T_{amb} = −20 to + 70 °C; V_{DD} = 4,75 to 5,25 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Inputs					
System clock CLA frequency	f_{CLA}	–	–	2,1	MHz
LR and DB8 to CLA set-up times	t_{su}	20	–	–	ns
DB0-DB7 to CLA set-up time	t_{su}	20	–	–	ns
LR and DB8 to CLA hold times	t_h	10	–	–	ns
DB0-DB7 to CLA hold time	t_h	10	–	–	ns
Outputs					
CLA to FLOUT, DB0-DB7 output delay time C_L = 50 pF	t_{OD}	20	–	100	ns

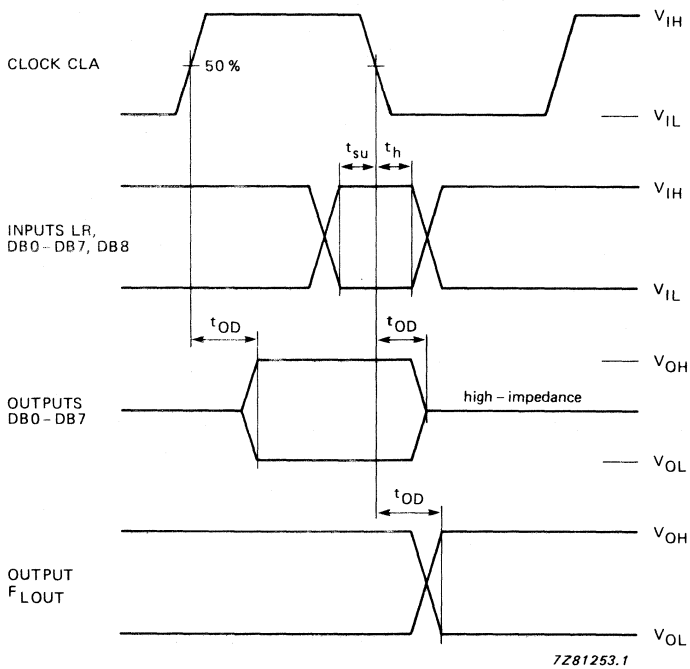


Fig. 7 Waveforms showing the input set-up and hold times of LR, DB0-DB7 and DB8 to CLA, and the clock-to-output delay time from CLA to DB0-DB7 and FLOUT (DB0-DB7 input levels are TTL, all other levels are CMOS).

DEVELOPMENT DATA

PCM-AUDIO IDENT-WORD INTERFACE (IDI)

GENERAL DESCRIPTION

The SAA1136 is an extension to the PCM-audio system for 8 mm cassette video recorders that allows the PCM bus to be accessed via the two-line bidirectional I²C bus. Other ICs in the system are error-corrector-1 ECO-1 (SAA1131), error-corrector-2 ECO-2 (SAA1132), analog/digital interface ADI (SAA1133) and RAM storage.

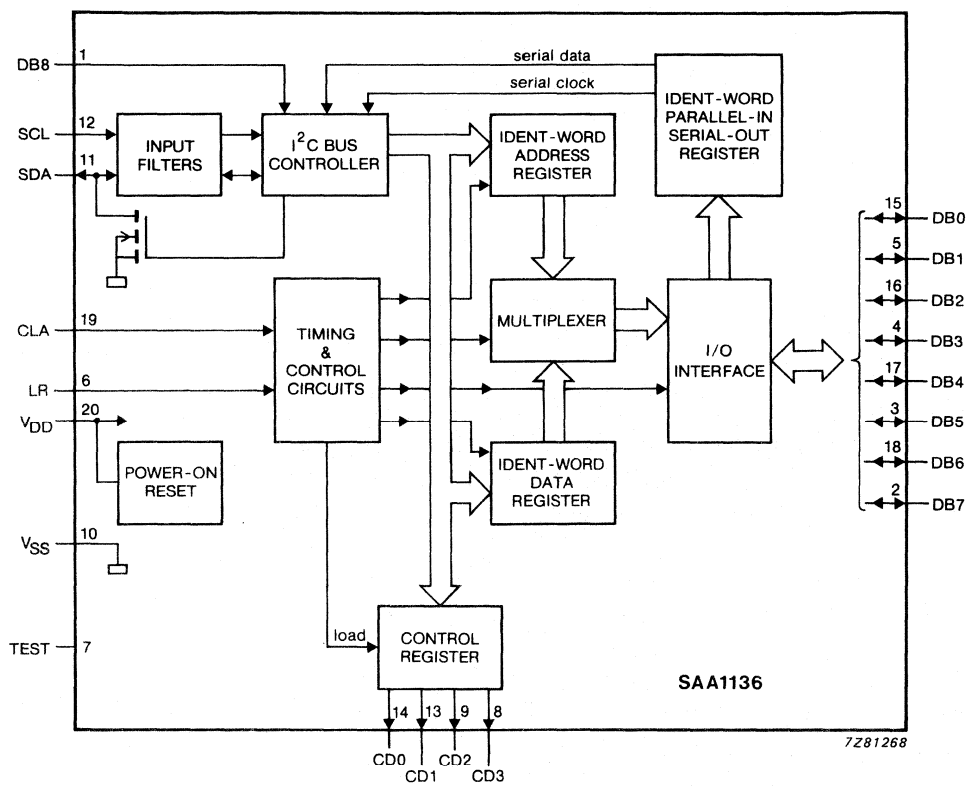


Fig. 1 Block diagram.

PACKAGE OUTLINES

SAA1136P: 20-lead DIL; plastic (SOT-146).
SAA1136T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PINNING

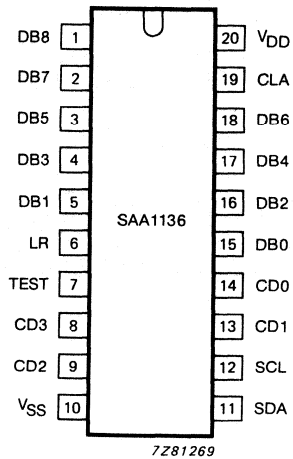


Fig. 2 Pinning diagram.

Power supplies

V_{DD}	positive supply voltage (+ 5 V)
V_{SS}	ground (0 V)

Inputs (TTL)

DB8	fault flag input from data bus
SCL	I^2C bus serial data clock

Inputs (CMOS)

LR	system data bus control, typ. 31,25 kHz (CCIR) or 31,45 kHz (NTSC)
TEST	test pin. Must be held LOW for normal operation
CLA	system clock, typ. 1437,5 kHz (CCIR) or 1449 kHz (NTSC) (92 x line frequency)

Input/outputs (TTL-input/3-state push-pull output)

DB0 (lsb) to DB7 (msb)	data bus connections. I/O state is determined by the process being performed

Input/output (TTL-input/open drain output)

SDA	I^2C bus data input/output

Outputs (CMOS push-pull)

CD0 to CD3	control outputs

FUNCTIONAL DESCRIPTION

The IDI is instructed via the I²C bus to perform one of three functions:

WRITE — Following a WRITE instruction, the address and data for an ident-word are received from the I²C bus. These are transcoded and transferred to the PCM bus during the 6th CLA clock following a transition of LR.

READ — Following a READ instruction, an ident-word address is received from the I²C bus. The ident-word corresponding to this address is read from the PCM bus on the 6th CLA clock following a transition of LR. The ident-word is then transcoded and transferred to the I²C bus.

CONTROL — Following a WRITE instruction and a specific (pointer) address from the I²C bus, the next I²C data controls the CD0-CD3 outputs.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

DEVELOPMENT DATA

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

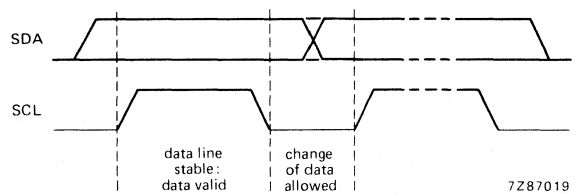


Fig. 3 Bit transfer.

CHARACTERISTICS OF THE I²C BUS (continued)

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

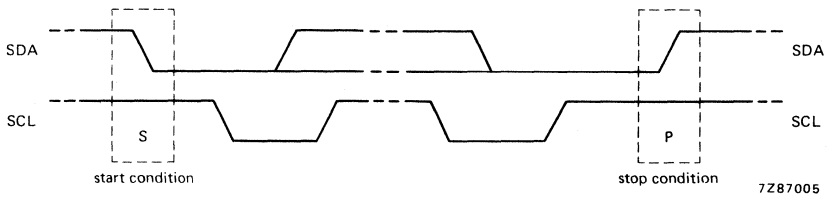


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

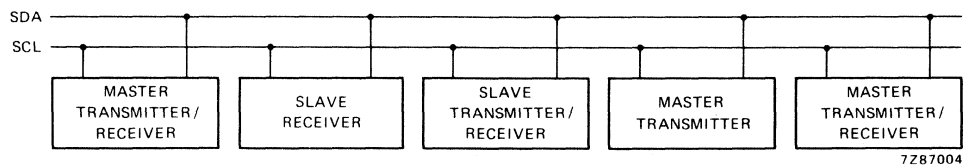


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

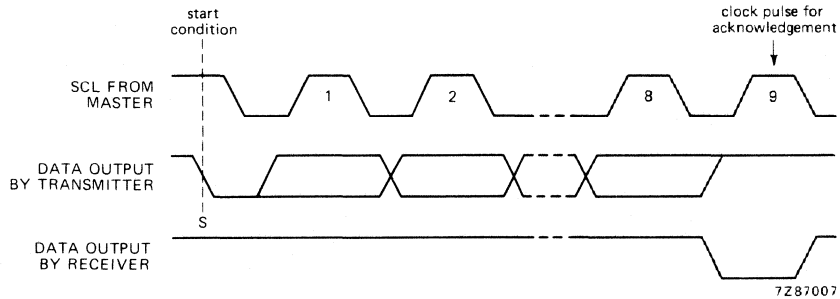


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The device operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

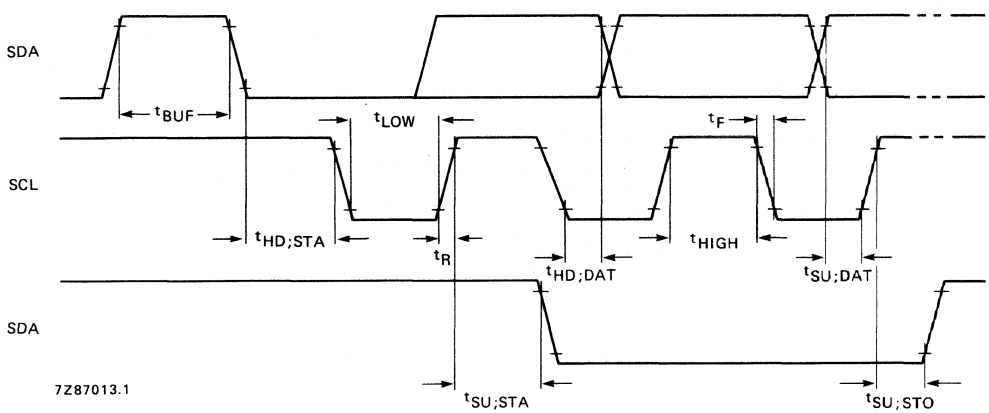


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period

Timing specifications (continued)

High-speed mode (continued)

$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

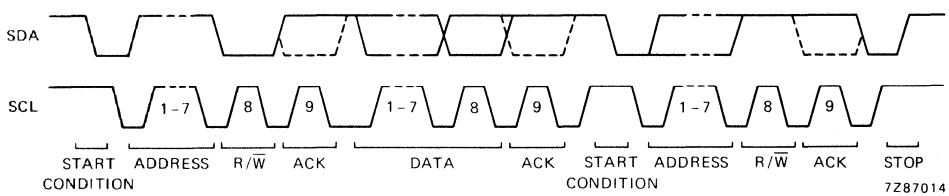


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

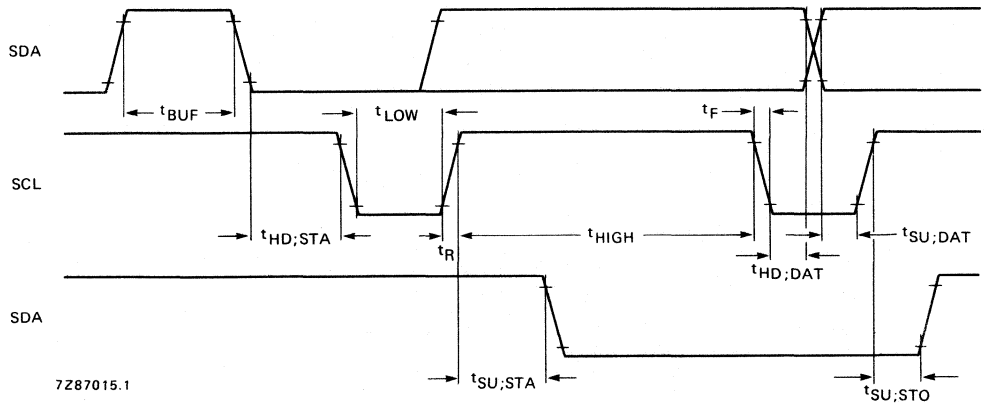


Fig. 9 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs *
$t_{HD;DAT}$	$t \geqslant$ 0 μs
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant$ 1 μs
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

* Only valid for repeated start code.

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

Timing specifications (continued)

Low-speed mode (continued)

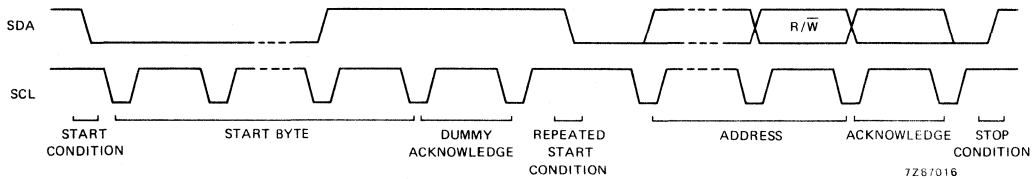
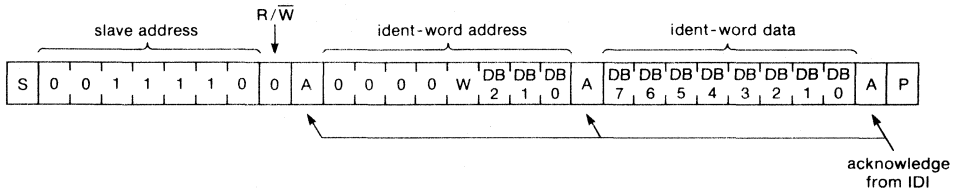


Fig. 10 Complete data transfer in the low-speed mode.

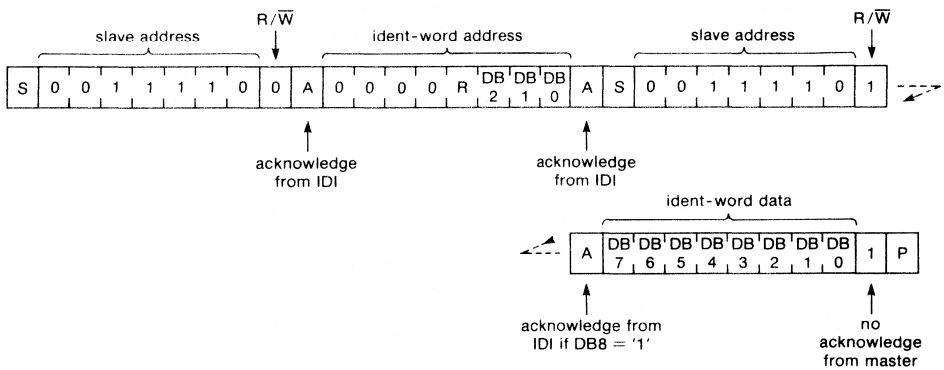
Where:	
Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

I²C bus protocol

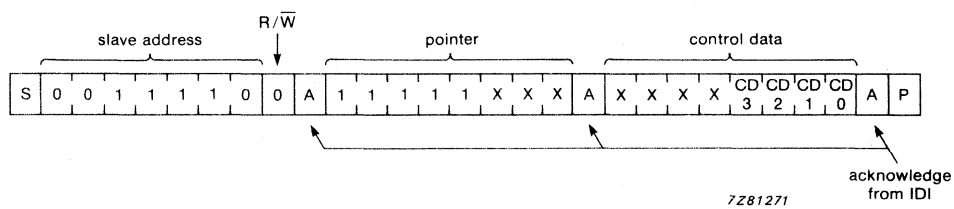
Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte after the start procedure. The IDI slave address is 0 0 1 1 1 1 0. The bus protocol for the WRITE, READ and CONTROL functions is shown in Fig. 11.



(a) WRITE



(b) READ



(c) CONTROL

Fig. 11 I^2C bus protocol.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	pin 20	$V_{DD} = V_{20-10}$	−0,5	7,0	V
Supply current	pin 20	I_{DD}	—	50	mA
Supply current	pin 10	I_{SS}	—	50	mA
Input voltage range		V_I	−0,5	V_{DD} + 0,5*	V
Input current		I_I	—	±10	mA
Output current		I_O	—	±10	mA
Total power dissipation		P_{tot}	—	200	mW
Storage temperature range		T_{stg}	−55	+150	°C

* V_{DD} + 0,5 V not to exceed 7,0 V.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

T_{amb} = −20 to +70 °C; V_{DD} = 4,75 to 5,25 V; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 20	V_{DD}	4,75	5,0	5,25	V
Supply current	pin 20; $V_I = V_{DD}$ or V_{SS} for all inputs; I_O = 0 mA for all outputs	I_{DD}	—	—	100	μA
Inputs LR, CLA						
Input voltage HIGH		V_{IH}	$0,7 \times V_{DD}$	—	—	V
Input voltage LOW		V_{IL}	—	—	$0,3 \times V_{DD}$	V
Input leakage current		I_I	—	—	1	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs DB8, SCL, TEST						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V
Input leakage current		I_I	–	–	1	μA
Input/outputs DB0 to DB7						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V
Output voltage HIGH	$-I_{OH}$ = 1,0 mA	V_{OH}	V_{DD}–0,4	–	–	V
Output voltage LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
3-state OFF-state leakage current		I_{OZ}	–	–	20	μA
Input/output SDL						
Input voltage HIGH		V_{IH}	2,0	–	–	V
Input voltage LOW		V_{IL}	–	–	0,8	V
Output voltage LOW	$+I_{OL}$ = 5 mA	V_{OL}	–	–	0,4	V
3-state OFF-state leakage current		I_{OZ}	–	–	20	μA

DEVELOPMENT DATA

A.C. CHARACTERISTICS

T_{amb} = −20 to +70 °C; V_{DD} = 4,75 to 5,25 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
INPUTS					
Serial data clock SCL frequency	f_{SCL}	–	–	100	kHz
System clock CLA frequency	f_{CLA}	–	–	2,1	MHz
LR to CLA set-up time	t_{su}	20	–	–	ns
DB0-DB7, DB8 to CLA set-up time	t_{su}	20	–	–	ns
LR to CLA hold time	t_h	10	–	–	ns
DB0-DB7, DB8 to CLA hold time	t_h	10	–	–	ns
OUTPUTS					
CLA to DB0-DB7 output delay time C_L = 50 pF	t_{OD}	20	–	100	ns

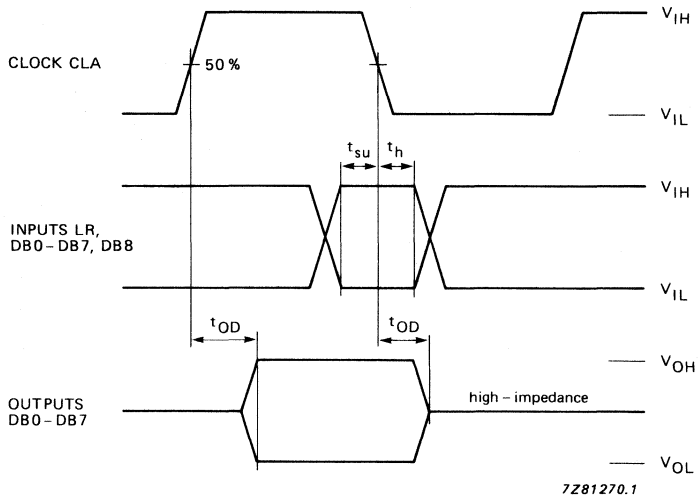


Fig. 12 Waveforms showing the input set-up and hold times of LR, DB0-DB7 and DB8 to CLA, and the clock-to-output delay time from CLA to DB0-DB7 (DB0-DB7 input levels are TTL, all other levels are CMOS).

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 85 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

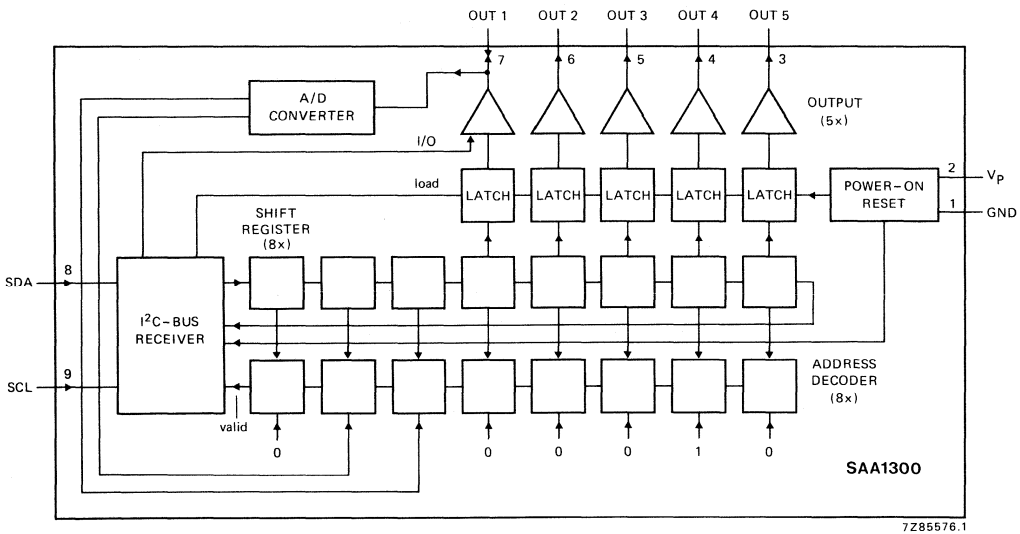


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

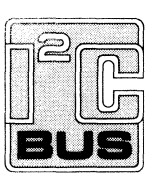
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max. 13,2	V
Input voltage range at SDA, SCL	V_I	−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I	−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O	−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max. 20	mA
Input current at OUT 1	I_I	max. 20	mA
Total power dissipation	P_{tot}	max. 825	mW
Storage temperature range	T_{stg}	−40 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	8	12	V
Supply current					
5 outputs LOW	I_{PL}	5	10	15	mA
5 outputs HIGH	I_{PH}	30	50	70	mA
Power-on reset level output stage in "OFF' condition	V_{PR}	–	3,5	3,8	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	3,0	–	5,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	$-I_{IH}$	–	–	10	μA
Input current LOW	I_{IH}	–	–	0,4	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source: "ON"	I_{Oso}	+ 85	–	+ 150	mA
Maximum output current; source: "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso} = 85 mA	V_{OH}	V_P–2	–	–	V
Output current; sink "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi} = –100 μA	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 10 mA	V_{OM}	V_P–0,5	–	–	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* Outputs must not be driven simultaneously at maximum source current.

REMOTE CONTROL TRANSMITTER

GENERAL DESCRIPTION

The SAA3004 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The SAA3004 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

The SAA3004 has the following features:

- Flashed or modulated transmission
- 7 sub-system addresses
- Up to 64 commands per sub-system address
- High-current remote output at V_{DD} = 6 V ($-I_{OH}$ = 40 mA)
- Low number of additional components
- Key release detection by toggle bits
- Very low stand-by current ($< 2\ \mu A$)
- Operational current < 2 mA at 6 V supply
- Wide supply voltage range (4 to 11 V)
- Ceramic resonator controlled frequency (typ. 450 kHz)
- Encapsulation: 20-lead plastic DIL or 20-lead plastic mini-pack (SO-20)

PACKAGE OUTLINES

SAA3004P: 20-lead DIL; plastic (SOT-146).
SAA3004T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

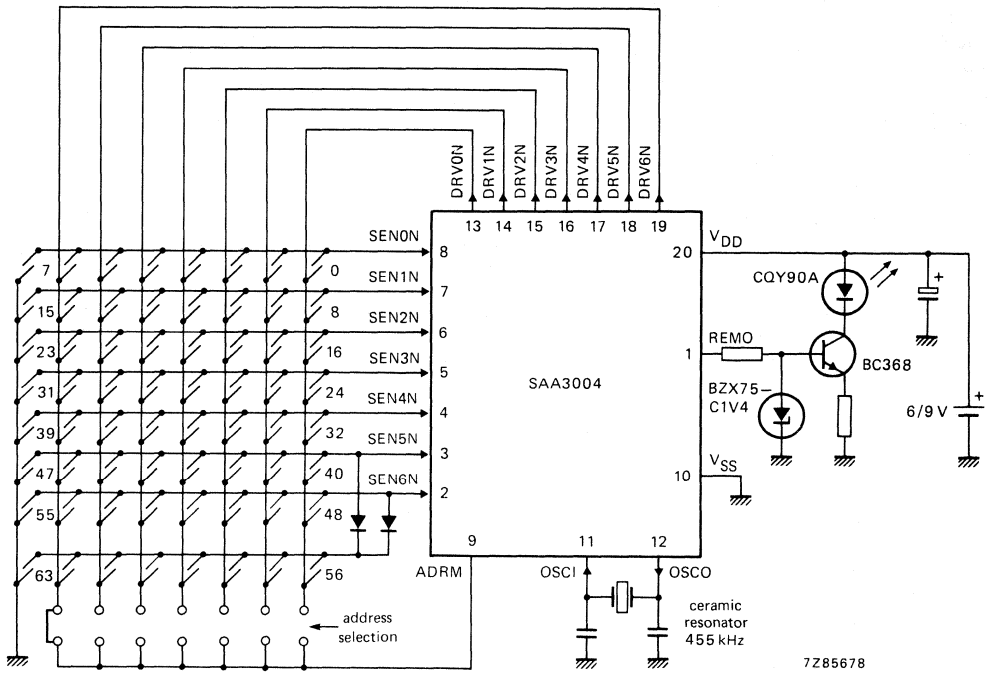


Fig. 1 Transmitter with SAA3004.

INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable.The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

Address mode input (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven sub-system addresses as shown in Table 3. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by presssing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if driver DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in transmitters for more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4.

A change of the sub-system address will not start a transmission.

Remote control signal output (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in Tables 1 and 2.

The information is defined by the distance t_D between the leading edges of the flashed pulses or the first edge of the modulated pulses (see Fig. 3).

The format of the output data is given in Figs 2 and 3. In the flashed transmission mode the data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A, which are defined by the selected key.

In the modulated transmission mode the first toggle bit T1 is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence.

The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command.

The codes for the sub-system address and the selected key are given in Tables 3 and 4.

Oscillator input/output (OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 400 kHz and 500 kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation

In the stand-by mode all drivers (DRV0N to DRV6N) are on. Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see Fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch. In contradiction to the command code the sub-system address is sensed only within the *first* scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key-stroke sequence (see Fig. 5) the command code is always altered in accordance with the sensed key.

Multiple key-stroke protection

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see Fig. 5). In case of a multiple key-stroke the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

FUNCTIONAL DESCRIPTION (continued)

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored.
- SEN5N and SEN6N are not protected against multiple key-stroke on the same driver line, because this condition has been used for the definition of additional codes (code numbers 56 to 63).

Output sequence (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in Figs 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see Fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

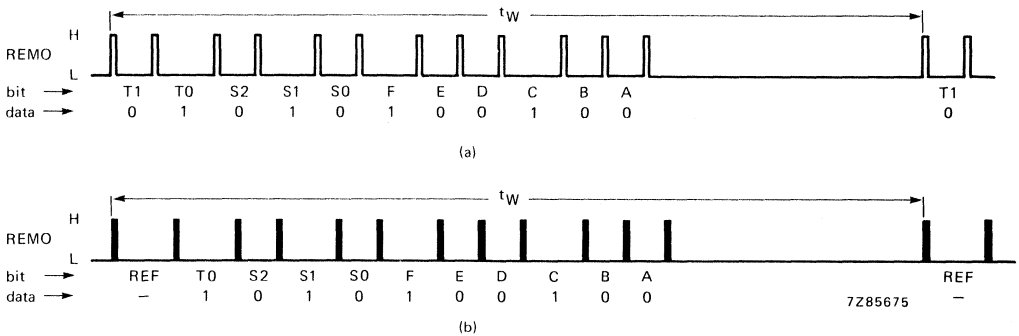
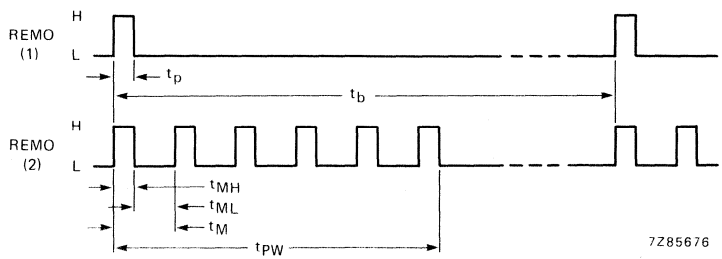


Fig. 2 Data format of REMO output; REF = reference time; T0 and T1 = toggle bits; S0, S1 and S2 = system address; A, B, C, D, E and F = command bits.
(a) flashed mode: transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).
(b) modulated mode: transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).



(1) Flashed pulse.
(2) Modulated pulse ($t_{PW} = (5 \times t_M) + t_{MH}$.

Fig. 3 REMO output waveform.

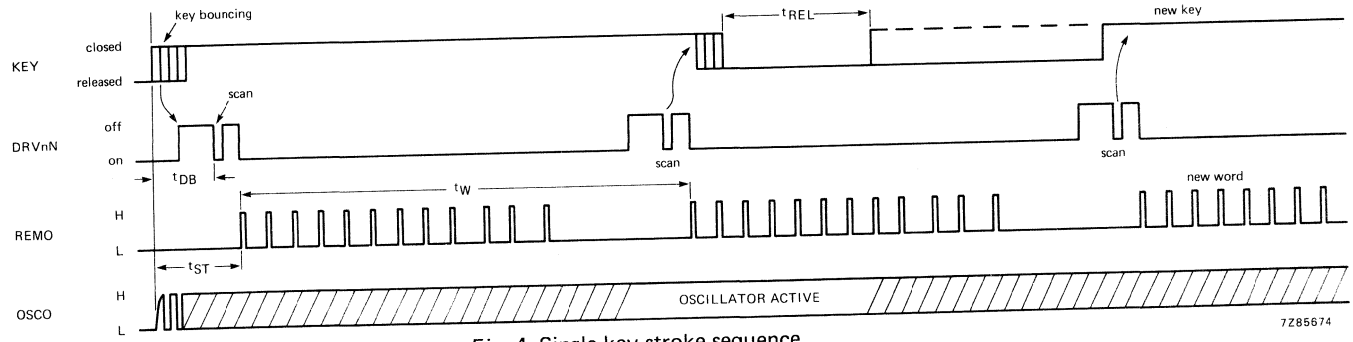


Fig. 4 Single key-stroke sequence.
Debounce time: $t_{DB} = 4$ to $9 \times T_o$.
Start time: $t_{ST} = 5$ to $10 \times T_o$.
Minimum release time: $t_{REL} = T_o$.
Word distance: t_W.

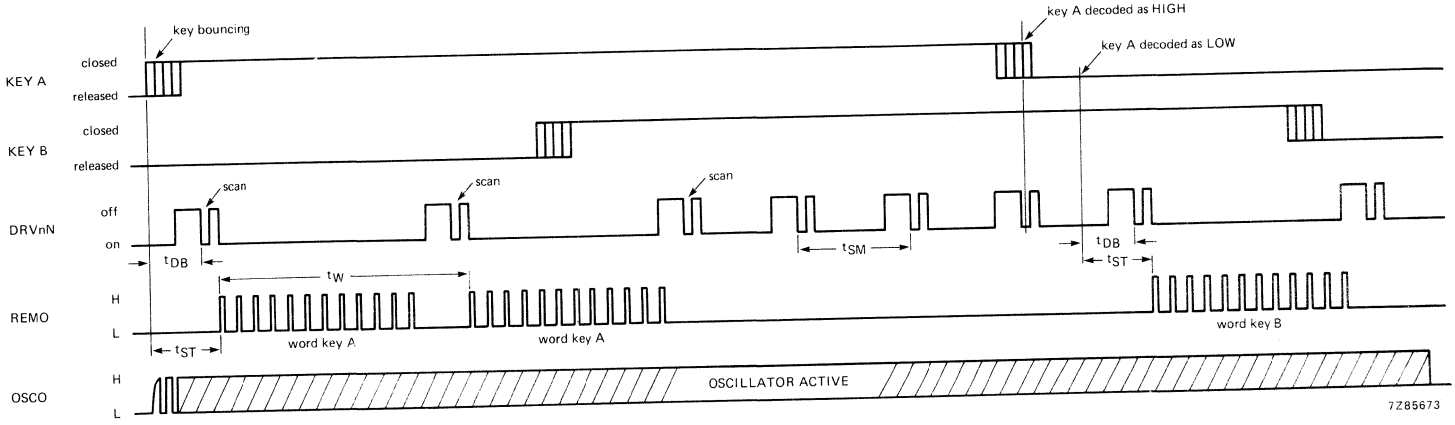


Fig. 5 Multiple key-stroke sequence.
Scan rate multiple key-stroke: $t_{SM} = 6$ to $10 \times T_o$.
For t_{DB}, t_{ST} and t_W see Fig. 4.

Table 1 Pulse train timing

mode	T_o ms	t_p μs	t_M μs	t_{ML} μs	t_{MH} μs	t_W ms
flashed	2,53	8,8	–	–	–	121
modulated	2,53	–	26,4	17,6	8,8	121

f_{osc}	455 kHz	$t_{osc} = 2{,}2\ \mu s$
t_p	$4 \times t_{osc}$	flashed pulse width
t_M	$12 \times t_{osc}$	modulation period
t_{ML}	$8 \times t_{osc}$	modulation period LOW
t_{MH}	$4 \times t_{osc}$	modulation period HIGH
T_o	$1152 \times t_{osc}$	basic unit of pulse distance
t_W	$55\ 296 \times t_{osc}$	word distance

Table 2 Pulse train separation (t_b)

code	t_b
logic "0"	$2 \times T_o$
logic "1"	$3 \times T_o$
reference time	$3 \times T_o$
toggle bit time	$2 \times T_o$ or $3 \times T_o$

Table 3 Transmission mode and sub-system address selection

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode.

mode	sub-system address				driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	o						
A	2	0	0	1	X	o					
S	3	0	1	0	X	X	o				
H	4	0	1	1	X	X	X	o			
E	5	1	0	0	X	X	X	X	o		
D	6	1	0	1	X	X	X	X	X	o	
M											
O	0	1	1	1							o
D	1	0	0	0	o						o
U	2	0	0	1	X	o					o
L	3	0	1	0	X	X	o				o
A	4	0	1	1	X	X	X	o			o
T	5	1	0	0	X	X	X	X	o		o
E	6	1	0	1	X	X	X	X	X	o	o
D											

o = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 Key codes

matrix drive	matrix sense	code F	E	D	C	B	A	matrix position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1	**			8 to 15
*	SEN2N	0	1	0	**			16 to 23
*	SEN3N	0	1	1	**			24 to 31
*	SEN4N	1	0	0	**			32 to 39
*	SEN5N	1	0	1	**			40 to 47
*	SEN6N	1	1	0	**			48 to 55
*	SEN5N and SEN6N	1	1	1	**			56 to 63

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5N/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

DEVELOPMENT DATA

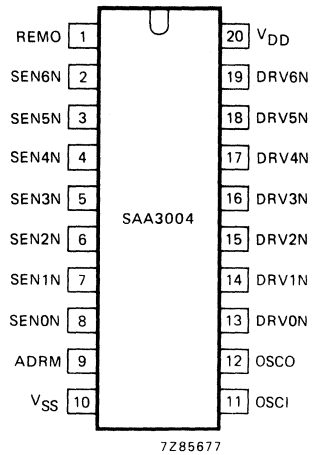


Fig. 6 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	key matrix sense inputs
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address mode control input
10	V_{SS}	ground
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	key matrix drive outputs
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to +15		V
Input voltage range	V_I	−0,5 to V_{DD} +0,5		V
Output voltage range	V_O	−0,5 to V_{DD} +0,5		V
D.C. current into any input or output	±I	max.	10	mA
Peak REMO output current during 10 μs; duty factor = 1%	$-I_{(REMO)M}$	max.	300	mA
Power dissipation per package for T_{amb} = −20 to +70 °C	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−55 to +150		°C
Operating ambient temperature range	T_{amb}	−20 to +70		°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage T_{amb} = 0 to +70 °C	–	V_{DD}	4	–	11	V
Supply current; active f_{osc} = 455 kHz; REMO output unloaded	6 9	I_{DD} I_{DD}	– –	1 3	– –	mA mA
Supply current; inactive (stand-by mode) T_{amb} = 25 °C	6 9	I_{DD} I_{DD}	– –	– –	2 2	μA μA
Oscillator frequency (ceramic resonator)	4 to 11	f_{osc}	400	–	500	kHz
Keyboard matrix						
Inputs SEN0N to SEN6N						
Input voltage LOW	4 to 11	V_{IL}	–	–	0,2 x V_{DD}	V
Input voltage HIGH	4 to 11	V_{IH}	0,8 x V_{DD}	–	–	V
Input current V_I = 0 V	4 11	$-I_I$ $-I_I$	10 30	– –	100 300	μA μA
Input leakage current V_I = V_{DD}	11	I_I	–	–	1	μA
Outputs DRV0N to DRV6N						
Output voltage "ON" I_O = 0,1 mA I_O = 1,0 mA	4 11	V_{OL} V_{OL}	– –	– –	0,3 0,5	V V
Output current "OFF" V_O = 11 V	11	I_O	–	–	10	μA
Control input ADRM						
Input voltage LOW	–	V_{IL}	–	–	0,8 x V_{DD}	V
Input voltage HIGH	–	V_{IH}	0,2 x V_{DD}	–	–	V
Input current (switched P- and N-channel pull-up/ pull-down)						
Pull-up active stand-by voltage: 0 V	4 11	I_{IL} I_{IL}	10 30	– –	100 300	μA μA
Pull-down active stand-by voltage: V_{DD}	4 11	I_{IH} I_{IH}	10 30	– –	100 300	μA μA

CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Data output REMO						
Output voltage HIGH	6	V_{OH}	3	–	–	V
$-I_{OH}$ = 40 mA	9	V_{OH}	6	–	–	V
Output voltage LOW	6	V_{OL}	–	–	0,2	V
I_{OL} = 0,3 mA	9	V_{OL}	–	–	0,1	V
Oscillator						
Input current OSCI at V_{DD}	6	I_I	0,8	–	2,7	μA
Output voltage HIGH $-I_{OL}$ = 0,1 mA	6	V_{OH}	–	–	V_{DD}–0,6	V
Output voltage LOW I_{OH} = 0,1 mA	6	V_{OL}	–	–	0,6	V

LOW VOLTAGE INFRARED REMOTE CONTROL TRANSMITTER (RC-5)

GENERAL DESCRIPTION

The SAA3006 is intended as a general purpose (RC-5) infrared remote control system for use where only low supply voltages are available. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

Features

- Low supply voltage requirements
- Very low current consumption
- For infrared transmission link
- Transmitter for 32 x 64 commands
- One transmitter controls 32 systems
- Transmission biphase technique
- Short transmission times; speed-up of system reaction time
- Single-pin oscillator input
- Input protection
- Test mode facility

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	2 to 7	V
Input voltage range	V_I	0,5 to (V_{DD} + 0,5)	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)	V*
Output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	−25 to +85	°C

* V_{DD} + 0,5 V not to exceed 9 V.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

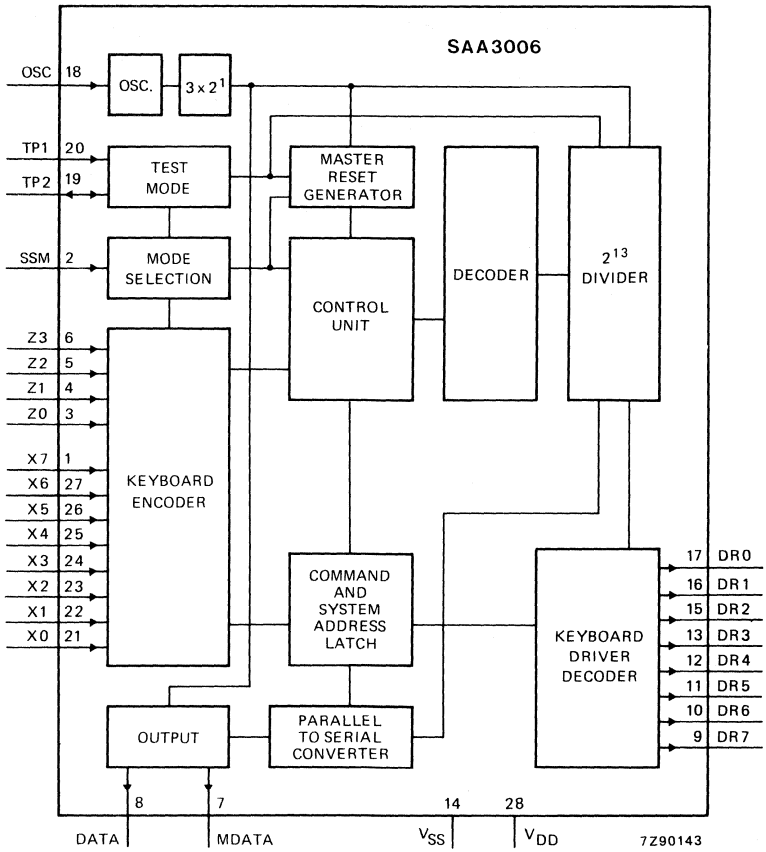


Fig. 1 Block diagram.

DEVELOPMENT DATA

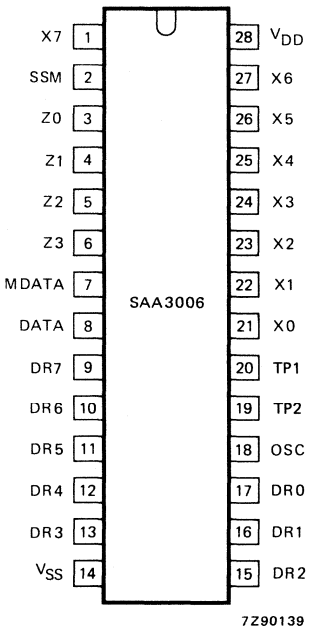
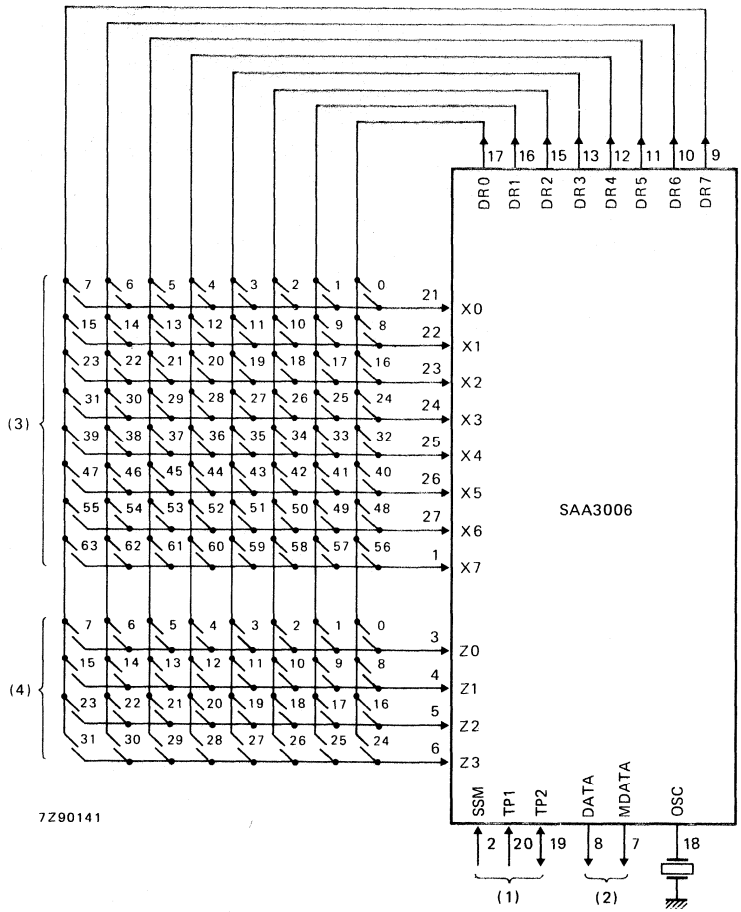


Fig. 2 Pinning diagram.

PINNING

14	V_{SS}	negative supply (ground)
28	V_{DD}	positive supply
21	X0	keyboard command inputs with P-channel pull-up transistors
22	X1	
23	X2	
24	X3	
25	X4	
26	X5	
27	X6	
1	X7	
3	Z0	keyboard system inputs with P-channel pull-up transistors
4	Z1	
5	Z2	
6	Z3	
2	SSM	system mode selection input
20	TP1	test input
19	TP2	test input/output
18	OSC	oscillator input
17	DR0	scan driver output with open drain N-channel transistors
16	DR1	
15	DR2	
13	DR3	
12	DR4	
11	DR5	
10	DR6	
9	DR7	
7	MDATA	remote signal outputs (3-state outputs)
8	DATA	



(1) Control inputs for operating modes, test modes and reset.
(2) Remote signal outputs.
(3) Keyboard command code matrix 8 x 8.
(4) Keyboard system code matrix 4 x 8.

Fig. 3 Keyboard interconnection.

FUNCTIONAL DESCRIPTION

Combined system mode (SSM = LOW)

The X and Z-lines are active HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z- or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches, depending on whether sensing was found in the Z- or X-input matrix. After latching a system address number, the device will generate the last command (i.e. all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single system mode (SSM = HIGH)

The X-lines are active HIGH in the quiescent state; the pull-up transistors of the Z-lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off, those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

DEVELOPMENT DATA

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

The oscillator is formed by a ceramic resonator (catalogue number 2422 540 98021 or equivalent) feeding the single-pin input OSC. Direct connection is made for supply voltages in the range 2 to 5,25 V but it is necessary to fit a 10 kΩ resistor in series with the resonator when using supply voltages in the range 2,6 to 7 V.

Key-release detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key operation during code transmission, the correct system and command numbers are generated.

FUNCTIONAL DESCRIPTION (continued)

Outputs

The output DATA carries the generated information according to the format given in Fig. 4 and Tables 2 and 3. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Fig. 5.

The code consists of four parts:

- Start part formed by 2 bits (two times a logical '1');
- Control part formed by 1 bit;
- System part formed by 5 bits;
- Command part formed by 6 bits.

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of 1/12 of the oscillator frequency, so that each bit is presented as a burst of 32 pulses. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation all the driver outputs go into the high ohmic state; a scanning procedure is then started so that the outputs are switched into the conducting state one after the other.

Reset action

The circuit will be reset immediately when a key release occurs during:

- debounce time;
- between two codes.

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:

- the key is released while one of the driver outputs is in the low-ohmic '0' state;
- the key is released before detection of that key;
- there is no wired connection in the Z-DR matrix while SSM is HIGH.

Test pin

The test pins TP1 and TP2 are used for testing in conjunction with inputs Z2 and Z3 as shown in Table 1.

Table 1 Test functions

TP1	TP2	Z2	Z3	function
LOW	LOW	matrix input	matrix input	normal
LOW	HIGH	matrix input	matrix input	scan + output frequency six times faster than normal
HIGH	output $f_{OSC}{}^{6}$	LOW	LOW	reset
HIGH	output $f_{OSC}{}^{6}$	HIGH	HIGH	output frequency 3×2^{7} faster than normal

KEY ACTIVITIES

Every connection of one X-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X-input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z-inputs, or Z-inputs and X-inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is made, the code is not generated.

When one X or Z-input is connected to more than one DR-output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 7 kΩ.

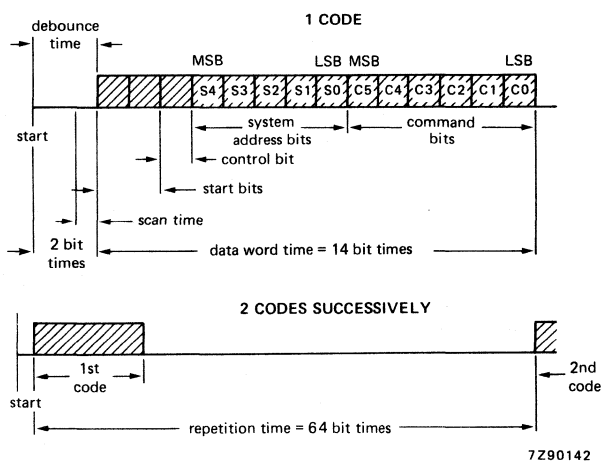


Fig. 4 DATA output format (RC-5).

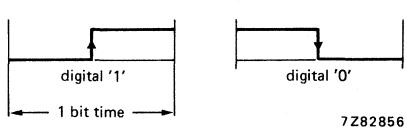


Fig. 5 Biphase transmission code; 1 bit time = $3 \times 2^8 \times T_{OSC}$ (typically 1,778 ms) where T_{OSC} is the oscillator period time.

Table 2 Command matrix X-DR

code no.	X-lines X..								DR-lines DR..								command bits C..					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
0	●								●								0	0	0	0	0	0
1	●									●							0	0	0	0	0	1
2	●										●						0	0	0	0	1	0
3	●											●					0	0	0	0	1	1
4	●												●				0	0	0	1	0	0
5	●													●			0	0	0	1	0	1
6	●														●		0	0	0	1	1	0
7	●															●	0	0	0	1	1	1
8		●							●								0	0	1	0	0	0
9		●								●							0	0	1	0	0	1
10		●									●						0	0	1	0	1	0
11		●										●					0	0	1	0	1	1
12		●											●				0	0	1	1	0	0
13		●												●			0	0	1	1	0	1
14		●													●		0	0	1	1	1	0
15		●														●	0	0	1	1	1	1
16			●						●								0	1	0	0	0	0
17			●							●							0	1	0	0	0	1
18			●								●						0	1	0	0	1	0
19			●									●					0	1	0	0	1	1
20			●										●				0	1	0	1	0	0
21			●											●			0	1	0	1	0	1
22			●												●		0	1	0	1	1	0
23			●													●	0	1	0	1	1	1
24				●					●								0	1	1	0	0	0
25				●						●							0	1	1	0	0	1
26				●							●						0	1	1	0	1	0
27				●								●					0	1	1	0	1	1
28				●									●				0	1	1	1	0	0
29				●										●			0	1	1	1	0	1
30				●											●		0	1	1	1	1	0
31				●												●	0	1	1	1	1	1

DEVELOPMENT DATA

code no.	X-lines X.. 0	1	2	3	4	5	6	7	DR-lines DR.. 0	1	2	3	4	5	6	7	command bits C.. 5	4	3	2	1	0
32					●				●								1	0	0	0	0	0
33					●					●							1	0	0	0	0	1
34					●						●						1	0	0	0	1	0
35					●							●					1	0	0	0	1	1
36					●								●				1	0	0	1	0	0
37					●									●			1	0	0	1	0	1
38					●										●		1	0	0	1	1	0
39					●											●	1	0	0	1	1	1
40						●			●								1	0	1	0	0	0
41						●				●							1	0	1	0	0	1
42						●					●						1	0	1	0	1	0
43						●						●					1	0	1	0	1	1
44						●							●				1	0	1	1	0	0
45						●								●			1	0	1	1	0	1
46						●									●		1	0	1	1	1	0
47						●										●	1	0	1	1	1	1
48							●		●								1	1	0	0	0	0
49							●			●							1	1	0	0	0	1
50							●				●						1	1	0	0	1	0
51							●					●					1	1	0	0	1	1
52							●						●				1	1	0	1	0	0
53							●							●			1	1	0	1	0	1
54							●								●		1	1	0	1	1	0
55							●									●	1	1	0	1	1	1
56								●	●								1	1	1	0	0	0
57								●		●							1	1	1	0	0	1
58								●			●						1	1	1	0	1	0
59								●				●					1	1	1	0	1	1
60								●					●				1	1	1	1	0	0
61								●						●			1	1	1	1	0	1
62								●							●		1	1	1	1	1	0
63								●								●	1	1	1	1	1	1

Table 3 System matrix Z-DR

system no.	Z-lines Z..				DR-lines DR..								system bits S..				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	●				●								0	0	0	0	0
1	●					●							0	0	0	0	1
2	●						●						0	0	0	1	0
3	●							●					0	0	0	1	1
4	●								●				0	0	1	0	0
5	●									●			0	0	1	0	1
6	●										●		0	0	1	1	0
7	●											●	0	0	1	1	1
8		●			●								0	1	0	0	0
9		●				●							0	1	0	0	1
10		●					●						0	1	0	1	0
11		●						●					0	1	0	1	1
12		●							●				0	1	1	0	0
13		●								●			0	1	1	0	1
14		●									●		0	1	1	1	0
15		●										●	0	1	1	1	1
16			●		●								1	0	0	0	0
17			●			●							1	0	0	0	1
18			●				●						1	0	0	1	0
19			●					●					1	0	0	1	1
20			●						●				1	0	1	0	0
21			●							●			1	0	1	0	1
22			●								●		1	0	1	1	0
23			●									●	1	0	1	1	1
24				●	●								1	1	0	0	0
25				●		●							1	1	0	0	1
26				●			●						1	1	0	1	0
27				●				●					1	1	0	1	1
28				●					●				1	1	1	0	0
29				●						●			1	1	1	0	1
30				●							●		1	1	1	1	0
31				●								●	1	1	1	1	1

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5	to	8,5	V
Input voltage range	V_I	−0,5	to	$(V_{DD}+0,5)$	V*
Input current	$+I_I$	max.		10	mA
Output voltage range	V_O	−0,5	to	$(V_{DD}+0,5)$	V*
Output current	$+I_O$	max.		10	mA
Power dissipation output OSC	P_O	max.		50	mW
Power dissipation per output (all other outputs)	P_O	max.		100	mW
Total power dissipation per package	P_{tot}	max.		200	mW
Operating ambient temperature range	T_{amb}	−25	to	+85	°C
Storage temperature range	T_{stg}	−55	to	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

* V_{DD} + 0,5 V not to exceed 9 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	—	V_{DD}	2	—	7	V
Supply current at I_O = 0 mA for all outputs; X0 to X7 and Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; excluding leakage current from open drain N-channel outputs; T_{amb} = 25 °C	7	I_{DD}	—	—	10	μA
Inputs						
Keyboard inputs X and Z with P-channel pull-up transistors						
Input current (each input) at V_I = 0 V; TP = SSM = LOW	2 to 7	$-I_I$	10	—	600	μA
Input voltage HIGH	2 to 7	V_{IH}	0,7 x V_{DD}	—	V_{DD}	V
Input voltage LOW	2 to 7	V_{IL}	0	—	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C; TP = HIGH; V_I = 7 V		I_{IR}	—	—	1	μA
V_I = 0 V		$-I_{IR}$	—	—	1	μA
SSM, TP1 and TP2						
Input voltage HIGH	2 to 7	V_{IH}	0,7 x V_{DD}	—	V_{DD}	V
Input voltage LOW	2 to 7	V_{IL}	0	—	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C; V_I = 7 V		I_{IR}	—	—	1	μA
V_I = 0 V		$-I_{IR}$	—	—	1	μA
OSC						
Input leakage current at T_{amb} = 25 °C; V_I = 0 V; TP1 = HIGH; Z2 = Z3 = LOW	2 to 7	$-I_I$	—	—	2	μA

DEVELOPMENT DATA

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Outputs						
DATA and MDATA						
Output voltage HIGH at $-I_{OH}$ = 0,4 mA	2 to 7	V_{OH}	V_{DD} −0,3	–	–	V
Output voltage LOW at I_{OL} = 0,6 mA	2 to 7	V_{OL}	–	–	0,3	V
Output leakage current at:						
V_O = 7 V		I_{OR}	–	–	10	μA
V_O = 0 V		$-I_{OR}$	–	–	20	μA
T_{amb} = 25 °C;						
V_O = 7 V		I_{OR}	–	–	1	μA
V_O = 0 V		$-I_{OR}$	–	–	2	μA
DR0 to DR7, TP2						
Output voltage LOW at I_{OL} = 0,3 mA	2 to 7	V_{OL}	–	–	0,3	V
Output leakage current at V_O = 7 V	7	I_{OR}	–	–	10	μA
at V_O = 7 V						
T_{amb} = 25 °C		I_{OR}	–	–	1	μA
OSC						
Oscillator current at OSC = V_{DD}	7	I_{OSC}	4,5	–	30	μA
Oscillator						
Maximum oscillator frequency at C_L = 40 pF (Figs 6 and 7)	2	f_{OSC}	–	–	450	kHz
Free-running oscillator frequency at T_{amb} = 25 °C	2	f_{OSC}	10	–	120	kHz

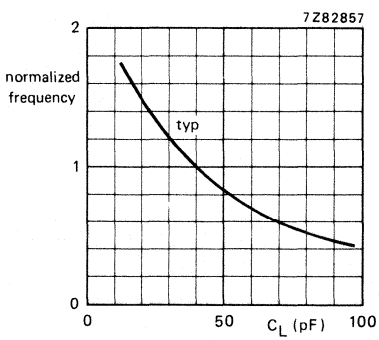


Fig. 6 Typical normalized input frequency as a function of the load (keyboard) capacitance.

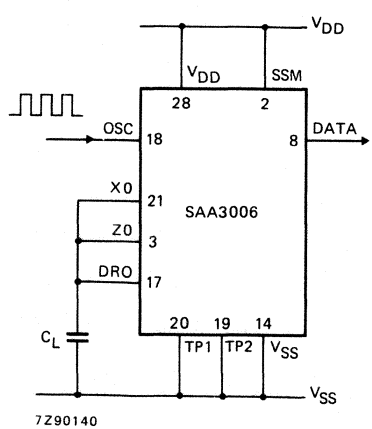


Fig. 7 Test circuit for measurement of maximum oscillator frequency.

INFRARED REMOTE CONTROL TRANSCODER (RC-5)

GENERAL DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available: one for RC-5 coded signals only; the other is selectable to accept (1) RC-5 coded signals only, or (2) RC-5 (extended) coded signals only. The input used is that at which an active code is first detected. Coded signals not in RC-5/RC-5(ext) format are rejected. Data input and output is by serial transfer, the output interface being compatible for I^2C bus operation.

Features

- Converts RC-5 or RC-5(ext) biphase coded signals into binary equivalents
- Two data inputs, one fixed (RC-5), one selectable (RC-5/RC-5(ext))
- Rejects all codes not in RC-5/RC-5(ext) format
- I^2C output interface capability
- Power-off facility
- Master/slave addressable for multi-transmitter/receiver applications in RC-5(ext) mode
- Power-on-reset for defined start-up

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,5 to	5,5 V
Supply current (quiescent) at V_{DD} = 5,5 V; T_{amb} = 25 °C	I_{DD}	max.	200 μA
Operating ambient temperature range	T_{amb}	−25 to	+85 °C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

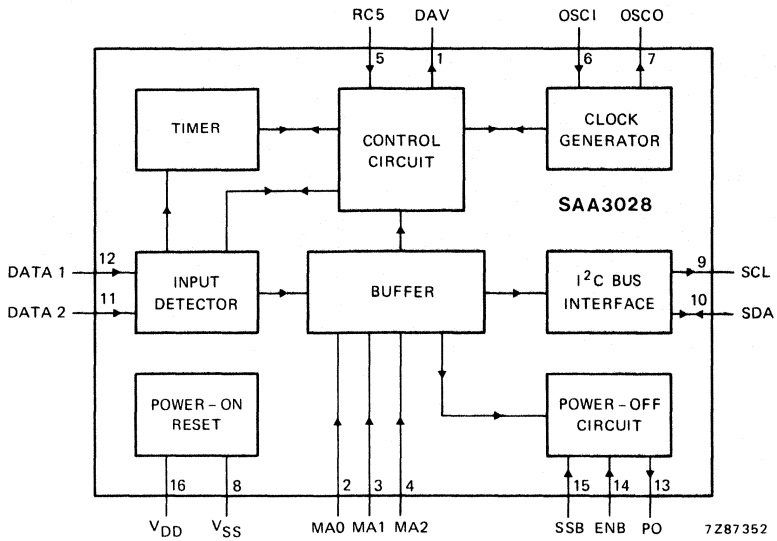


Fig. 1 Block diagram.

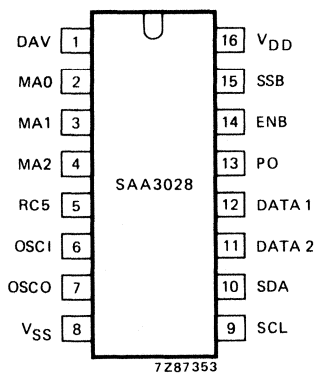


Fig. 2 Pinning diagram.

PINNING

1	DAV	data valid output with open drain N-channel transistor
2	MA0	master address inputs
3	MA1	master address inputs
4	MA2	master address inputs
5	RC5	data 2 input select
6	OSCI	oscillator input
7	OSCO	oscillator output
8	V_{SS}	negative supply (ground)
9	SCL	serial clock line (I^2C bus)
10	SDA	serial data line (I^2C bus)
11	DATA 2	data 2 input
12	DATA 1	data 1 input
13	PO	power-off signal output with open drain N-channel transistor
14	ENB	enable input
15	SSB	set standby input
16	V_{DD}	positive supply (+5 V)

FUNCTIONAL DESCRIPTION

Input function

The two data inputs are accepted into the buffer as follows:

- DATA 1. Only biphase coded signals which conform to the RC-5 format are accepted at this input.
- DATA 2. This input performs according to the logic state of the select input RC5. When RC5 = HIGH, DATA 2 input will accept only RC-5 coded signals. When RC5 = LOW, DATA 2 input will accept only RC-5(ext) coded signals.

The input detector selects the input, DATA 1 or DATA 2, in which a HIGH to LOW transition is first detected. The selected input is then accepted by the buffer for code conversion. All signals received that are not in the RC-5 or RC-5(ext) format are rejected.

Formats of RC-5 and RC-5(ext) biphase coded signals are shown in Figs 3 and 4 respectively; the codes commence from the left of the formats shown. The bit-times of the biphase codes are defined in Fig. 5.

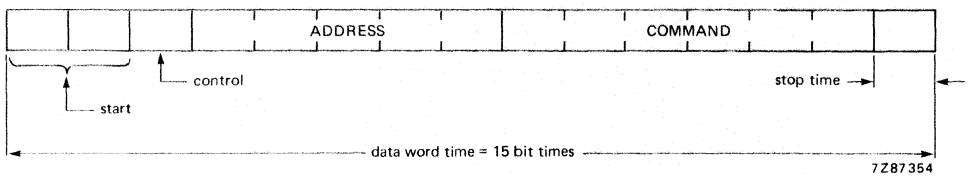


Fig. 3 RC-5 code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

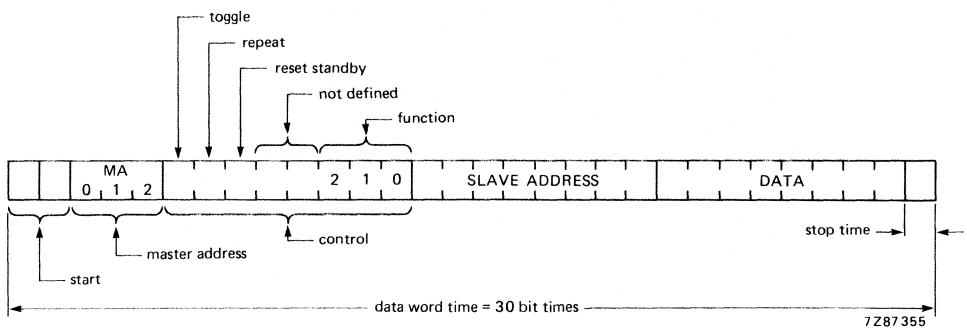


Fig. 4 RC-5(extended) code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

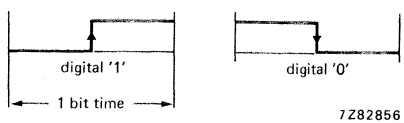


Fig. 5 Biphase code definition: RC-5 bit-time = $2^7 \times T_{OSC}$ = 1,778 ms (typical); RC-5(ext) bit-time = $2^6 \times T_{OSC}$ = 0,89 ms (typical), where T_{OSC} = the oscillator period time.

FUNCTIONAL DESCRIPTION (continued)

More information is added to the input data held in the buffer in order to make it suitable for transmission via the I^2C interface. The information now held in the buffer is as follows:

RC-5 buffer contents		RC-5(ext) buffer contents	
• data valid indicator	1 bit	• data valid indicator	1 bit
• format indicator	1 bit	• format indicator	1 bit
• input indicator	1 bit	• input indicator	1 bit
• control	1 bit	• master address	3 bits
• address data	5 bits	• control	8 bits
• command data	6 bits	• slave address	8 bits
		• data	8 bits

The information assembled in the buffer is subjected to the following controls before being made available at the I^2C interface:

ENB = HIGH — Enables the set standby input SSB.

SSB = LOW — Causes power-off output PO to go HIGH.

PO = HIGH — This occurs when the set standby input SSB = LOW and allows the existing values in the buffer to be overwritten by the new binary equivalent values. After ENB = LOW, SSB is don't care.

PO = LOW — This occurs according to the type of code being processed, as follows:

RC-5. When the binary equivalent value is transferred to the buffer.

RC-5(ext). When the reset standby bit is active and the master address bits are equal in value to the MA0, MA1, MA2 inputs.

At power-on, PO is reset to LOW.

DAV = HIGH — This occurs when the buffer contents are valid. If the buffer is not empty, or an output transfer is taking place, then the new binary values are discarded.

Output function

The data is assembled in the buffer in the format shown in Fig. 6 for RC-5 binary equivalent values, or in the format shown in Fig. 7 for RC-5(ext) binary equivalent values. The data is output serially, starting from the left of the formats shown in Figs 6 and 7.

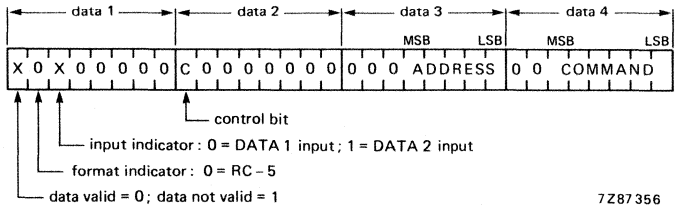


Fig. 6 RC-5 binary equivalent value format.

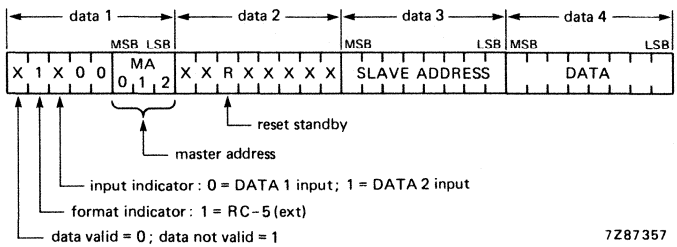


Fig. 7 RC-5(ext) binary equivalent value format.

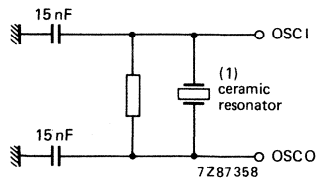
DEVELOPMENT DATA

The output signal DAV, derived in the buffer from the data valid bit, is provided to facilitate use of the transcoder on an interrupt basis. This output is reset to LOW during power-on.

The I^2C interface allows transmission on a bidirectional, two-wire I^2C bus. The interface is a slave transmitter with a built-in slave address, having a fixed 7-bit binary value of 0100110. Serial output of the slave address onto the I^2C bus starts from the left-hand bit.

Oscillator

The oscillator can comprise a ceramic resonator circuit as shown in Fig. 8. The typical frequency of oscillation is 455 kHz.



(1) Catalogue number of ceramic resonator: 2422 540 98008.

Fig. 8 Oscillator circuit.

FUNCTIONAL DESCRIPTION (continued)

I²C bus transmission

Formats for I²C transmission in low and high speed modes are shown respectively in Figs 9 and 10.

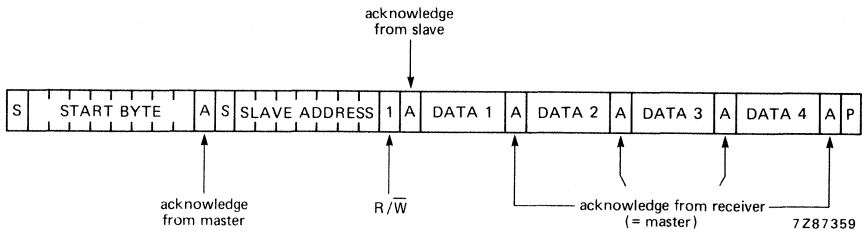


Fig. 9 Format for transmission in I²C low speed mode.

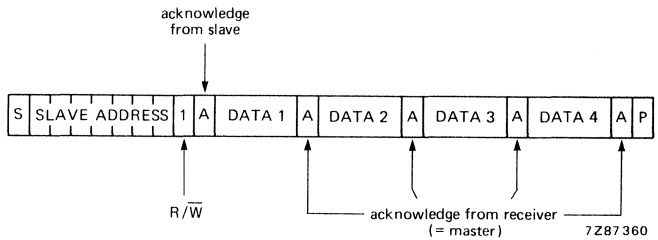


Fig. 10 Format for transmission in I²C high speed mode.

Note to Figures 9 and 10

When R/$\overline{W}$ bit = 0; the slave generates a NACK (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.

When the receiver generates a NACK; the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).

When all data has been transmitted, the data line remains HIGH and the slave waits for P.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to	+15 V
Input voltage range	V_I	−0,5 to	$(V_{DD}+0,5)$ V*
Input current	$\pm I_I$	max.	10 mA
Output voltage range	V_O	−0,5 to	$(V_{DD}+0,5)$ V*
Output current	$\pm I_O$	max.	10 mA
Power dissipation output OSCO	P_O	max.	50 mW
Power dissipation per output (all other outputs)	P_O	max.	100 mW
Total power dissipation per package	P_{tot}	max.	200 mW
Operating ambient temperature range	T_{amb}	−25 to	+85 °C
Storage temperature range	T_{stg}	−55 to	+150 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

Purchase of Philips I²C components conveys a licence under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	4,5	–	5,5	V
Supply current; quiescent at T_{amb} = 25 °C	5,5	I_{DD}	–	–	200	μA
Inputs						
MA0, MA1, MA2, DATA 1, DATA 2, RC5, SCL, ENB, SSB, OSCI						
Input voltage HIGH	4,5 to 5,5	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,5 to 5,5	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 5,5 V; T_{amb} = 25 °C	5,5	I_I	–	–	1	μA
Input leakage current at V_I = 0 V; T_{amb} = 25 °C;	5,5	$-I_I$	–	–	1	μA
Outputs						
DAV, PO						
Output voltage LOW at I_{OL} = 1,6 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
OSCO						
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	4,5 to 5,5	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 0,3 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at T_{amb} = 25 °C; V_O = 5,5 V	5,5	I_{OR}	–	–	1	μA
V_O = 0 V	5,5	I_{OR}	–	–	1	μA
SDO						
Output voltage LOW at I_{OL} = 2 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
Oscillator						
Max. oscillator frequency (Fig. 8)	4,75	f_{OSCI}	500	–	–	kHz

TELETEXT VIDEO PROCESSOR

GENERAL DESCRIPTION

The SAA5231 is a bipolar integrated circuit intended as a successor to the SAA5030. It extracts Teletext Data from the video signal, regenerates Teletext Clock and synchronizes the text display to the television syncs. The integrated circuit is intended to work in conjunction with CCT (Computer Controlled Teletext), EUROM or other compatible devices.

Features

- Adaptive data slicer
- Data clock regenerator
- Adaptive sync separator, horizontal phase detector and 6 MHz VCO forming display phase locked loop (PLL)

QUICK REFERENCE DATA

Supply voltage (pin 16)	V_{CC}	typ.	12 V
Supply current (pin 16)	I_{CC}	typ.	70 mA
Video input amplitude (pin 27) (peak-to-peak value)			
pin 2 LOW	$V_{27\text{-}13(p\text{-}p)}$	typ.	1 V
pin 2 HIGH	$V_{27\text{-}13(p\text{-}p)}$	typ.	2,5 V
Storage temperature range	T_{stg}		−20 to + 125 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT-117).

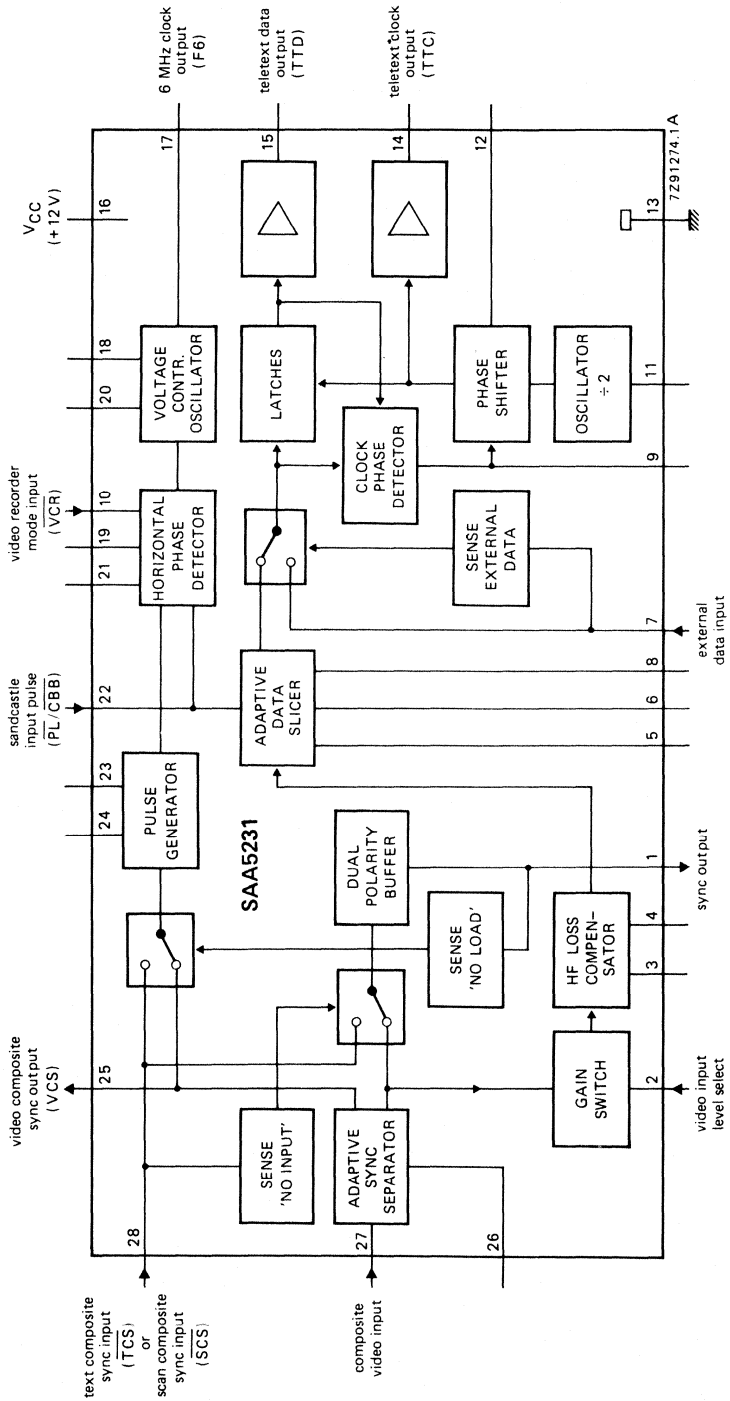


Fig. 1 Block diagram.

PINNING

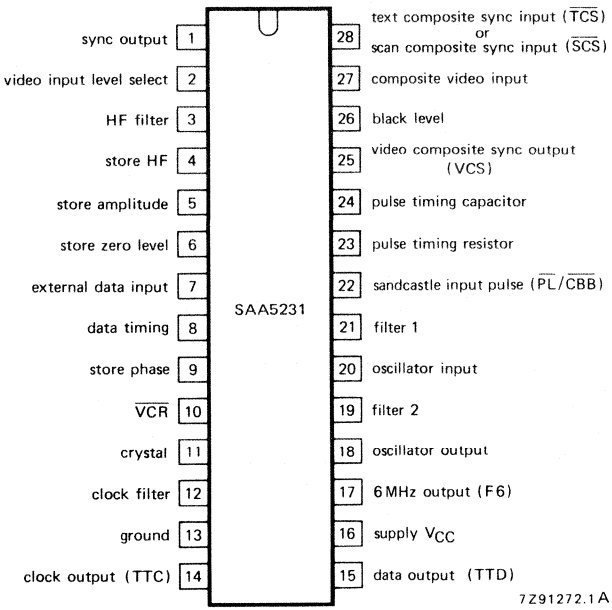


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 16)	V_{CC}	max. 13,2 V
Storage temperature range	T_{stg}	−20 to + 125 °C
Operating ambient temperature	T_{amb}	0 to + 70 °C

CHARACTERISTICS

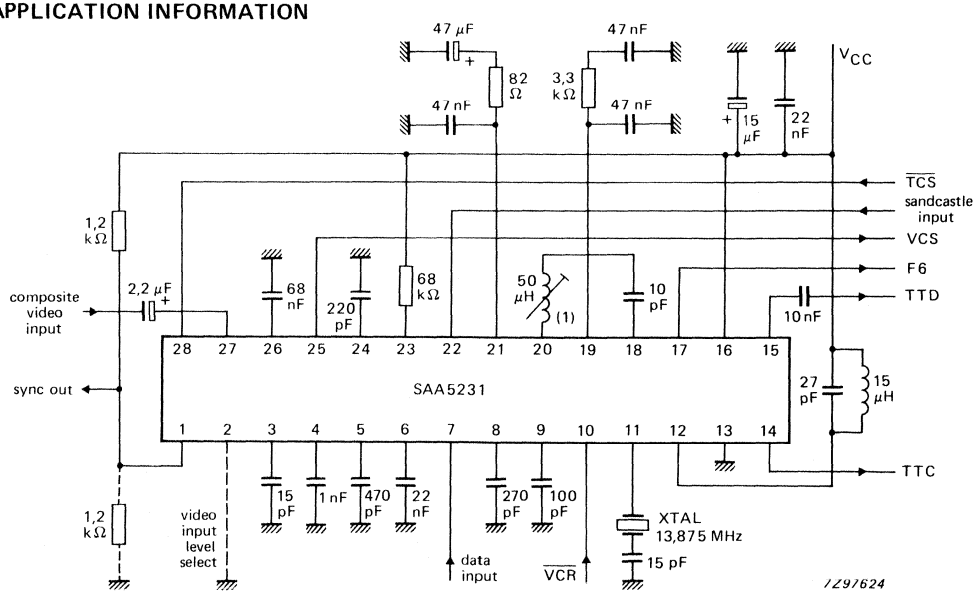
V_{CC} = 12 V; T_{amb} = 25 °C with external components as shown in application circuits unless otherwise stated.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{CC}	10,8	12,0	13,2	V
Supply current	I_{CC}	50	70	105	mA
Video input and sync separator					
Video input amplitude (sync to white) (peak-to-peak value)					
video input select level LOW (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	0,7	1	1,4	V
video input select level HIGH (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude (peak-to-peak value)	$V_{27\text{-}13(p\text{-}p)}$	0,1	–	1	V
Video input level select					
Input voltage LOW	$V_{2\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{2\text{-}13}$	2,0	–	5,5	V
Input current LOW	I_2	0	–	−150	μA
Input current HIGH	I_2	0	–	1	mA
Text composite sync input ($\overline{TCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{28\text{-}13}$	2,0	–	7,0	V
Scan composite sync input ($\overline{SCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	1,5	V
Input voltage HIGH	$V_{28\text{-}13}$	3,5	–	7,0	V
Select video sync from pin 1					
Input current (pin 28)					
at V_{28} = 0 to 7 V	I_{28}	−40	−70	−100	μA
at V_{28} = 10 V to V_{CC}	I_{28}	−5	–	+ 5	μA
Video composite sync output (VCS)					
Output voltage LOW	$V_{25\text{-}13}$	0	–	0,4	V
Output voltage HIGH	$V_{25\text{-}13}$	2,4	–	5,5	V
D.C. output current LOW	I_{25}	–	–	0,5	mA
D.C. output current HIGH	I_{25}	–	–	−1,5	mA
Sync separator delay time	t_d	0,25	0,35	0,40	μs

parameter	symbol	min.	typ.	max.	unit
Dual polarity buffer output					
$\overline{TCS}$ amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	0,20	0,45	0,65	V
Video sync amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	–	–	1	V
Output current	I_1	–3	–	+ 3	mA
D.C. output voltage					
R_L to ground (0 V)	$V_{1\text{-}13}$	1,0	1,4	2,0	V
R_L to V_{CC} (12 V)	$V_{1\text{-}13}$	9,0	10,1	11,0	V
Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)					
Phase lock pulse (PL)					
PL on (LOW)	$V_{22\text{-}13}$	0	–	3	V
PL off (HIGH)	$V_{22\text{-}13}$	3,9	–	5,5	V
Blanking pulse (CBB)					
CBB on (LOW)	$V_{22\text{-}13}$	0	–	0,5	V
CBB off (HIGH)	$V_{22\text{-}13}$	1,0	–	5,5	V
Input current	I_{22}	–10	–	+ 10	μA
Phase locked loop (PLL)					
Phase detector timing					
Pulse duration using composite video	t_p	2,0	2,4	2,8	μs
using scan composite sync	t_p	3,0	3,5	4,0	μs
time PL must be LOW to make VCO run-free	t_L	100	–	–	μs
6 MHz clock output (F6)					
A.C. output voltage (peak-to-peak value)	$V_{17\text{-}13(p\text{-}p)}$	1	2	3	V
A.C. and d.c. output voltage range	$V_{17\text{-}13(max)}$	4	–	8,5	V
Rise and fall time	t_r; t_f	20	–	40	ns
Load capacitance	$C_{17\text{-}13}$	–	–	40	pF
Video recorder mode input ($\overline{VCR}$)					
VCR-mode on (LOW)	$V_{10\text{-}13}$	0	–	0,8	V
VCR-mode off (HIGH)	$V_{10\text{-}13}$	2,0	–	V_{CC}	V
Input current	I_{10}	–10	–	+ 10	μA

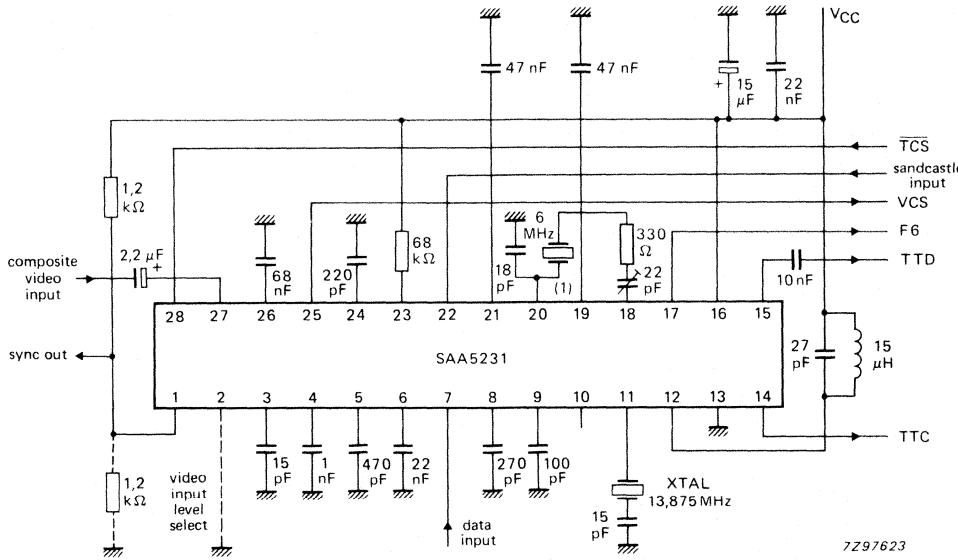
parameter	symbol	min.	typ.	max.	unit
Data slicer					
Data amplitude of video input (pin 27)					
video input level select LOW (pin 2)	V_{27-13}	0,30	0,46	0,70	V
video input level select HIGH (pin 2)	V_{27-13}	0,75	1,15	1,75	V
Teletext clock output					
A.C. output voltage (peak-to-peak value)	$V_{14-13(p-p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	V_{14-13}	3,0	4,0	5,0	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r; t_f	20	30	45	ns
Delay of falling edge relative to other edges of TTD	t_d	−20	0	+ 20	ns
Teletext data output					
A.C. output voltage (peak-to-peak value)	$V_{15-13(p-p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	V_{15-13}	3,0	4,0	5,0	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r; t_f	20	30	45	ns

APPLICATION INFORMATION



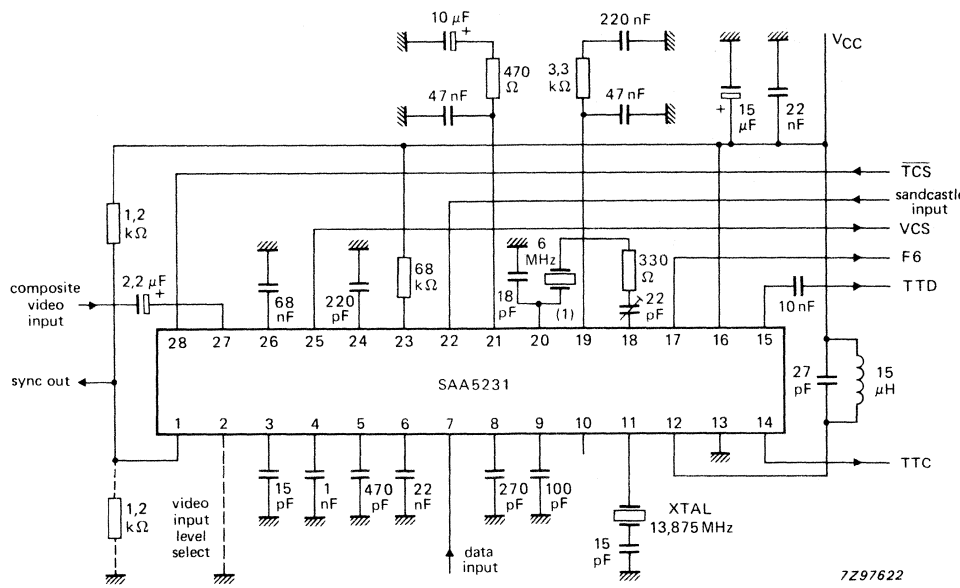
(1) Coil: 50 µH at 1 kHz, C_o = 4 pF. Adjust the free-running frequency to 6000 kHz ± 30 kHz.

Fig. 3a Application circuit using L/C circuit in PLL.



(1) Quartz crystal e.g. catalogue number 4322 143 04101. Adjust the free-running frequency to 6000,2 kHz ± 0,2 kHz.

Fig. 3b Application circuit using quartz crystal in PLL.



(1) Ceramic resonator e.g. Kyocera KBR 6,0 M. Adjust the free-running frequency to 6010 kHz ± 5 kHz.

Fig. 3c Application circuit using ceramic resonator in PLL.

Component specifications

Specifications of some external components in Figs 3a, 3b and 3c.

Quartz crystal 13,875 MHz; Figs 3a, 3b and 3c

Load resonance frequency (f) 13,875 MHz; adjustment tolerance $\pm 40 \cdot 10^{-6}$

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance maximum $\pm 30 \cdot 10^{-6}$

Resonance resistance (R_r) typical 10 Ω maximum 60 Ω

Motional capacitance (C_1) typical 19 fF

Static parallel capacitance (C_0) typical 5 pF

Fixed inductance Figs 3a, 3b and 3c

Inductance (L) 15 μH ± 20%

Quality factor (Q) minimum 20

Variable inductance Fig. 3a

Inductance (L) 50 μH at 1 kHz

Static parallel capacitance (C_0) typical 4 pF

Quartz crystal Fig. 3b

Preferred type 4322 143 04101

Load resonance frequency (f) 6 MHz; adjustment tolerance $\pm 40 \cdot 10^{-6}$

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance $\pm 30 \cdot 10^{-6}$

Resonance resistance (R_r) 60 Ω

Motional capacitance (C_1) typical 28 fF

Static parallel capacitance (C_0) typical 7 pF

Ceramic resonator; Fig. 3c

Preferred type KBR 6,0 M, Kyocera

Load resonance frequency (f) 6 MHz; adjustment tolerance ± 0,5%

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance maximum ± 0,3%

Resonance resistance (R_r) typical 6 Ω

Motional capacitance (C_1) typical 9 pF

Static parallel capacitance (C_0) typical 60 pF

Ageing (10 years) f maximum ± 0,3%

The function is quoted against the corresponding pin number.

1. **Synch output to TV**

   Output with dual polarity buffer, a load resistor to 0 V or + 12 V selects positive-going or negative-going syncs.

2. **Video input level select**

   When this pin is LOW a 1 V video input level is selected. When the pin is not connected it floats HIGH selecting a 2,5 V video input level.

3. **HF filter**

   The video signal for the h.f.-loss compensator is filtered by a 15 pF capacitor connected to this pin.

4. **Store h.f.**

   The h.f. amplitude is stored by a 1 nF capacitor connected to this pin.

5. **Store amplitude**

   The amplitude for the adaptive data slicer is stored by a 470 pF capacitor connected to this pin.

6. **Store zero level**

   The zero level for the adaptive data slicer is stored by a 22 nF capacitor connected to this pin.

7. **External data input**

   Current input for sliced teletext data from external device.
   Active HIGH level (current), low impedance input.

8. **Data timing**

   A 270 pF capacitor is connected to this pin for timing of the adaptive data slicer.

9. **Store phase**

   The output signal from the clock phase detector is stored by a 100 pF capacitor connected to this pin.

10. **Video tape recorder mode ($\overline{\text{VCR}}$)**

    Signal input to command PLL into short time constant mode. Not used in application circuit Fig. 3b or Fig. 3c.

11. **Crystal**

    A 13,875 MHz crystal, 2 x data rate, connected in series with a 15 pF capacitor is applied via this pin to the oscillator and divide-by-two to provide the 6,9375 MHz clock signal.

12. **Clock filter**

    A filter for the 6,9375 MHz clock signal is connected to this pin.

13. **Ground (0 V)**

14. **Teletext clock output (TTC)**

    Clock output for CCT (Computer Controlled Teletext).

APPLICATION INFORMATION (continued)

15. **Teletext data output (TTD)**

    Data output for CCT.

16. **Supply voltage V_{CC} (+ 12 V typ.)**

17. **Clock output (F6)**

    6 MHz clock output for timing and sandcastle generation in CCT.

18. **Oscillator output (6 MHz)**

    A series resonant circuit is connected between this pin and pin 20 to control the nominal frequency of the VCO.

19. **Filter 2**

    A filter with a short time constant is connected to this pin for the horizontal phase detector. It is used in the video recorder mode and while the loop is locking up.

20. **Oscillator input (6 MHz)**

    See pin 18.

21. **Filter 1**

    A filter with a long time constant is connected to this pin for the horizontal phase detector.

22. **Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)**

    This input accepts a sandcastle waveform, which is formed from PL and CBB from the CCT. Signal timing is shown in Fig. 4.

23. **Pulse timing resistor**

    The current for the pulse generator is defined by a 68 kΩ resistor connected to this pin.

24. **Pulse timing capacitor**

    The timing of the pulse generator is determined by a 220 pF capacitor connected to this pin.

25. **Video composite sync output (VCS)**

    This output signal is for CCT.

26. **Black level**

    The black level for the adaptive sync separator is stored by a 68 nF capacitor connected to this pin.

27. **Composite video input (CVS)**

The composite video signal is input via a 2,2 μF clamping capacitor to the adaptive sync separator.

28. **Text composite sync input ($\overline{\text{TCS}}$)/Scan composite sync input ($\overline{\text{SCS}}$)**

$\overline{\text{TCS}}$ is input from CCT or $\overline{\text{SCS}}$ from external sync circuit. $\overline{\text{SCS}}$ is expected when there is no load resistor at pin 1. If pin 28 is not connected the sync output on pin 1 will be the composite video input at pin 27, internally buffered.

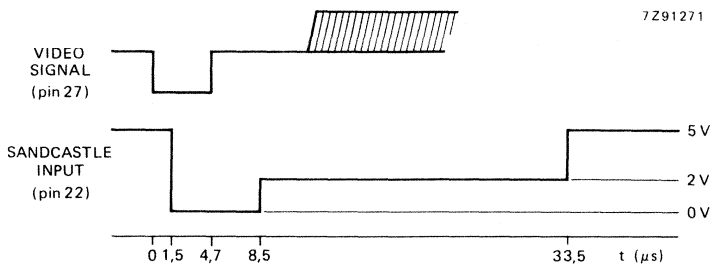


Fig. 4 Sandcastle waveform and timing.

DATALINE SLICER

The SAA5235 is a bipolar integrated circuit for dataline receivers. It extracts the dataline signal from the video signal and regenerates the dataline clock. It also provides signals for the dataline decoder.

Features

- Adaptive dataline slicer
- Dataline clock regenerator
- Buffered clock and data outputs
- Buffered composite sync output
- Gain switch for the video input signal

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 16)	V_{CC}	10,8	12	13,2	V
Supply current at V_{CC} = 12 V	I_{CC}	–	70	–	mA
Composite video amplitude					
pin 2 LOW	$V_{27(p\text{-}p)}$	–	1	–	V
pin 2 floating	$V_{27(p\text{-}p)}$	–	2,5	–	V
Storage temperature range	T_{stg}	−20	–	+ 125	°C
Operating ambient temperature	T_{amb}	0	–	+ 70	°C

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT-117).

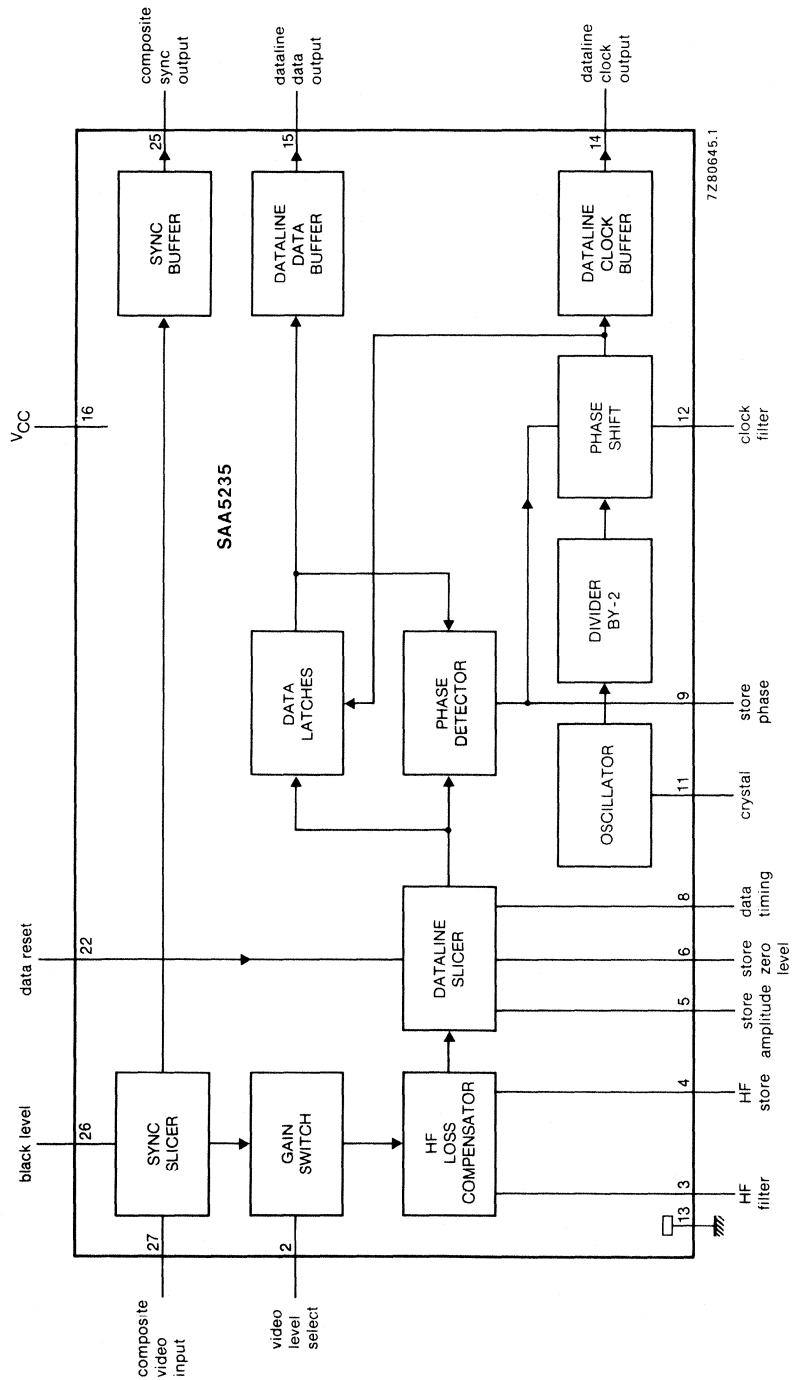


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 16)	V_{CC}	–	–	13,2	V
Storage temperature range	T_{stg}	−20	–	125	°C
Operating ambient temperature	T_{amb}	0	–	70	°C

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; with external components as shown in Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 16)	V_{CC}	10,8	12,0	13,2	V
Supply current	I_{CC}	–	70	–	mA
Video input and sync separator					
Composite video input (CV)					
Level select input (pin 2) LOW	$V_{27\text{-}13(p\text{-}p)}$	0,7	1	1,4	V
Level select input (pin 2) HIGH	$V_{27\text{-}13(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude	$V_{27\text{-}13(p\text{-}p)}$	0,1	–	1	V
Video level select					
Input voltage					
LOW	$V_{2\text{-}13}$	0	–	0,8	V
HIGH	$V_{2\text{-}13}$	2,0	–	5,5	V
Input current					
LOW	I_2	0	–	−150	μA
HIGH	I_2	0	–	1	mA
Video composite sync output (VCS)					
Output voltage					
LOW	$V_{25\text{-}13}$	0	–	0,4	V
HIGH	$V_{25\text{-}13}$	2,4	–	5,5	V
Sync separator delay time	t_d	–	0,35	–	μs
Data reset input (DAR)					
Input voltage					
LOW (DAR on)	$V_{22\text{-}13}$	0	–	0,5	V
HIGH (DAR off)	$V_{22\text{-}13}$	1,0	–	5,5	V
Input current	I_{22}	−10	–	10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Dataline slicer					
Dataline amplitude (pin 27)					
Video select voltage (pin 2) LOW	$V_{27\text{-}13(p\text{-}p)}$	0,3	0,46	0,7	V
Video select (pin 2) FLOATING	$V_{27\text{-}13(p\text{-}p)}$	0,75	1,15	1,75	V
Dataline clock output (DLCL)					
A.C. output voltage	$V_{14\text{-}13(p\text{-}p)}$	2,5	3,5	4,5	V
Output voltage (d.c.) centre	$V_{14\text{-}13}$	–	4,0	–	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r, t_f	20	30	45	ns
Delay of falling edge relative to edges of DLD	t_d	−20	–	20	ns
Dataline data output (DLD)					
A.C. output voltage	$V_{15\text{-}13(p\text{-}p)}$	2,5	3,5	4,5	V
Output voltage (d.c.) centre	$V_{15\text{-}13}$	–	4,0	–	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r, t_f	20	30	45	ns

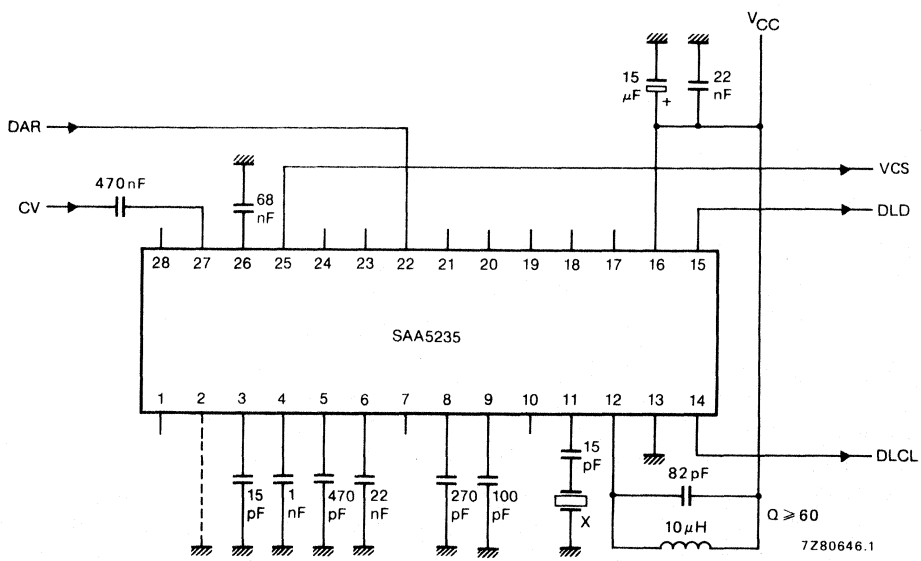


Fig. 2 Application circuit; crystal X; f = 10,000 MHz.

APPLICATION DATA

Composite video input CV (pin 27)

The composite video has to be fed into this input via a clamp capacitor. The input amplitude depends on the position of the gain switch at pin 2.

Video gain switch (pin 2)

Low level selects 1 V video input amplitude at pin 27. With no connection pin 2 floats HIGH, selecting 2,5 V video amplitude.

Black level (pin 26)

A capacitor connected to this pin stores the black level for the adaptive sync separator.

Video composite sync output VCS (pin 25)

This pin provides a video composite sync signal for the data-line decoder.

H.F. loss compensator (pins 3 and 4)

The h.f. loss compensator needs two capacitors for operation. The capacitor at pin 3 filters the video signal for the h.f. loss compensator. The h.f. amplitude information is stored in the capacitor connected to pin 4.

Dataline slicer (pins 5, 6 and 8)

A capacitor at pin 5 stores the amplitude information for the dataline slicer. The zero-level information is stored in a capacitor connected to pin 6. The capacitor at pin 8 is necessary for timing of the dataline slicer.

Phase detector (pin 9)

The phase information which is detected from the phase detector is stored in a capacitor connected to pin 9.

Oscillator (pin 11)

The one-pin oscillator needs a 10,000 MHz crystal (2 x dataline frequency) connected to pin 11.

Phase shifter (pin 12)

A clock filter for the dataline clock of 5,000 MHz is connected to the phase shifter at pin 12.

Outputs

The dataline clock output DLCL (pin 14) and the dataline data output DLD (pin 15) provide signals for the dataline decoder.

Data reset DAR (pin 22)

The dataline slicer needs a reset signal each line, for signal timing see Fig. 3.

APPLICATION DATA (continued)

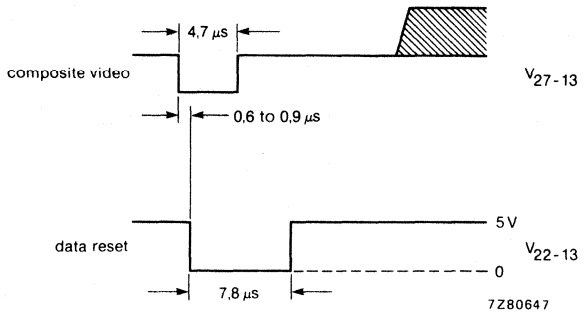


Fig. 3 Data-reset input signal timing in relation to composite video signal.

ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUIT (ECCT)

GENERAL DESCRIPTION

The SAA5243 is a MOS N-channel integrated circuit which performs all the digital logic functions of a 625-line World System Teletext decoder. It operates in conjunction with the teletext video processor SAA5231, standard static RAMs and is controlled via the 2-wire I²C bus. The device can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 2 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language section of up to seven different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I²C bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- $\overline{\text{Odd}}$/even field output for de-interlaced displays

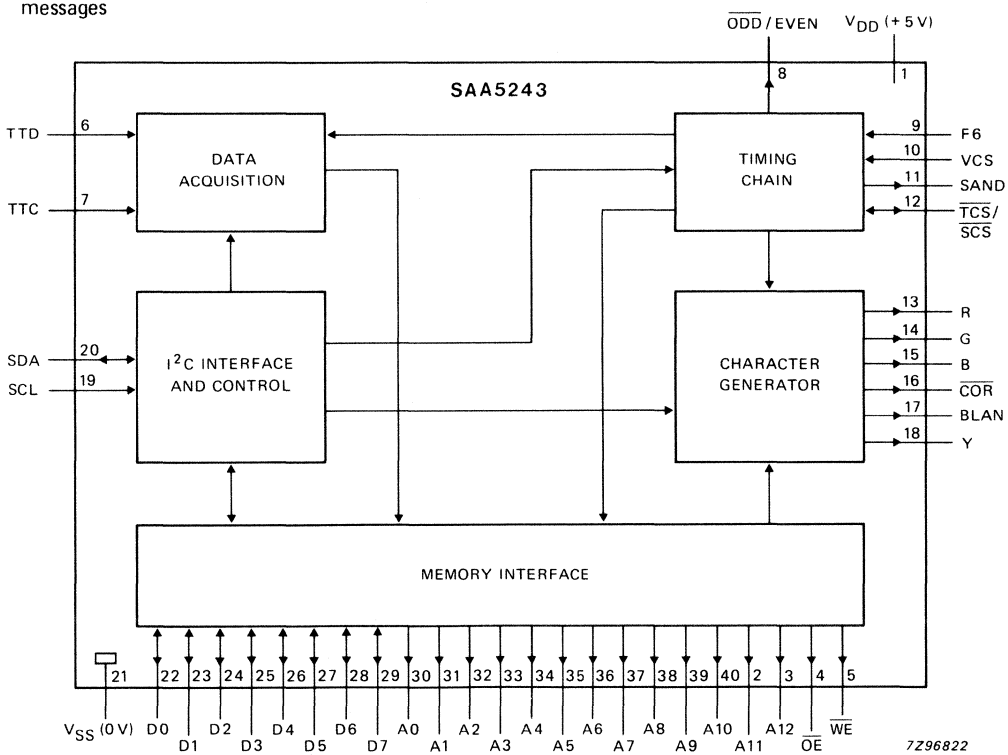


Fig. 1 Block diagram.

PACKAGE OUTLINES 40-lead DIL; plastic (SOT-129).

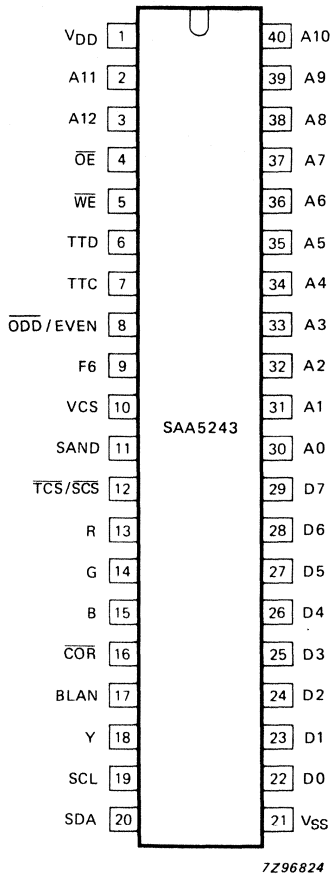


Fig. 2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.
5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct d.c. level following the external a.c. coupling.

7	TTC	**Teletext Clock**: 6,9375 MHz clock input from the SAA5231. It is internally a.c. coupled to an active clamp input buffer.
8	$\overline{\text{ODD}}$/EVEN	**$\overline{\text{Odd}}$/Even**: for interlaced mode, the output changes once per field at 2 μs before the end of line 311 (624). The output is high for even fields and low for odd fields.
9	F6	**Character display clock**: 6 MHz clock input from the SAA5231. It is internally a.c. coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync**: input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{\text{TCS}}$/$\overline{\text{SCS}}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig. 6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue**: these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{\text{COR}}$	**Contrast Reduction**: open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking**: open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground**: open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	DO-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 1)	V_{DD}	−0,3 to + 7,5	V
Input voltage range			
VCS, SDA, SCL, D0-D7	V_I	−0,3 to + 7,5	V
TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$	V_I	−0,3 to + 10,0	V
Output voltage range			
SAND, A0-A12, $\overline{OE}$, $\overline{WE}$, D0-D7, SDA, $\overline{ODD}$/EVEN, R, G, B, BLAN, $\overline{COR}$, Y	V_O	−0,3 to + 7,5	V
$\overline{TCS}/\overline{SCS}$	V_O	−0,3 to + 10,0	V
Storage temperature range	T_{stg}	−20 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2,0	–	7,0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
D.C. input voltage range	V_I	−0,3	–	+ 10,0	V
A.C. input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1,0	–	7,0	V
A.C. input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1,5	–	7,0	V
Input peaks relative to 50% duty cycle	± V_P	0,2	–	3,5	V
TTC clock frequency	f_{TTC}	–	6,9375	–	MHz
F6 clock frequency	f_{F6}	–	6,0	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5,5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5,5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0,4 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
at I_{OH} = 0,1 mA	V_{OH}	2,4	–	6,0	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5,5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0,5	V
Output fall time between 3,0 V and 1,0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5,5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0,4 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0,2 mA	V_{OL}	0	–	0,25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1,1	–	3,1	V

CHARACTERISTICS (continued)

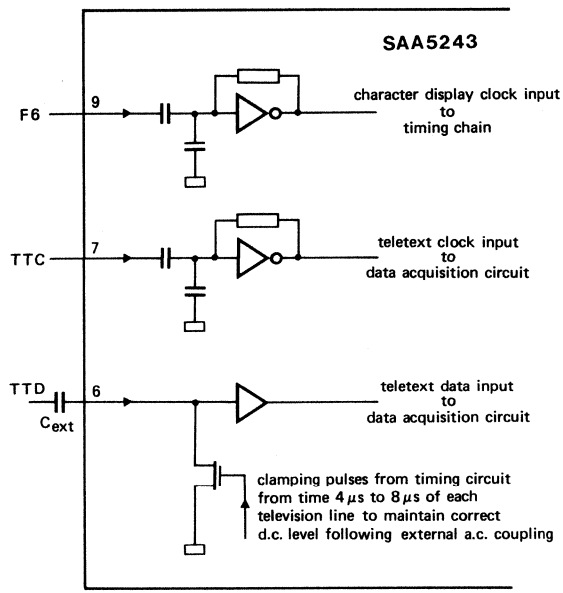
parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4,0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0,4 V and 0,9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3,3 V and 3,8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3,8 V and 0,4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0,4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1,0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6,0	V
Output fall time with a load resistor of 1,2 kΩ to 6 V and measured between 5,5 V and 1,5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1,2 kΩ to 6 V and measured on the falling edges at 3,5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns

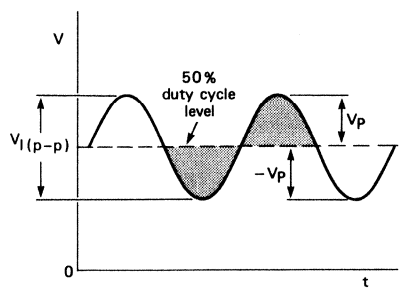
DEVELOPMENT DATA

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig. 3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2,0 V; data stable 0 $\leqslant$ 0,8 V (see Fig. 4).
5. The TTC and F6 inputs have internal clamping diodes and are a.c. coupled (see Fig. 3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C bus timing see Fig. 8.
8. For details of RAM timing see Fig. 9.
9. For details of synchronization timing see Fig. 5.
10. For details of display output timing see Fig. 7.
11. The I^2C bus timings are referred to V_{IH} = 3 V and V_{IL} = 1,5 V. For waveforms see Fig. 8.
12. The memory interface timings are referred to V_{IL} = 1,5 V. For waveforms see Fig. 9.



(a)



shaded regions equal in area

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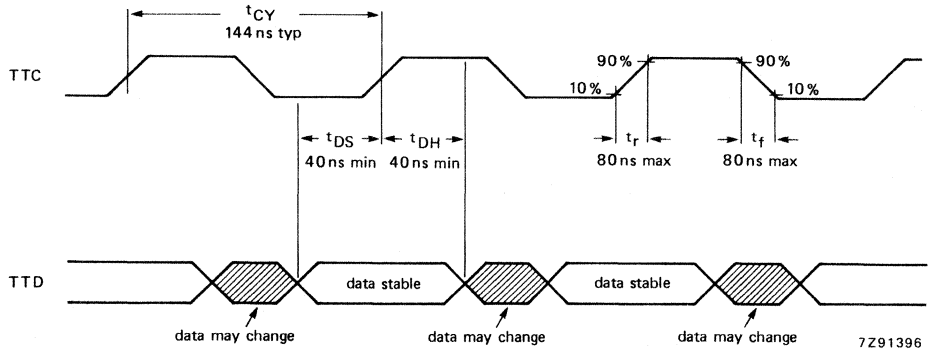
(b)

Fig. 3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2,0 V; 0 is $\leqslant$ 0,8 V.

Fig. 4 Teletext data input timing.

DEVELOPMENT DATA

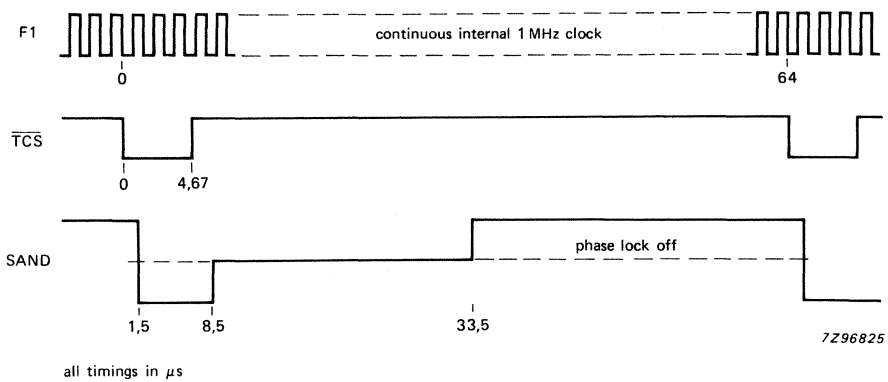
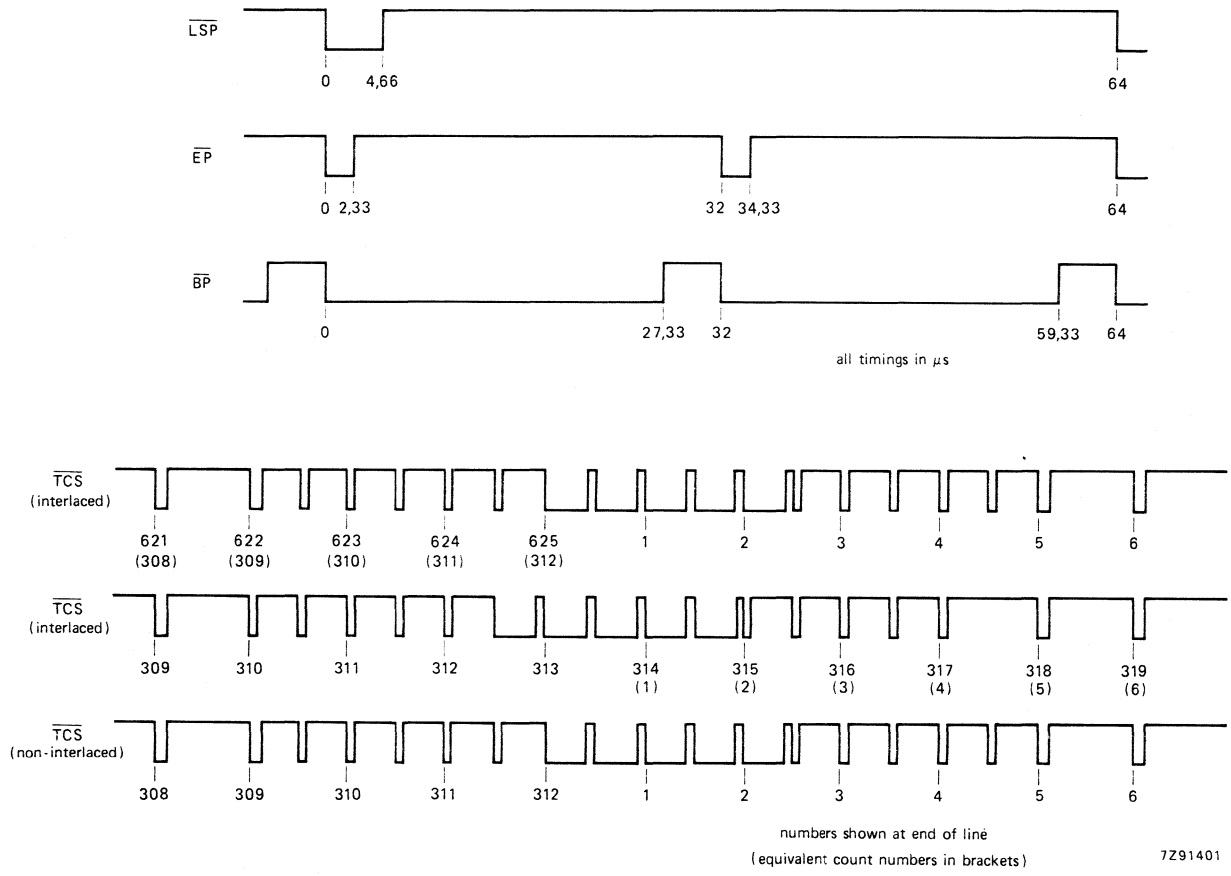


Fig. 5 Synchronization timing.



Line sync pulses ($\overline{\text{LSP}}$), equalizing pulses ($\overline{\text{EP}}$) and broad pulses ($\overline{\text{BP}}$) are combined to provide the text composite sync waveform ($\overline{\text{TCS}}$) as shown. All timings measured from falling edge of $\overline{\text{LSP}}$ with a tolerance of ± 100 ns.

Fig. 6 Composite sync waveforms.

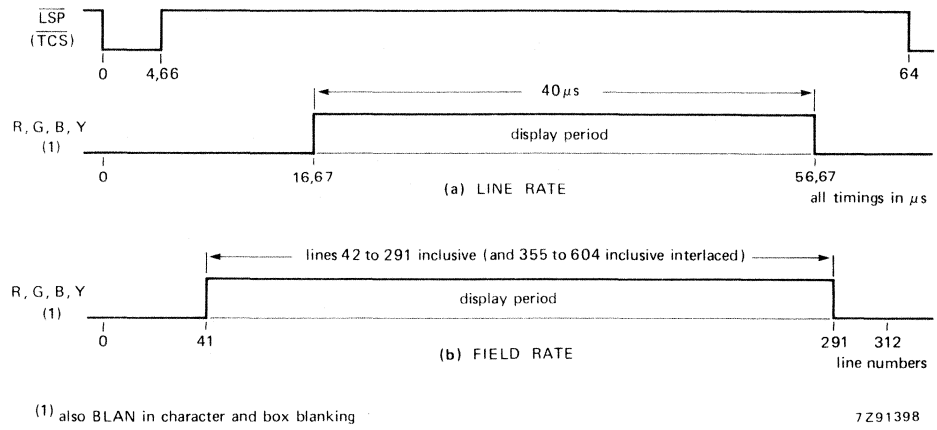


Fig. 7 Display output timing (a) line rate (b) field rate.

DEVELOPMENT DATA

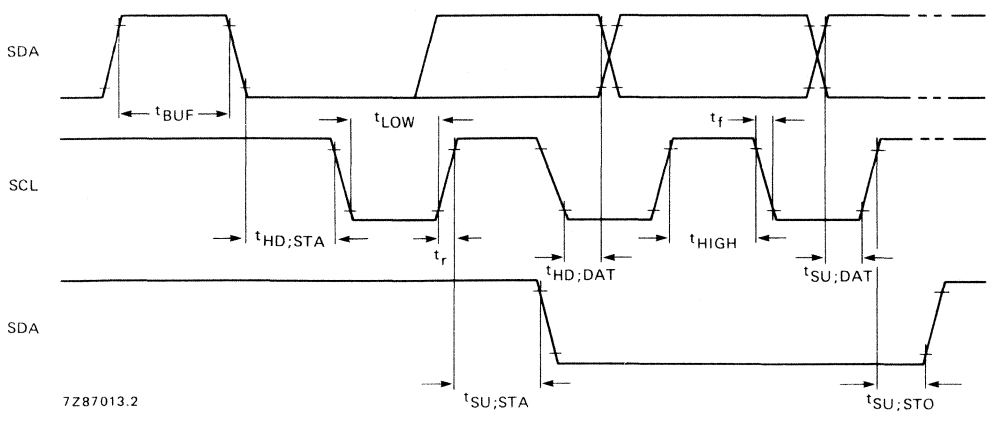


Fig. 8 I²C bus timing.

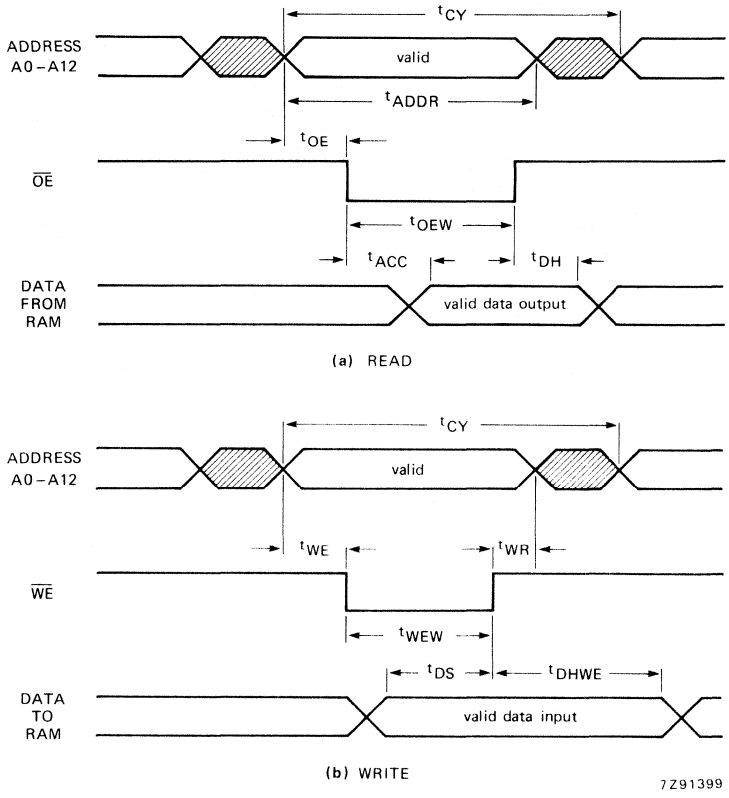
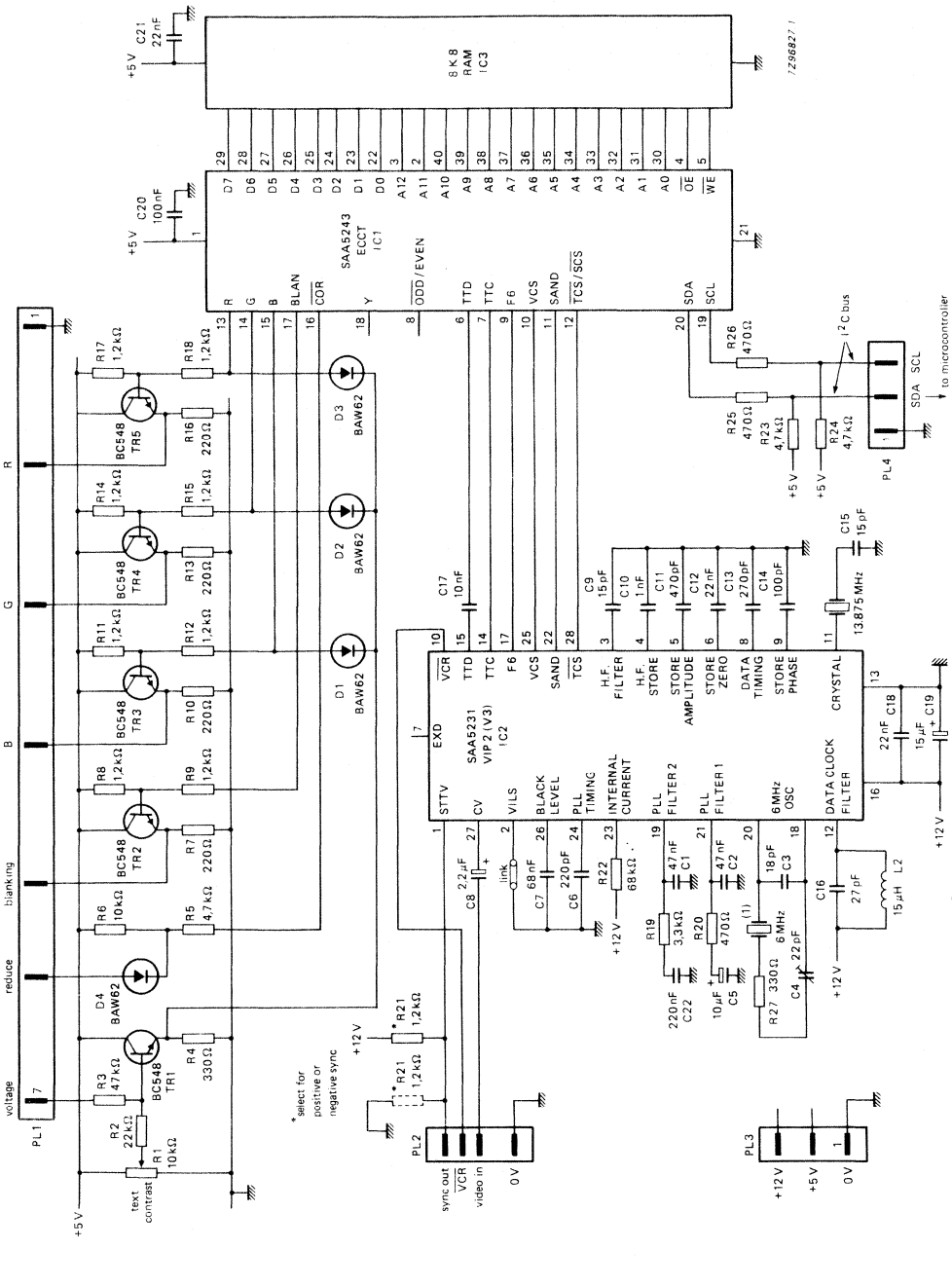


Fig. 9 Memory interface timing (a) read (b) write.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Ceramic resonator e.g. Kyocera KBR 6,0 M.

Fig. 10 ECCT based multi-page decoder circuit diagram.

APPLICATION INFORMATION (continued)

ECCT page memory organization

The organization of a page memory is shown in Fig. 11. The ECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF ECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

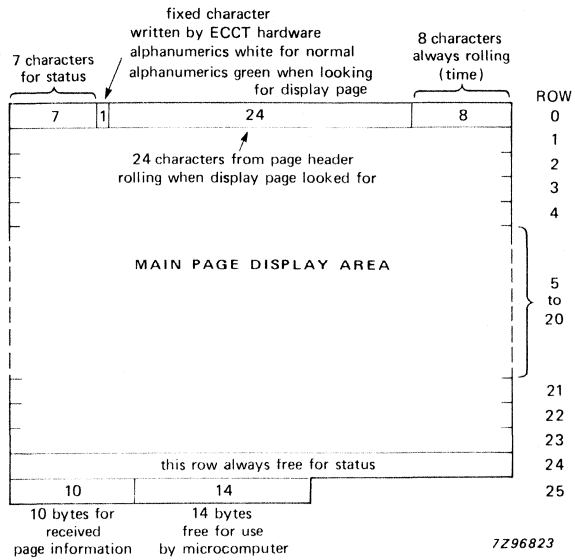


Fig. 11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
PBLF	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

Row 0

Row 0 is for the page header. The first seven columns (o to 6) are free for status messages. The eigth is an alphanumeric white or green control character, written automatically by ECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

ECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 ECCT register map

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	GHOST ROW ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
–	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
–	–	–	–	–	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
–	–	–	–	CLEAR MEM.	A2	A1	A0	R8	Active chapter
–	–	–	R4	R3	R2	R1	R0	R9	Active row
–	–	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

– bit does not exist

DEVELOPMENT DATA

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

APPLICATION INFORMATION (continued)

Table 2 (continued)

Where:

R1 Mode

T0, T1	interlace/non-interlace 312/313 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
7 + $\overline{\text{P}}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation
R2 Page request address	
START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode

BOX ON 0 (1-23, $\overline{\text{24}}$)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C bus.

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for D0 CARE bits.
When the D0 CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the D0 CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

CHARACTER SETS

The UK teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14 as shown in Table 4. The basic 96 character sets differs only in the 13 national option characters as indicated in Table 7 with reference to their table position in the basic character matrix shown in Table 6. ECCT automatically decodes transmission bits C12 to C14. Other combinations of C12 to C14 are defaulted to English in SAA5243P/E. With 8-bit decoding the character matrices are shown in Table 5.

Table 4 Selection of national character sets (SAA5243P/E)

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH	SPANISH
C12	0	0	0	0	1	1
C13	0	0	1	1	0	0
C14	0	1	0	1	0	1

Where:

PHCB page header control bits.

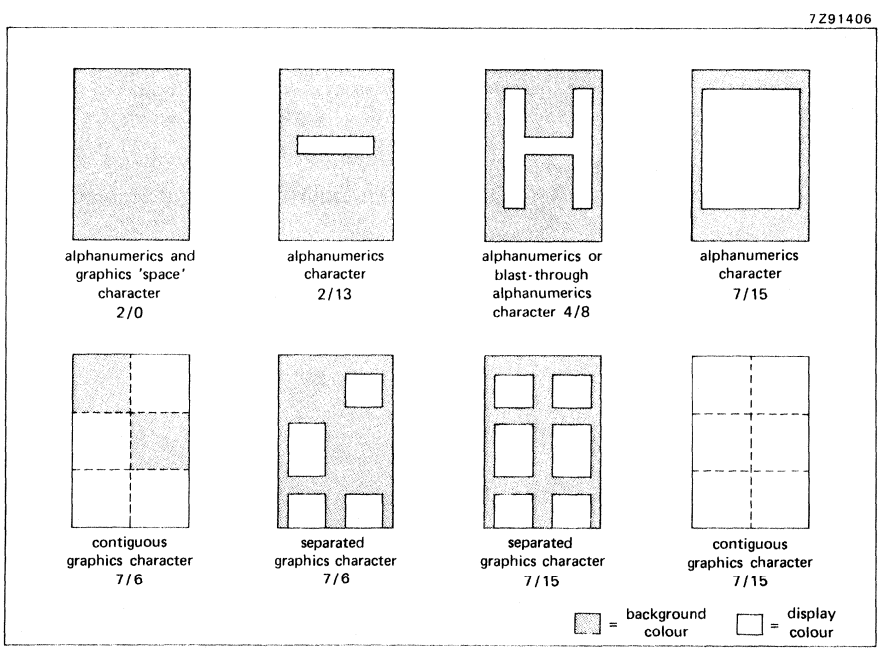


Fig. 12 Character format.

Table 5 Character data input decoding (SAA5243E)

BIT	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	row \ column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
	0	0	0	0																						
	0	0	0	1																						
	0	0 or 1	0	0																						
	0	0 or 1	0	1																						
	0	1	1	0																						
	0	1	1	1																						
	1	0	1	0																						
	1	0	1	1																						
0	0	0	0	0	alpha-numerics black	graphics black					§	P	°		p		@	É	é	à	i	Á
0	0	0	1	1	alpha-numerics red	graphics red	!		1		A	Q	a		q		—	é	ù	è	¿	À
0	0	1	0	2	alpha-numerics green	graphics green	"		2		B	R	b		r		¼	ä	à	â	ü	È
0	0	1	1	3	alpha-numerics yellow	graphics yellow	#		3		C	S	c		s		£	#	£	é	ç	ł
0	1	0	0	4	alpha-numerics blue	graphics blue	$		4		D	T	d		t		$	¤	$	ï	$	Ï
0	1	0	1	5	alpha-numerics magenta	graphics magenta	%		5		E	U	e		u				ä	Ä	ö	ó
0	1	1	0	6	alpha-numerics cyan	graphics cyan	&		6		F	V	f		v				õ	Õ	ö	ò
0	1	1	1	7	alpha-numerics white **	graphics white	'		7		G	W	g		w		?		·	Ç	Ñ	Ú
1	0	0	0	8	flash	conceal display	(		8		H	X	h		x		‖	ö	ò	ô	ñ	æ
1	0	0	1	9	steady **	contiguous graphics **	)		9		I	Y	i		y		¾	å	è	û	è	Æ
1	0	1	0	10	end box **	separated graphics	*		:		J	Z	j		z		÷	ü	ì	ç	à	ð
1	0	1	1	11	start box	ESC *	+		;		K	Ä	k		ä		←	Ä	°	ë	á	Ð
1	1	0	0	12	normal height **	black background **	,		<		L	Ö	l		ö		½	Ö	ç	ê	é	ø
1	1	0	1	13	double height	new background	—		=		M	Ü	m		ü		→	Å	→	ù	í	Ø
1	1	1	0	14	SO *	hold graphics	.		>		N	^	n		ß		↑	Ü	↑	î	ó	þ
1	1	1	1	15	SI *	release graphics **	/		?		O	_	o				#	_	#	#	ú	Þ

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DEVELOPMENT DATA

* These control characters are reserved for compatibility with other data codes.

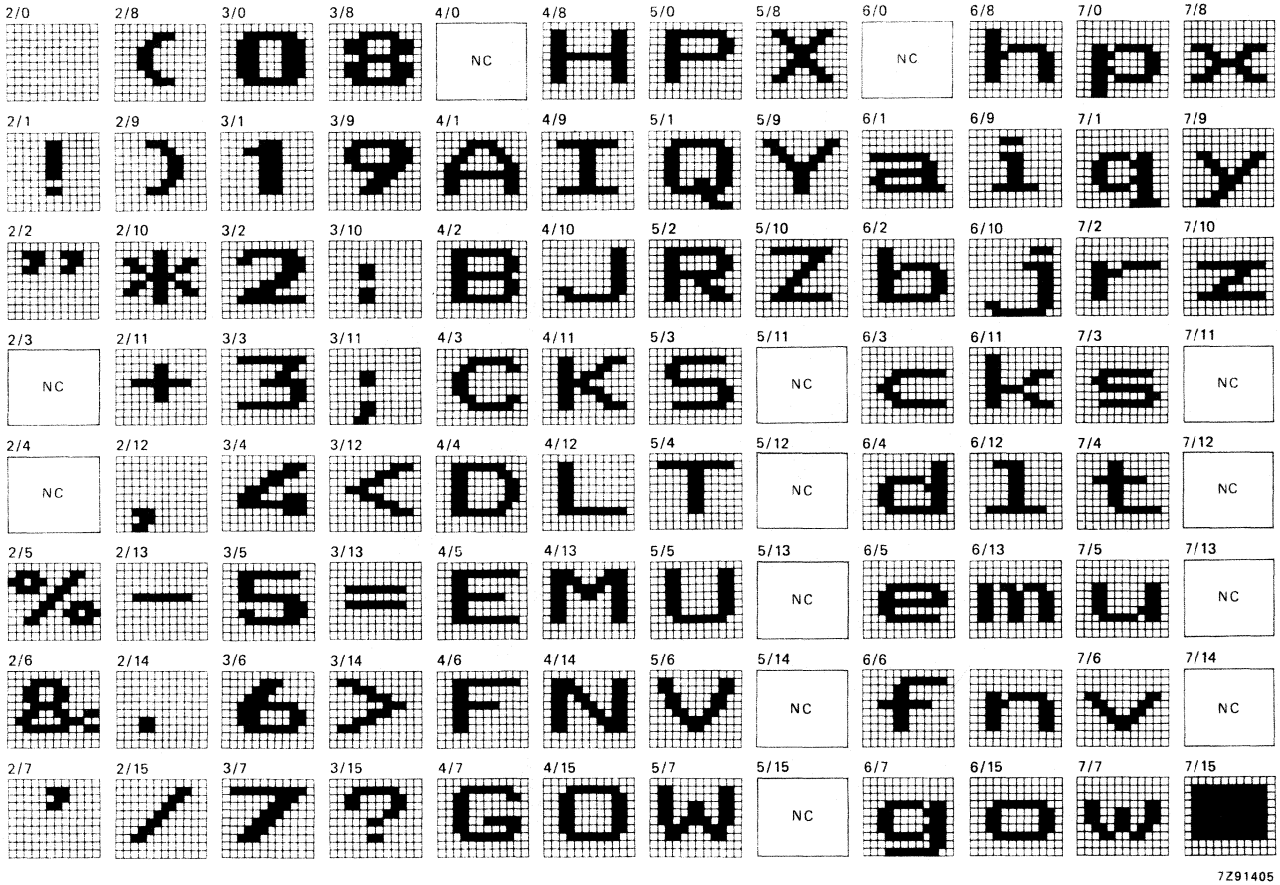
** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Notes to Table 5

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. The SAA5243E national option characters are shown in Table 7.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters to combine with character 8/5.
7. With bit 8 = 0 national option characters will be decoded according to the setting of control bits C12 to C14 (see Table 4).

Table 6 SAA5243 basic character matrix

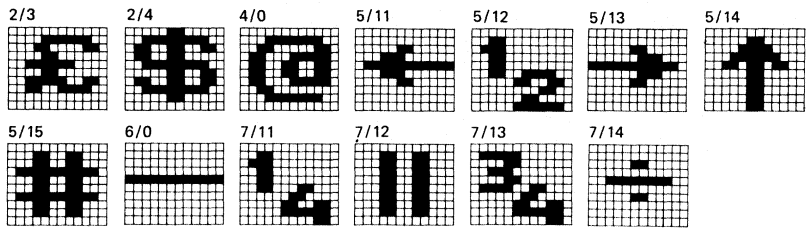


Where: NC national option character position.

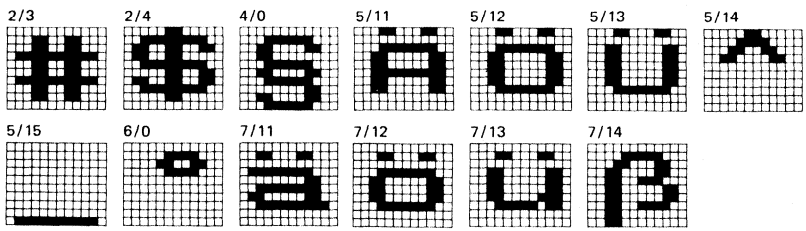
APPLICATION INFORMATION (continued)

Table 7 SAA5243E character set (national option characters)

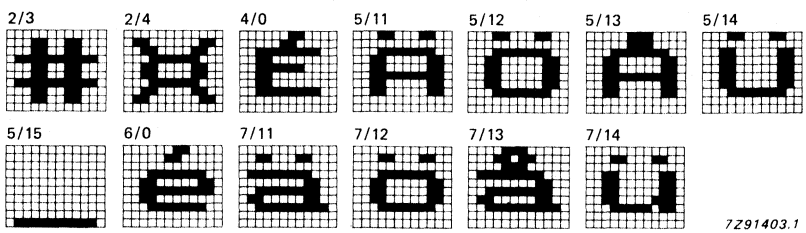
ENGLISH



GERMAN



SWEDISH



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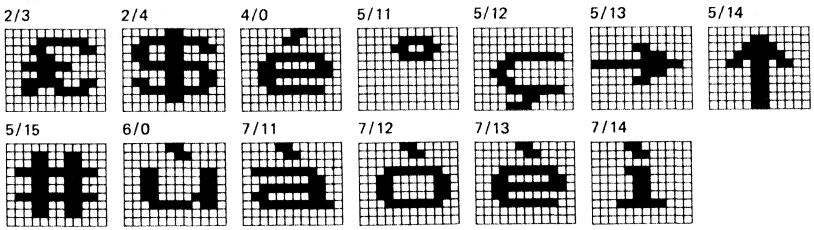
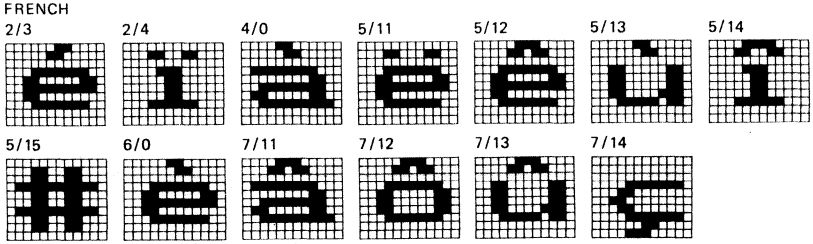
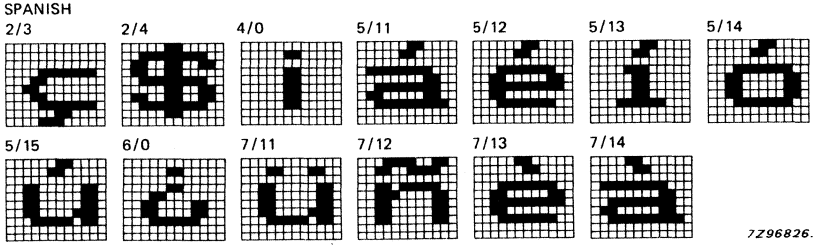
ITALIAN



FRENCH



SPANISH



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INTERFACE FOR DATA ACQUISITION AND CONTROL (for multi-standard teletext systems)

GENERAL DESCRIPTION

The SAA5250 is a CMOS Interface for Data Acquisition and Control (CIDAC) designed for use in conjunction with the Video Input Processor (SAA5230) in a multi-standard teletext decoder. The device retrieves data from a user selected channel (channel demultiplexer), as well as providing control signals and consecutive addressing space necessary to drive a 2 K bytes buffer memory.

The system operates in accordance with the following transmission standards:

- French Didon Antiope specification D2 A4-2 (DIDON)
- North American Broadcast Teletext specification (NABTS)
- U.K. teletext (CEEFAX)

Features

- 7,5 MHz maximum conversion rate
- Three prefixes; DIDON, NABTS and U.K. teletext (CEEFAX)
- Mode without prefix
- Internal calculation of the validation (VAL) and colour burst blanking (CBB) signals, if programmed
- Programmable framing code and channel numbers
- Error parity calculation or not (odd parity)
- Hamming processing of the prefix byte
- Full channel or VBI reception
- Slow/fast mode (detection of page flags or not)
- Maximum/default format up to 63 bytes
- Addressing space of 2 K bytes of the static memory
- Multiplexed address/data information is compatible with Motorola or Intel microcontrollers
- CIDAC is 'MOTEL' compatible

PACKAGE OUTLINES

SAA5250P: 40-lead DIL; plastic (SOT-129).
SAA5250T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

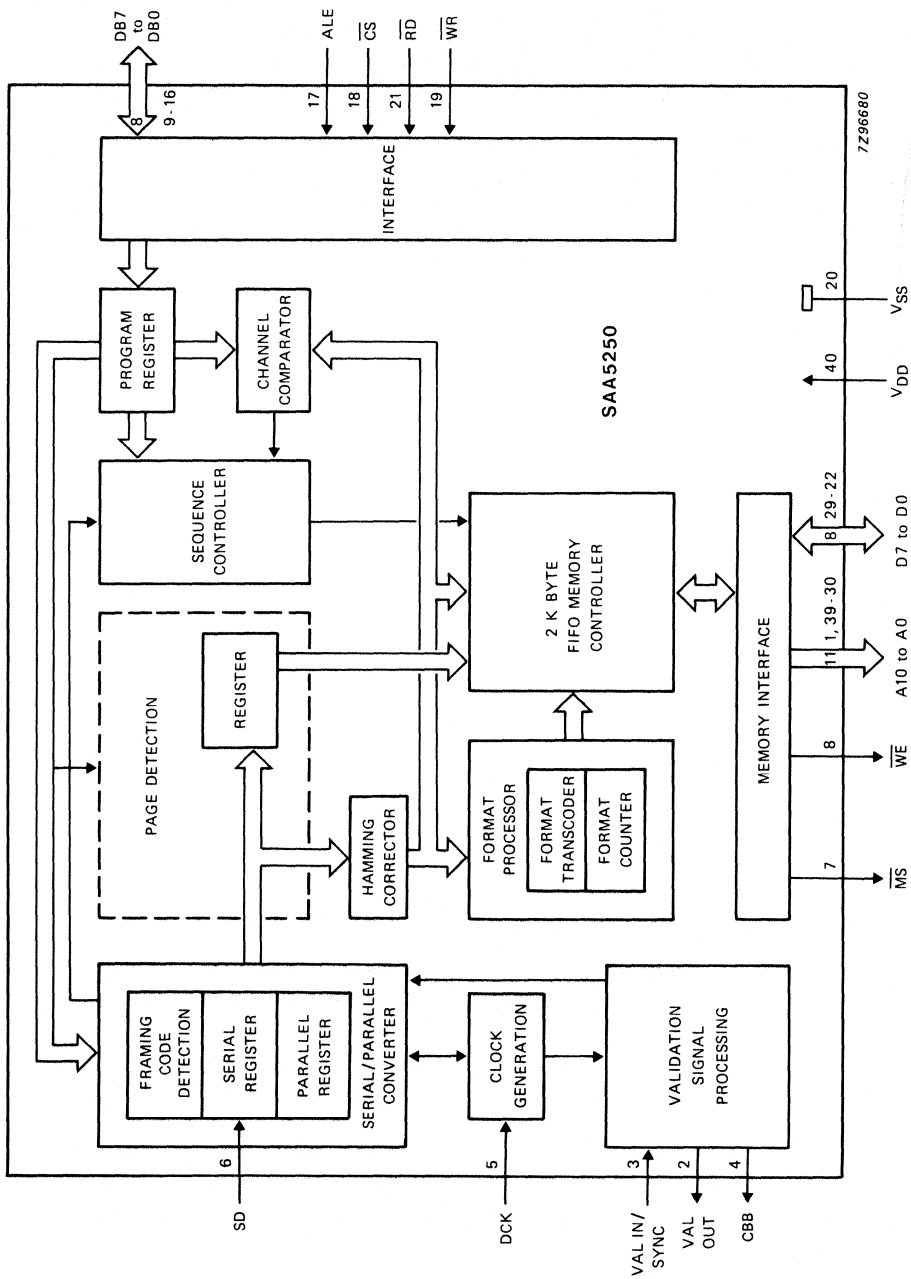


Fig. 1 Block diagram.

DEVELOPMENT DATA

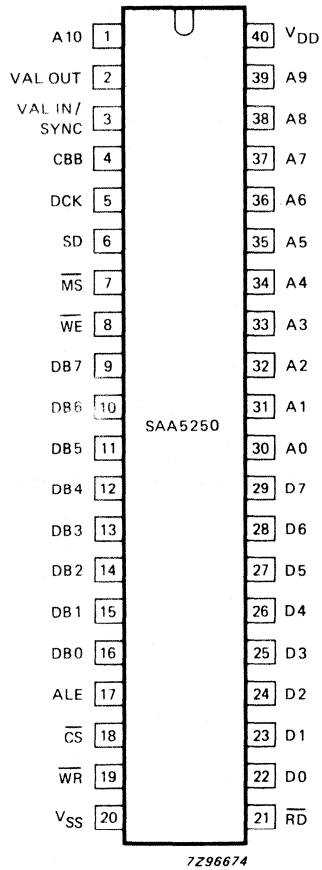


Fig. 2 Pinning diagram.

PINNING FUNCTION

mnemonic	pin no.	function
A10 and A0 to A9	1 and 30 to 39	Memory address outputs used by CIDAC to address a 2 K byte buffer memory
VAL OUT	2	Validation output signal used to control the location of the window for the framing code
VAL IN/SYNC	3	Validation input signal (line signal) used to give or calculate a window for the framing code detection
CBB	4	Colour burst blanking output signal used by the SAA5230 as a data slicer reset pulse
DCK	5	Data clock input, in synchronization with the serial data signal
SD	6	Serial data input, arriving from the demodulator
$\overline{MS}$	7	Chip enable output signal for buffer memory selection
$\overline{WE}$	8	Write command output for the buffer memory
DB7 to DB0	9 to 16	8-bit three state input/output data/address bus used to transfer commands, data and status between the CIDAC registers and the CPU
ALE	17	Demultiplexing input signal for the CPU data bus
$\overline{CE}$	18	Chip enable input for the SAA5250
$\overline{WR}$	19	Write command input (when LOW)
V_{SS}	20	ground
$\overline{RD}$	21	Read command input (when LOW)
D0 to D7	22 to 29	8-bit three state input/output data bus used to transfer data between CIDAC and the buffer memory
V_{DD}	40	+5 V power supply

FUNCTIONAL DESCRIPTION

Microcontroller interface

The microcontroller interface communicates with the CPU via the handshake signals DB7 – DB0, ALE, CS, $\overline{RD}$, $\overline{WR}$. The microcontroller interface produces control commands as well as programming the registers to write their contents or read incoming status/data information from the buffer memory. The details of the codes used to address the registers are given in Table 2.

The CIDAC is 'MOTEL' compatible (MOTEL compatible means it is compatible with standard **Mo**torola or **Intel** microcontrollers). It automatically recognizes the microcontroller type (such as the 6801 or 8501) by using the ALE signal to latch the state of the $\overline{RD}$ input. No external logic is required.

Table 1 Recognition signals

CIDAC	8049/8051 timing 1	6801/6805 timing 2
ALE	ALE	AS
$\overline{RD}$	$\overline{RD}$	DS, E, $\Phi 2$
$\overline{WR}$	$\overline{WR}$	R/$\overline{W}$

Table 2 CIDAC register addressing

codes						
R	W	CS	DB2	DB1	DB0	function
1	0	0	0	0	0	write register R0
1	0	0	0	0	1	write register R1
1	0	0	0	1	0	write register R2
1	0	0	0	1	1	write register R3
1	0	0	1	0	0	write register R4
1	0	0	1	0	1	write register R5
1	0	0	1	1	0	write command register R6 (initialization command)
1	0	0	1	1	1	write register R7
0	1	0	0	0	0	read status
0	1	0	0	0	1	read data register
0	1	0	0	1	0	test (not used)
0	1	0	0	1	1	test (not used)

DEVELOPMENT DATA

Register organization

R0 register

Table 3 R0 Register contents

R04 slow/fast mode	R03 parity	R02 to R00 used prefixes
0 = slow mode 1 = fast mode	0 = no parity control 1 = odd parity	000 = DIDON long 001 = DIDON medium 010 = DIDON short 011 = not used 100 = U.K. teletext 101 = NABTS 110, 111 = without prefix

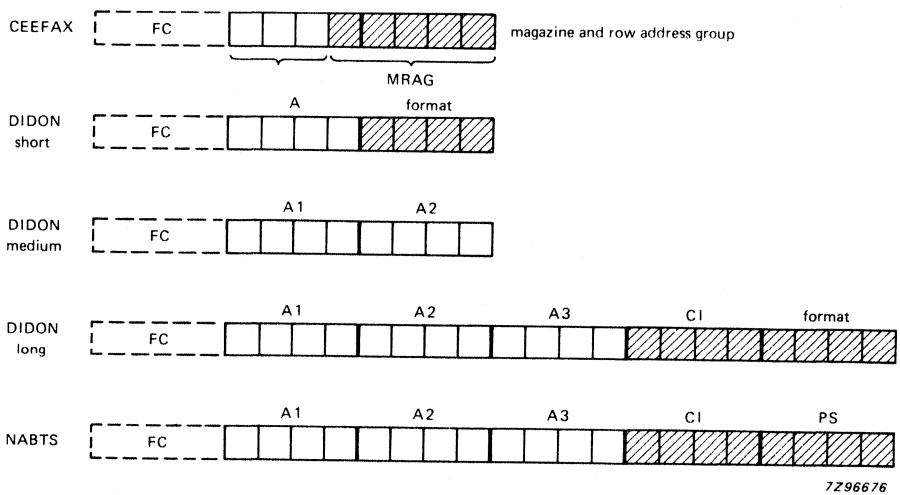


Fig. 3 Five prefixes.

All of the bytes (see Fig. 3) are Hamming protected. The hatched bytes are always stored in the memory in order to be processed by the CPU (see section 'Prefix processing'). In the mode without prefix all of the bytes which follow the framing code are stored in the memory until the end of the data packet, the format is then determined by the contents of the R3 register.

If R03 = 0; no parity control is carried out and the 8-bits of the incoming data bytes are stored in the fifo memory.

If R03 = 1; the 8th bit of the bytes following the prefix (data bytes) represents the result of the odd parity control.

If R04 = 0; the device operates in the slow mode. The CIDAC retrieves data from the user selected magazine (see section 'R1 and R2') and without searching for a start to a page stores the data into the FIFO memory.

If R04 = 1; the device operates in the fast mode. Prior to writing into the FIFO memory, the CIDAC searches for a start to a page which is variable due to the different prefixes:

- DIDON (long, medium and short): using the redundant bytes, SOH RS, X RS and SOH X (where X is a bit affected by a parity error)
- NABTS, the least significant bit of the PS byte is set to 1
- U.K. teletext, ROW = 0

R1 register

Table 4 R1 Register contents

R17 VAL IN/SYNC	R16 to R14 format table	R13 to R10 channel numbers (first digit)
1 = VAL 0 = SYNC	000 = list 1 001 = list 2 010 = list 3 011 = list 4 1XX = maximum/default value used (R3)	first digit hexadecimal value

Note

X = don't care

If VAL IN/SYNC = 1; the line signal immediately produces a validation signal for the framing code detection.

If VAL OUT = 0; the line signal is used as a starting signal for an internally processed validation signal (see Fig. 15). The framing code window width is fixed at 13 clock periods and the delay is determined by the contents of the R5 register (R56 to R50).

At any moment the user is able to ensure that the framing code window is correctly located. This is accomplished by the VAL OUT pin reflecting the internal validation signal. A CBB signal with programmable width (see section 'R7 register') can also be generated, this is used as a data slicer reset pulse by the SAA5230. The line signal is used as the starting point of the internal CBB signal width fixed by the contents of the R7 register.

If R16 = 0; then bits R15 and R14 provide the format table number using DIDON long and short prefixes (see Table 6).

If R16 = 1; then the format is determined by the contents of the R3 register.

The bits R13 to R10 represent the first channel number to be checked in the prefix. In U.K. teletext mode only 3 bits are required, so R13 = X.

Table 5 Format table

format byte B8, B6, B4 and B2	list 1	list 2	list 3	list 4
0000	0	0	0	0
0001	1	1	1	1
0010	2	2	2	2
0011	3	3	3	3
0100	4	5	6	7
0101	8	9	10	11
0110	12	13	14	15
0111	16	17	18	19
1000	20	21	22	23
1001	24	25	26	27
1010	28	29	30	31
1011	32	33	34	35
1100	36	37	38	39
1101	40	41	42	43
1110	44	45	46	47
1111	48	49	50	51

Note

B8 = MSB and B2 = LSB.

R2 register

Table 6 R2 Register contents

R27 to R24	R23 to R20
channel number, third digit	channel number, second digit
(hexadecimal value, third digit)	(hexadecimal value, second digit)

Note

R27 and R23 = MSB and R24 and R20 = LSB

The R2 register provides the other two parts of the channel number (depending on the prefix) that require checking.

R3 register

Table 7 R3 register contents

R35 to R30 6-bit format maximum/default value
000000 = 0 000001 = 1 – – – 111111 = 63

This 6-bit byte gives:

- In the DIDON long and short mode, a maximum format in case of corrupted transmission (multiple errors on the Hamming corrector)
- A possible 63-bit format for all types of prefix

R4 register

Table 8 R4 register contents

R47 to R40
8-bit register used for storing the framing code value which will be compared with the third byte of each data line

R5 register

Table 9 R5 register contents

R57 negative/positive	R56 to R50 synchronization delay
0 = negative edge for sync signal 1 = positive edge for sync signal	7-bit sync delay, giving a maximum delay of $(2^7 - 1) \times 10^6$ µs/F (Hz)

Note

F = data clock acquisition frequency (DCK).

Using R57 it is possible to start the internal synchronization delay (t_{DVAL}) on the positive or negative edge.

R6 write command register

This is a fictitious register. Only the address code (see Table 2) is required to reset the CIDAC. See Table 11 for the status of the FIFO memory on receipt of this command.

R7 register

Table 10 R7 register contents

R75 to R70
6-bit register used to give a maximum colour burst blanking signal of: $(2^6 - 1) \times 10^6$ µs/F (Hz)

Note

F = data clock acquisition frequency.

Fifo status register (read R0 register)

Table 11 Fifo register contents

DB2 to DB0		
DB2 = 1 memory empty	DB1 = 1, data not present in the read data register	DB0 = 0 memory not full

Once the relevant prefix and the right working modes have been given by the corresponding registers, a write command to the R6 register enables the CIDAC to accept and process serial data.

Channel comparator

This is a four bit comparator which compares the three user hexadecimal defined values in R1 and R2 to the corresponding bytes of the prefix coming from the Hamming corrector. If the three bytes match, the internal process of the prefix continues. If they do not match the CIDAC returns to a wait state until the next broadcast data package is received.

FIFO memory controller

The FIFO memory contains all the necessary functions required for the control of the 11-bit address memory (2 K byte). The functions contained in the FIFO memory are as follows:

- write address register (11-bits)
- read address register (11-bits)
- memory pointer (11-bits)
- address multiplexer (11-bits)
- write data register (8-bits)
- read data register (8-bits)
- data multiplexer
- control logic

The FIFO memory provides the memory interface with the following:

- 11-bit address bus (A10 to A0)
- 8-bit data bus (D7 to D0)
- two control signals, memory select ($\overline{MS}$) and write enable ($\overline{WE}$)

Operation

The CIDAC uses the same clock signal for data acquisition and internal processing, this allows the CIDAC to have a write and a read cycle during each character period (see Fig. 13). The first half of the character period is a write cycle and the second half is a read cycle. Consequently, for an 8 MHz bit rate the maximum memory cycle time is 500 ns.

When the first data byte is written into the FIFO memory, thus transferred into the read register, the FIFO memory enters the status shown in Table 12.

Table 12 FIFO status

DB2 to DB0		
DB2 = 1 memory empty	DB1 = 0 data available	DB0 = 0 memory not full

When the FIFO memory is full two events occur:

- the write address register points to the next address after the last written address
- when new data is to be written, the memory select signal output ceases

Memory interface

The memory interface contains all the buffers for the memory signals mentioned in the section 'FIFO memory controller'.

Page detection

This part of the CIDAC contains a parallel register with logic which detects (only in fast mode) a start of a page or data group (see section 'R0 register').

Hamming correction (see Tables 13 and 14)

The Hamming correction provides (see section 'Prefix processing'):

- hexadecimal value of the Hamming code
- accept/reject code signal
- parity information

Table 13 Hamming correction (coding)

Hexadecimal notation	B8	B7	B6	B5	B4	B3	B2	B1
0	0	0	0	1	0	1	0	1
1	0	0	0	0	0	0	1	0
2	0	1	0	0	1	0	0	1
3	0	1	0	1	1	1	1	0
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	0	1	1
6	0	0	1	1	1	0	0	0
7	0	0	1	0	1	1	1	1
8	1	1	0	1	0	0	0	0
9	1	1	0	0	0	1	1	1
A	1	0	0	0	1	1	0	0
B	1	0	0	1	1	0	1	1
C	1	0	1	0	0	0	0	1
D	1	0	1	1	0	1	1	0
E	1	1	1	1	1	1	0	1
F	1	1	1	0	1	0	1	0

Note

$B7 = B8 \oplus B6 \oplus \overline{B4}$
$B5 = B6 \oplus \overline{B4} \oplus \overline{B2}$
$B3 = \overline{B4} \oplus \overline{B2} \oplus B8$
$B1 = \overline{B2} \oplus B8 \oplus B6$

$\oplus$ = exclusive OR gate function
B8, B6, B4 and B2 = data bits
B7, B5, B3 and B1 = redundancy bits

Table 14 Hamming correction (decoding)

A	B	C	D	interpretation	information
1	1	1	1	no error	accepted
0	0	1	0	error on B8	corrected
1	1	1	0	error on B7	accepted
0	1	0	0	error on B6	corrected
1	1	0	0	error on B5	accepted
1	0	0	0	error on B4	corrected
1	0	1	0	error on B3	accepted
0	0	0	0	error on B2	corrected
0	1	1	0	error on B1	accepted
A.B.C = 0			1	multiple errors	rejected

Note

$A = B8 \oplus B6 \oplus B2 \oplus B1$
$B = B8 \oplus B4 \oplus B3 \oplus B2$
$C = B6 \oplus B5 \oplus B4 \oplus B2$
$D = B8 \oplus B7 \oplus B6 \oplus B5 \oplus B4 \oplus B3 \oplus B2 \oplus B1$

$\oplus$ = exclusive OR gate function

Format processing

The format processing consists of two parts:

part 1

A format transcoder produces a 6-bit code (up to 63) and uses the following as inputs:

- DIDON long and short prefixes;
  hamming corrected code (4-bits)
  accept/reject code condition
  table number (see section 'R1 register', bits R15 and R14)
- Other prefixes (R16 = 1)
- 6-bit maximum/default format (see section 'R3 register')

part 2

A format counter operating at the character clock frequency which receives the 6-bit code from the format transcoder and is used to check the data packet length following the prefix.

Serial/parallel converter

The serial/parallel converter consists of three parts:

- An 8-bit shift register which receives the SD input and operates at the bit frequency (DCK).
- An 8-bit parallel register used for storage.
- A framing code detection circuit. This logic circuit compares the 8-bits of the R4 register with that of the serial register. If seven bits out of eight match (in coincidence with a validation window), it produces a start signal for a new teletext data line to the sequence controller.

Clock generation

The clock generator does the following:

- acts as a buffer for the DCK clock
- generates the character clock

As soon as a framing code has been detected, a divide by 8 counter is initialized and the character clock is started. The clock drives the following:

- sequence controller
- parallel registers
- format counter

Processing of VAL and CBB signals

The circuit has one input (VAL IN/SYNC) and two outputs (VAL OUT and CBB). The circuit consists of:

- 7-bit counter operating at DCK frequency which produces the framing code validation pulse delay
- 7-bit comparator which compares the contents of the R5 register (bits R56 to R50) to the bit counter
- a 6-bit counter operating at DCK frequency which produces the CBB pulse width
- 6-bit comparator which compares the contents of the R7 register (bits R75 to R70) to the bit counter
- control logic required to provide the start condition for the VAL signal and the CBB pulse width (on the negative or positive edge of the sync signal)

The CBB signal usefulness occurs when the associated video processor:

- has no sandcastle pulse to send back to the demodulator
- carries out the synchronization of the time base clock. In this event the CBB acts as a data slicer reset pulse

The VAL OUT is a control signal which reflects the internal framing code window.

Prefix processing (see Table 21)

Figs 4 to 9 show the acquisition flow charts for each prefix type coded in the R0 register (bits R02 to R00).

As soon as an initialization command is received by the CIDAC, a write command to the R6 register (only the address is significant), is ready to receive data from a dedicated channel number and store the data in the FIFO memory (explained in the following paragraphs, each paragraph being dedicated to an individual type of prefix).

DIDON long (see Fig. 4)

In this mode, the continuity index, format and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 15 Continuity index processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	CI3	CI2	CI1	CI0

Table 16 Format processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	F5	F4	F3	F2	F1	F0

Note

A/R = 0, if rejected
A/R = 1, if accepted
X = don't care

DIDON mediun (see Fig. 5)

Only data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

DIDON short (see Fig. 6)

In this mode, format and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 17 Format processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	F5	F4	F3	F2	F1	F0

NABTS (see Fig. 7)

In this mode, the continuity index, packet structure and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 18 Continuity index processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	CI3	CI2	CI1	CI0

Table 19 Packet structure processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	PS3	PS2	PS1	PS0

U.K. teletext (see Fig. 8)

In this mode, the magazine and row address group (two bytes) and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a flag detection.)

Table 20 Magazine and row address group processing results

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	RW4	RW3	RW2	RW1	RW0

Without prefix

All the data following the framing code are stored in the FIFO memory.

Table 21 Prefix processing

prefixes	construction of prefixes	bytes stored in FIFO memory during slow mode	bytes stored in FIFO memory during fast mode
DIDON long	A1, A2, A3, CI, F and D	CI, F and D	CI*, F* and D*
DIDON medium	A1, A2 and D	D	D*
DIDON short	A1, F and D	F and D	F* and D*
NABTS	A1, A2, A3 CI, PS and D	CI, PS and D	CI*, PS* and D*
U.K. teletext	MRAG and D	MRAG and D	MRAG* and D*
without prefix		all bytes of the data packet following the framing code are written into the FIFO memory	

Note

* = after page/flag detection
A1, A2, A3 are channel numbers
CI = continuity index
F = format
PS = packet structure
D = data
MRAG = magazine and row address group

DEVELOPMENT DATA

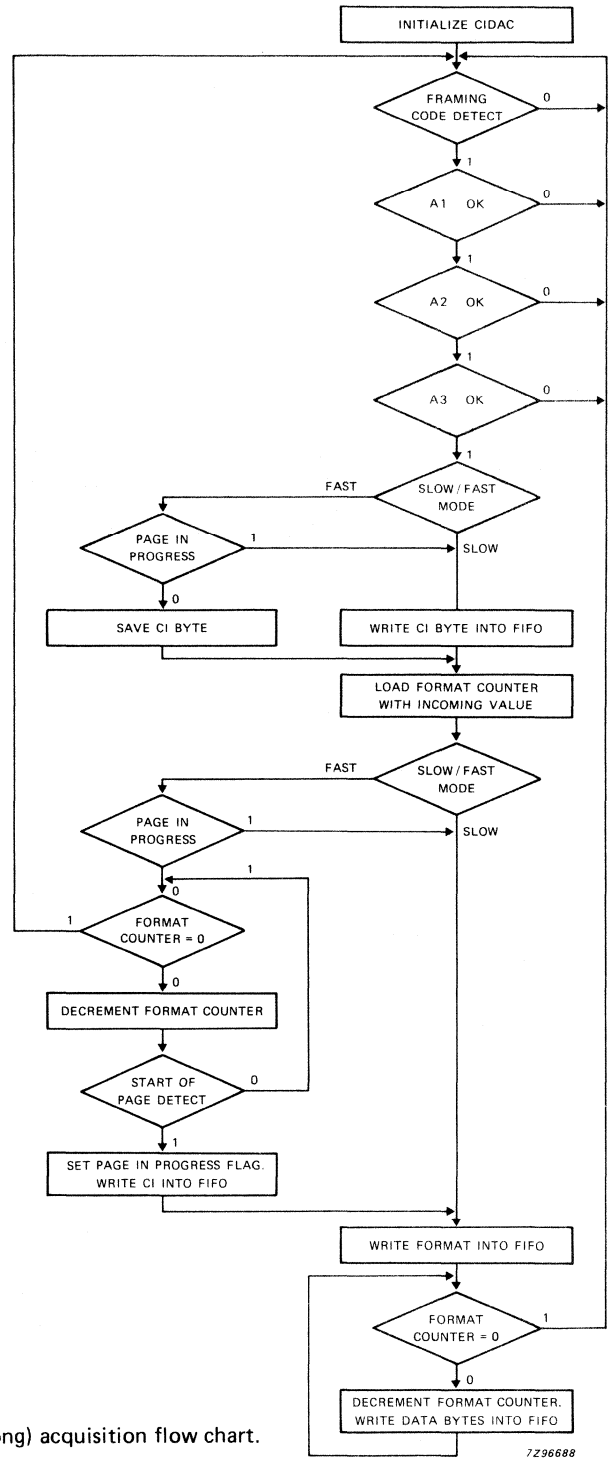


Fig. 4 DIDON (long) acquisition flow chart.

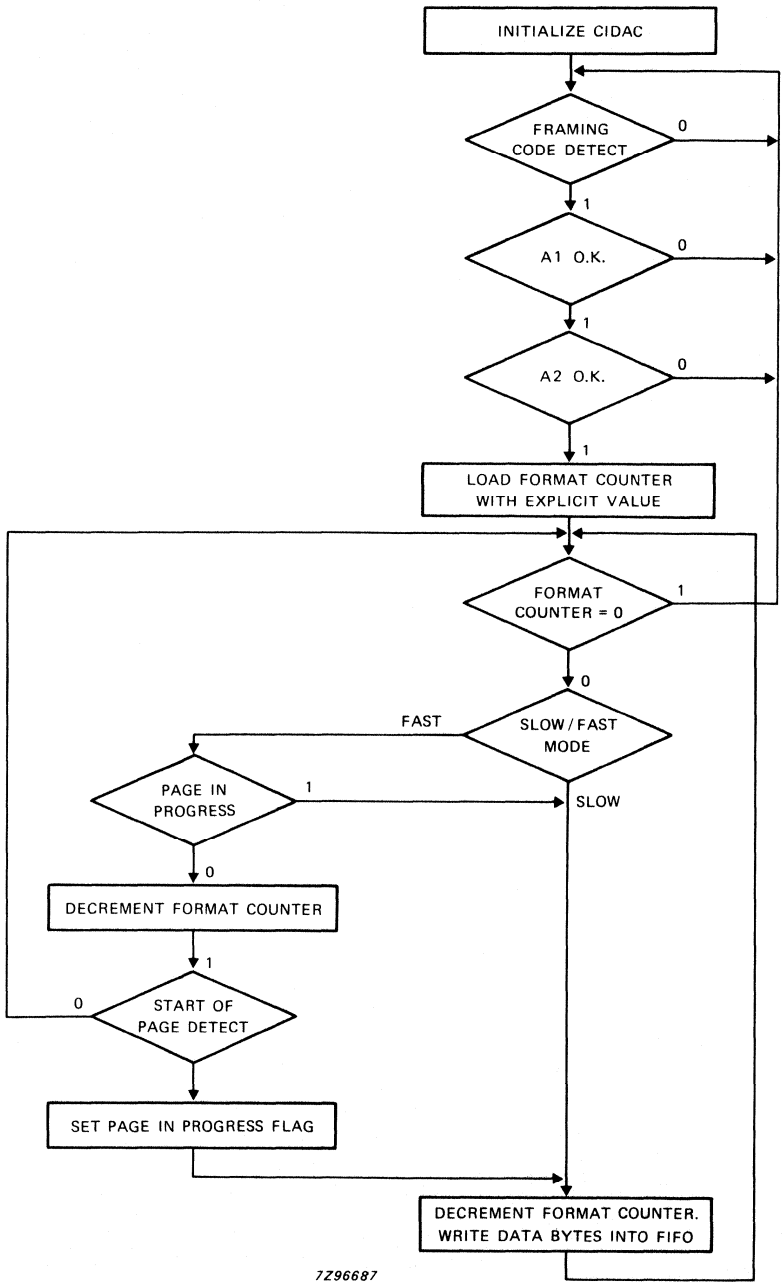


Fig. 5 DIDON (medium) acquisition flow chart.

DEVELOPMENT DATA

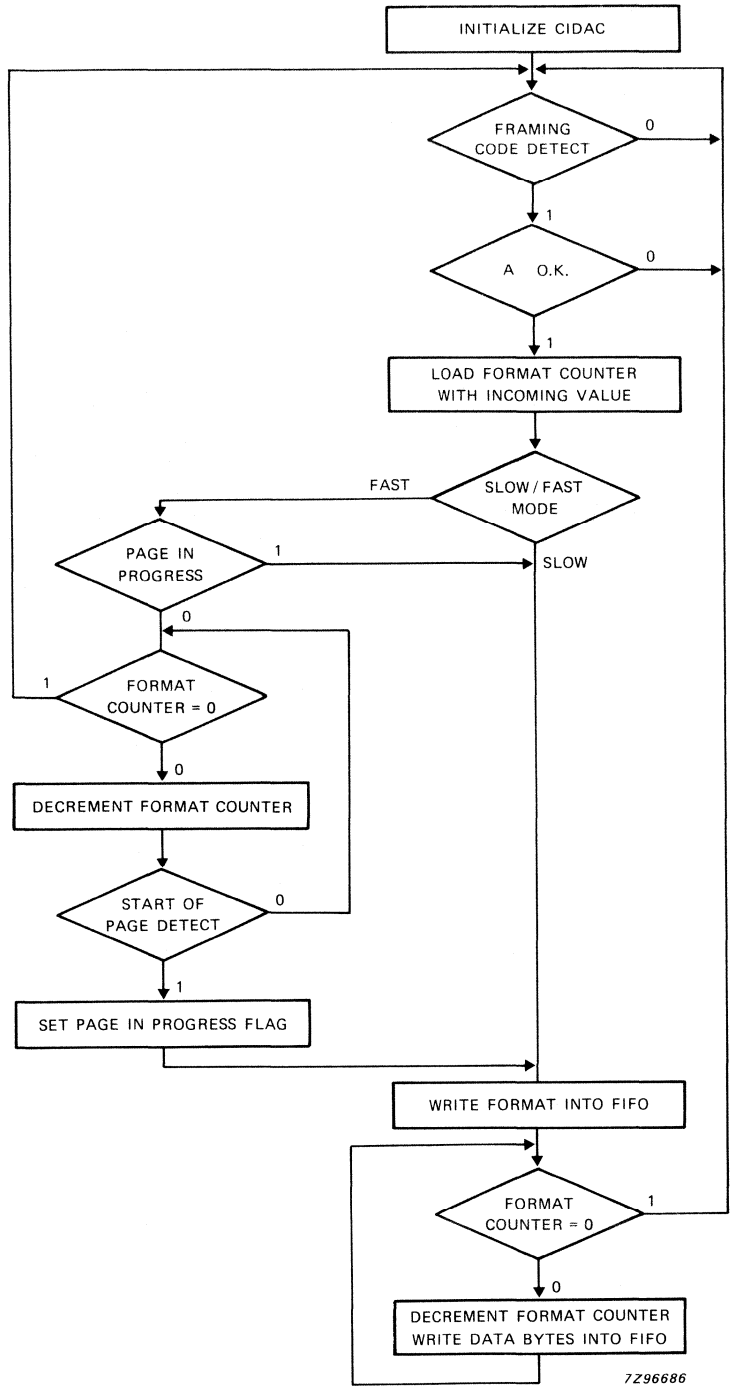


Fig. 6 DIDON (short) acquisition flow chart.

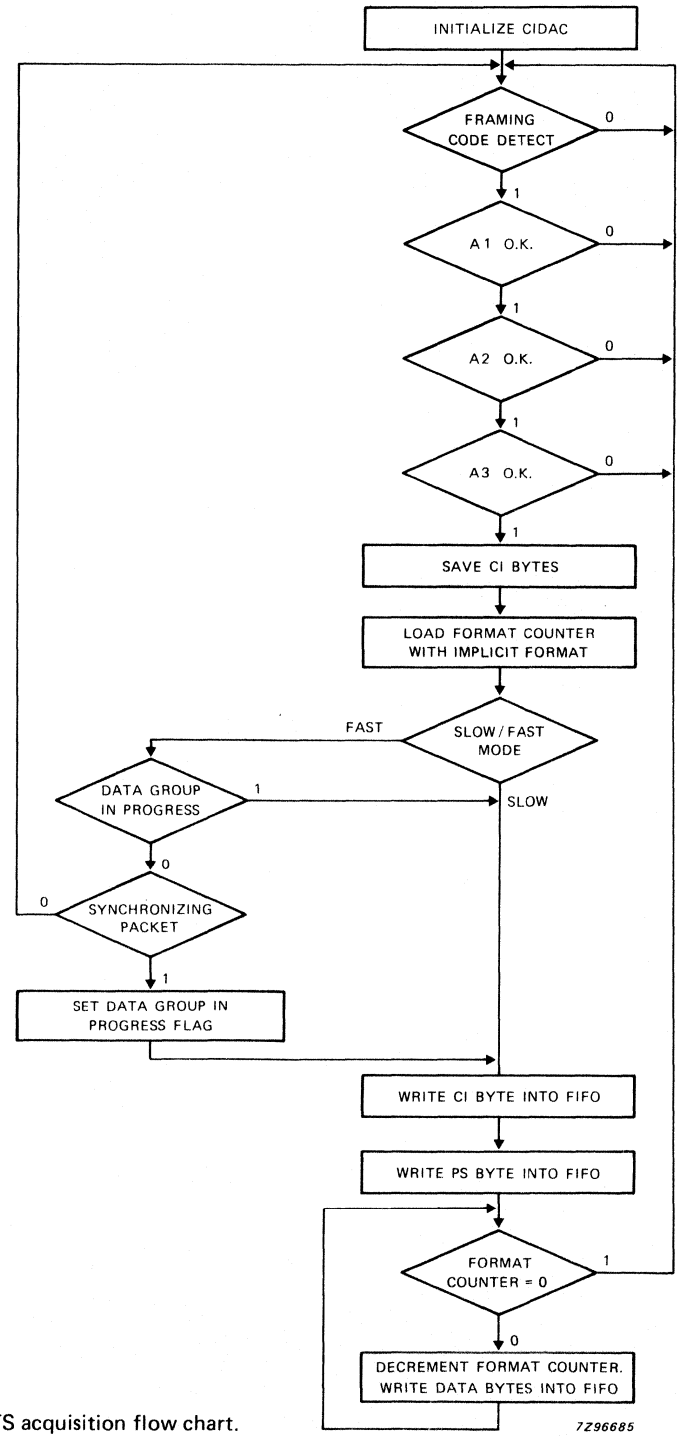


Fig. 7 NABTS acquisition flow chart.

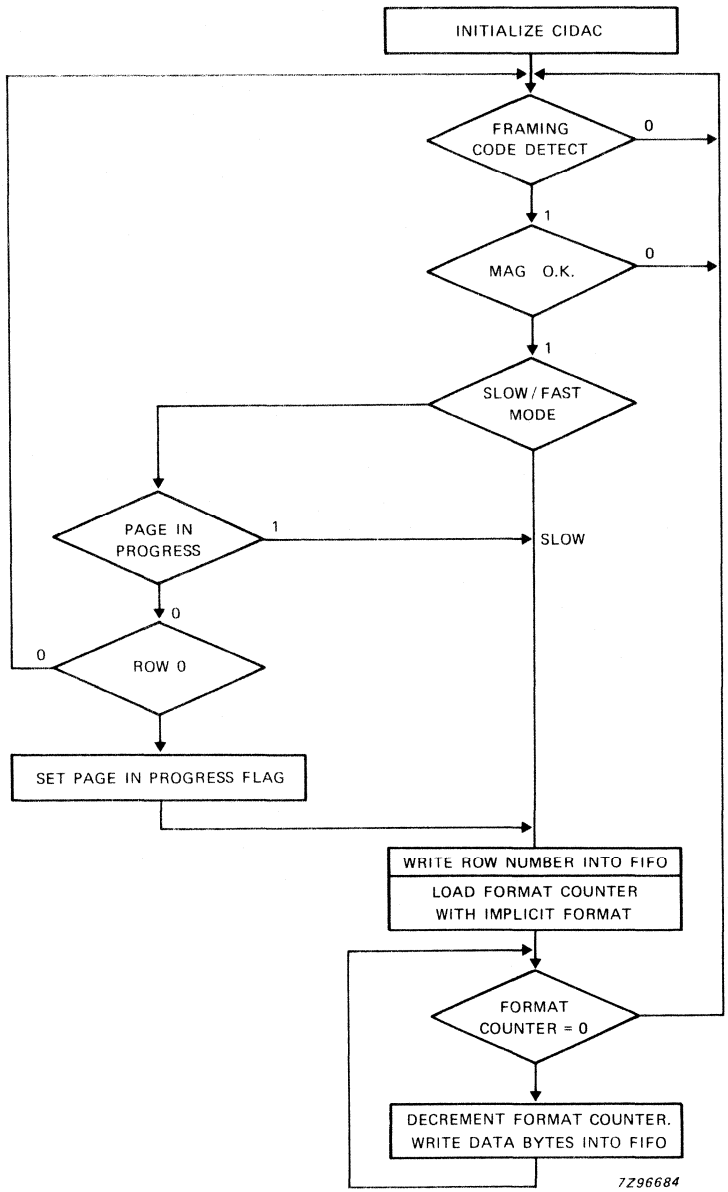


Fig. 8 U.K. teletext acquisition flow chart.

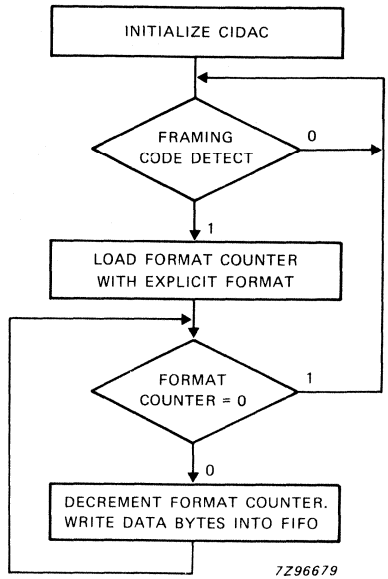


Fig. 9 Without prefix acquisition chart.

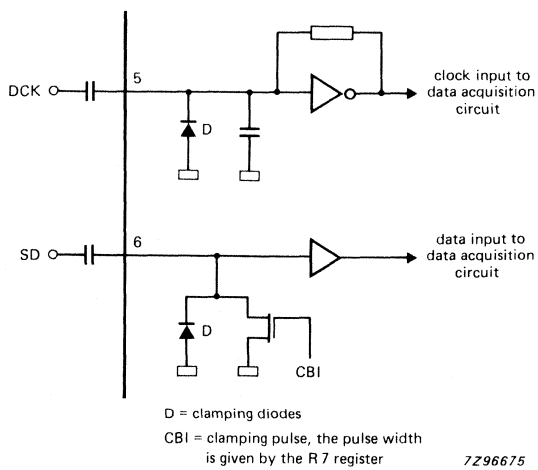


Fig. 10 SD and DCK input circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,3	6,5	V
Input voltage range		V_I	−0,3	V_{DD}+0,3	V
Total power dissipation		P_{tot}	−	400	mW
Operating ambient temperature range		T_{amb}	0	70	°C
Storage temperature range		T_{stg}	−20	+125	°C

D.C. CHARACTERISTICS (except SD and DCK)

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	4,5	5,0	5,5	V
Input voltage HIGH		V_{IH}	2	−	V_{DD}	V
Input voltage LOW		V_{IL}	−	−	0,8	V
Input leakage current		I_I	−	−	1,0	μA
Output voltage HIGH	I_{load} = 1 mA	V_{OH}	V_{DD}−0,4	−	−	V
Output voltage LOW	I_{load} = 4 mA, at pins 9 to 16 and 22 to 29	V_{OL}	−	−	0,4	V
	i_{load} = 1 mA all other outputs	V_{OL}	−	−	0,4	V
Power dissipation		P	−	5	−	mW
Input capacitance		C_I	−	−	7,5	pF

DEVELOPMENT DATA

SD and DCK D.C. CHARACTERISTICS (see Fig. 10)

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
DCK						
Input voltage range (peak-to-peak value)		$V_{I(p-p)}$	2,0	–	–	V
Input current	V_I = 0 to V_{DD}	I_I	5	–	200	μA
Input capacitance		C_I	–	–	30	pF
External coupling capacitor		C_{ext}	10	–	–	nF
SD						
D.C. input voltage range HIGH	note 1	V_{IH}	2,0	–	–	V
D.C. input voltage range LOW	note 2	V_{IL}	–	–	0,8	V
A.C. input voltage (peak-to-peak value)		$V_{I(p-p)}$	2,0	–	–	V
Input leakage current	V_I = 0 to V_{DD}	I_I	–	–	10	μA
Input capacitance		C_I	–	–	30	pF
External coupling capacitor		C_{ext}	10	–	–	nF

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 5 V ±10%; Reference levels for all inputs and outputs, V_{IH} = 2 V; V_{IL} = 0,8 V; V_{OH} = 2,4 V; V_{OL} = 0,4 V; C_L = 50 pF on DB7 to DB0; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Microcontroller interface	Figs 11 and 12					
Cycle time		t_{CY}	400	–	–	ns
Address pulse width		t_{LHLL}	50	–	–	ns
$\overline{RD}$ HIGH or $\overline{WR}$ to ALE HIGH	Fig. 11	t_{AHRD}	0	–	–	ns
DS LOW to AS HIGH	Fig. 12	t_{AHRD}	0	–	–	ns
ALE LOW to $\overline{RD}$ LOW or $\overline{WR}$ LOW	Fig. 11	t_{ALRD}	30	–	–	ns
AS LOW to DS HIGH	Fig. 12	t_{ALRD}	30	–	–	ns
Write pulse width		t_{WL}	120	–	–	ns
Address and chip select set-up time		t_{ASL}	10	–	–	ns
Address and chip select hold time		t_{AHL}	20	–	–	ns
Read to data out period		t_{RD}	–	–	130	ns
Data hold after $\overline{RD}$		t_{DR}	10	–	100	ns
R/$\overline{W}$ to DS set-up time	Fig. 12	t_{RWS}	40	–	–	ns
R/$\overline{W}$ to DS hold time	Fig. 12	t_{RWH}	10	–	–	ns
Data set-up time	write cycle	t_{DW}	50	–	–	ns
Data hold time	write cycle	t_{WD}	10	–	–	ns
Read pulse width	note 3	t_{RL}	150 or DCK + 50	–	–	ns

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Memory interface	Fig. 13					
$\overline{WE}$ LOW to DCK falling edge		t_{WEL}	10	–	80	ns
$\overline{WE}$ HIGH to DCK falling edge		t_{WEH}	10	–	80	ns
$\overline{MS}$ LOW to DCK rising edge		t_{MSL}	10	–	80	ns
$\overline{MS}$ HIGH to DCK rising edge		t_{MSH}	10	–	85	ns
Address output from DCK rising edge		t_{AV}	10	–	120	ns
Data output from $\overline{WE}$ falling edge		t_{DWL}	0	–	10	ns
Data hold from $\overline{WE}$ rising edge		t_{DWH}	0	–	–	ns
Address set-up time to data	note 4	t_{AD}	–	–	3 x DCK – 110	ns
$\overline{WE}$ pulse width	note 5	t_{WEW}	3 x DCK	–	–	ns
$\overline{MS}$ pulse width	note 6	t_{MSW}	2 x DCK	–	–	ns
Demodulator interface (see SD and DCK D.C. CHARACTERISTICS)	Fig. 14					
DCK LOW	conversion rate < 7,5 MHz	t_{DCKL}	55	–	–	ns
DCK HIGH	conversion rate < 7,5 MHz	t_{DCKH}	55	–	–	ns
Serial data set-up time		t_{SSD}	0	–	–	ns
Serial data hold time		t_{HSD}	30	–	–	ns
Validation signal set-up time		t_{SVALI}	50	–	–	ns
Validation signal hold time		t_{HVALI}	50	–	–	ns
Other I/O signals	Fig. 15					
User definable width as a multiple of DCK period		t_{WCBB}	0	–	63	DCK
Validation signal width	note 7	t_{WVAL}	X	12	X	DCK
User definable delay as a multiple of DCK period		t_{DVAL}	0	–	127	DCK

Notes to the characteristics

1. Unless R7 = 00 the value given is unacceptable.
2. When CBI signal is maintained at 0 V (R7 = 00) and if SD input signal is correctly referenced to ground, no coupling capacitor is required.
3. DCK + 50 is the DCK period plus 50 ns.
4. 3 x DCK − 110 is 3 x DCK period − 110 ns.
5. 3 x DCK is 3 x DCK period.
6. 2 x DCK is 2 x DCK period.
7. X = irrelevant.

DEVELOPMENT DATA

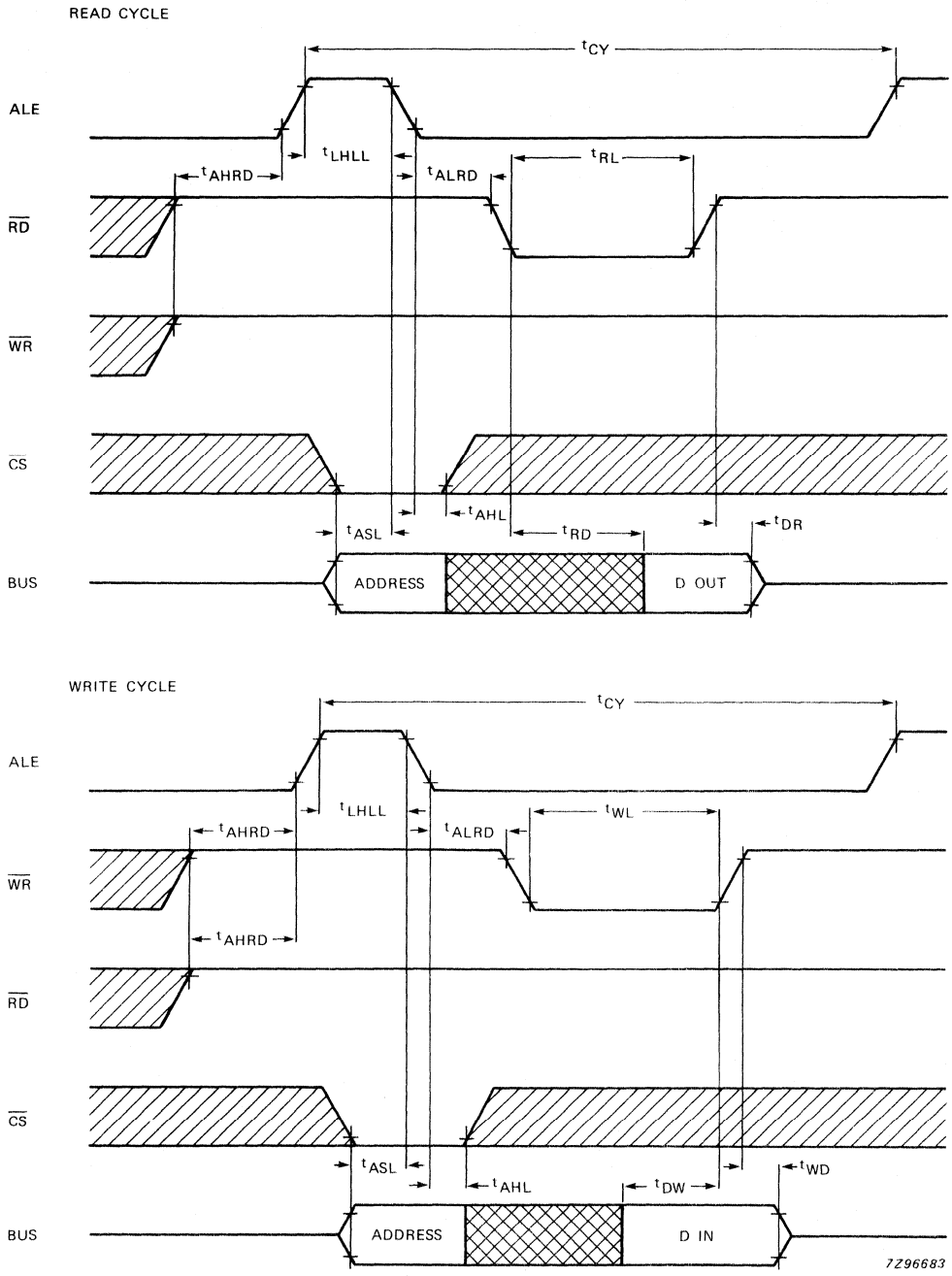


Fig. 11 Timing diagram for microcontroller interface (Intel).

DEVELOPMENT DATA

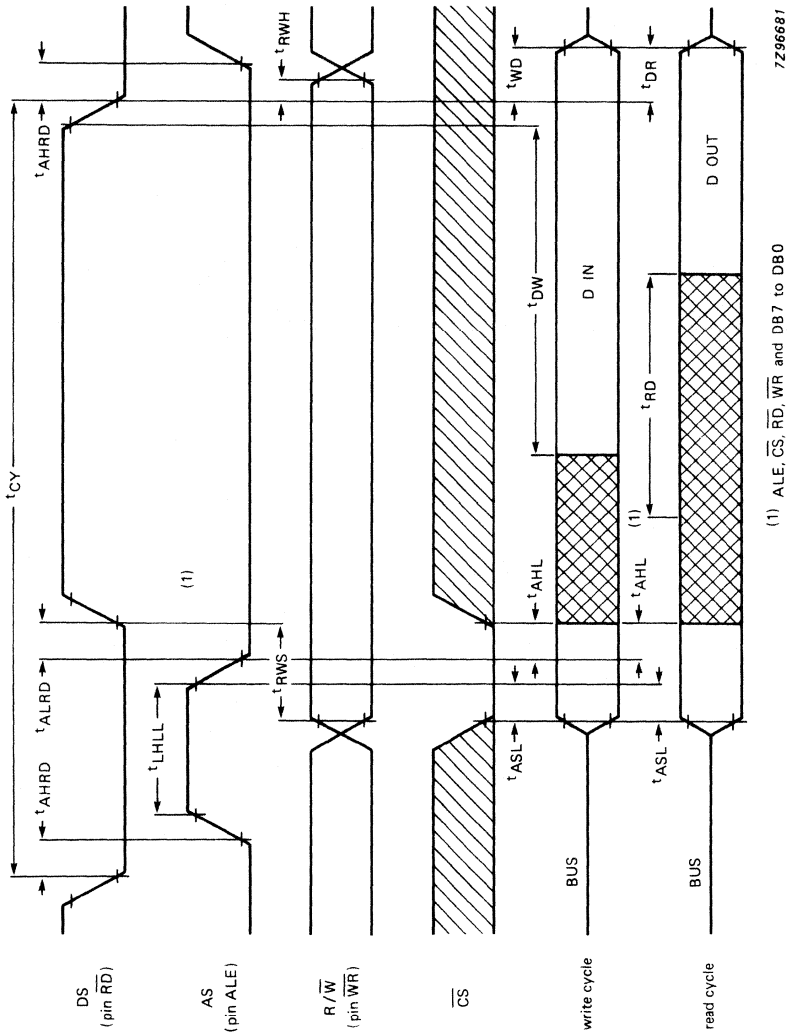


Fig. 12 Timing diagram for microcontroller interface (Motorola).

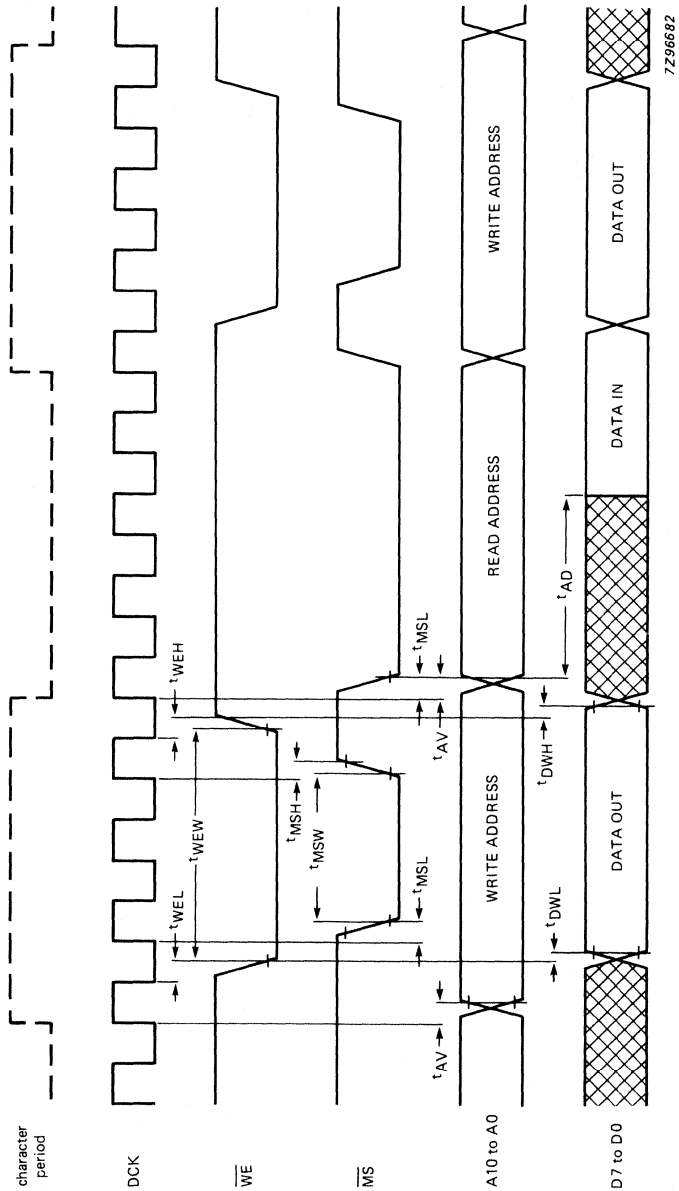


Fig. 13 Timing diagram for memory interface.

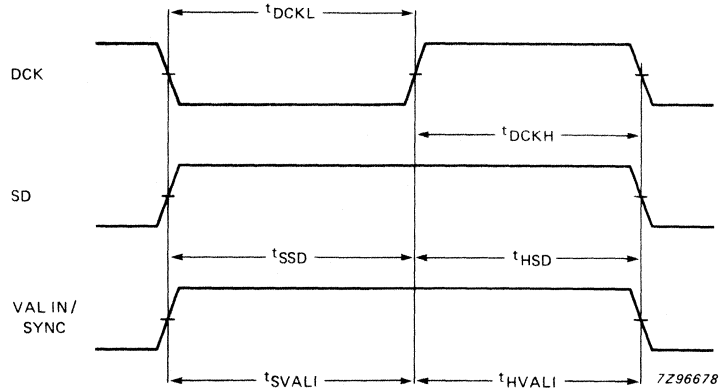


Fig. 14 Timing diagram for demodulator interface.

DEVELOPMENT DATA

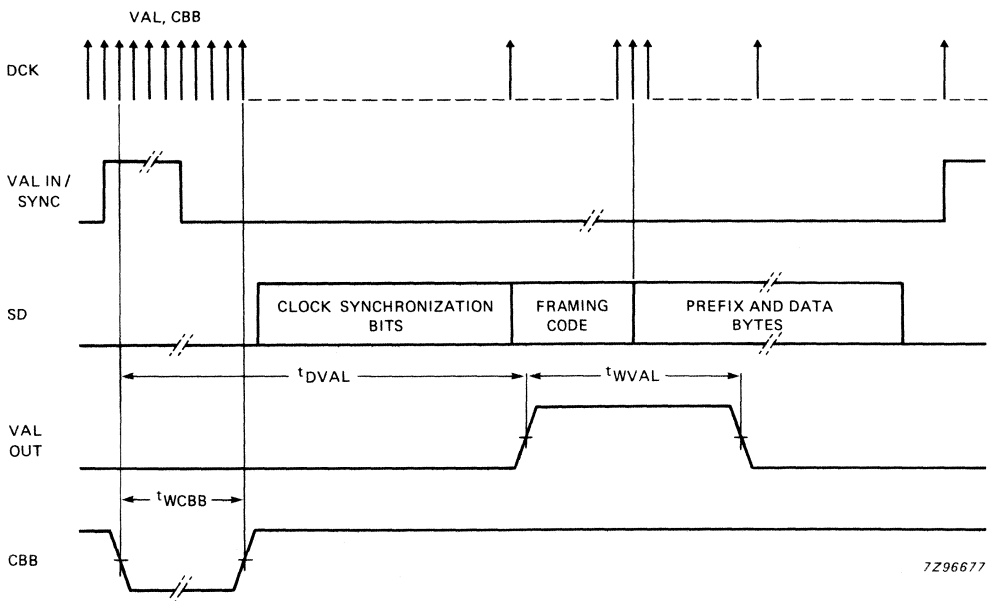


Fig. 15 Timing diagram for all other I/O signals.

SINGLE-CHIP COLOUR CRT CONTROLLER (EUROM)

GENERAL DESCRIPTION

The SAA5350 EUROM is a single-chip VLSI NMOS crt controller capable of handling all display functions required by the CEPT videotex terminal, model A4. Only minimal hardware is required to produce a videotex terminal using EUROM – the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- On-chip colour map RAM (4096 locations) and three on-chip digital-to-analogue converters allow 32 colours on-screen
- On-chip digital-to-analogue converters are non-linear to compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. EUROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 6 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129).

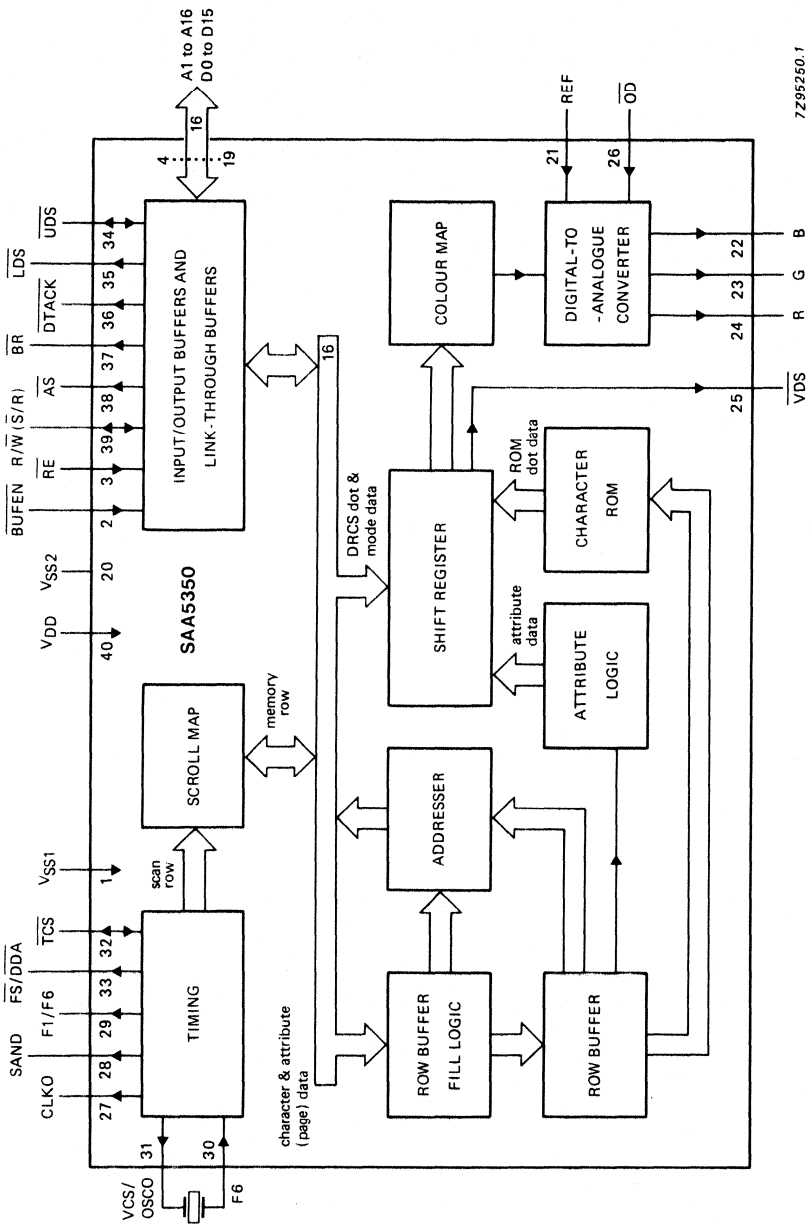


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

1	V_{SS1}	Ground 0 V.
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	V_{SS2}	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3560, TDA3505).
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/F6	1 MHz or 6 MHz output.
30	F6	6 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	R/$\overline{W}$ ($\overline{S}$/R)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

PINNING (continued)

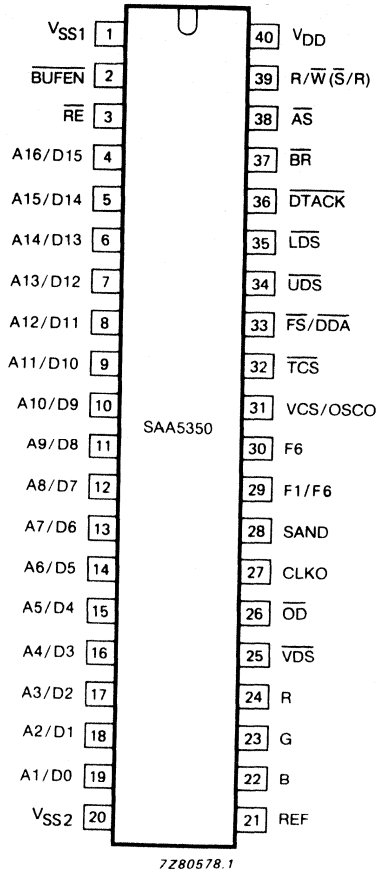


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0,3 to + 7,5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0,3 to + 7,5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0,3 to + 10,0 V
Maximum input voltage (REF)	V_{REF}	−0,3 to + 3,0 V
Maximum output voltage	V_{Omax}	−0,3 to + 7,5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4,75	5,0	5,25	V
Supply current (pin 40)	I_{DD}	–	–	350	mA
INPUTS					
F6 (note 1)					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	7,0	V
Input peaks relative to 50% duty factor	$\pm V_P$	0,2	–	3,5	V
Input leakage current at V_I = 0 to 10 V; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7,1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
Gain of circuit	G	–	–	tbf	V/V
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2,7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −10 μA	V_{OH}	4,2	–	V_{DD}	V
Output voltage intermediate level at I_O = −10 to + 10 μA	V_{OI}	1,3	2,0	2,7	V
Output voltage low level at I_O = 0,2 mA	V_{OL}	0	–	0,2	V
Load capacitance	C_L	–	–	130	pF
F1/F6, CLKO, $\overline{\text{DDA}}$/$\overline{\text{FS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
$\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF
$\overline{\text{DTACK}}$, $\overline{\text{BR}}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2,7 V	V_{OH}	2,4	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH at $I_{OH} = -250\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 2$ mA	V_{OL}	0	–	0,4	V
Output voltage LOW at $I_{OL} = 1$ mA	V_{OL}	0	–	0,2	V
Output leakage current (OFF state) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_{OFF}	−10	–	+ 10	μA
INPUT/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current (output OFF) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Load capacitance	C_L	–	–	50	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200$ to $100\ \mu A$	V_{OH}	2,4	–	6,0	V
Output voltage LOW at $V_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
A1/D0 to A16/D15, $\overline{UDS}$, R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5,9	–	6,1	MHz
CLKO, F1/F6, R, G, B, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$, $\overline{OD}$ (notes 4, 5 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	25	–	–	ns
CLKO LOW time	t_{CLKL}	15	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ change	t_{VCH}	10	–	–	ns
R, G, B, $\overline{VDS}$ valid to CLKO rise	t_{VOC}	10	–	–	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ valid	t_{COV}	–	–	60	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall	t_{FOD}	0	–	30	ns
Skew between outputs R, G, B, $\overline{VDS}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{VDS}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	t_{AOD}	0	–	60	ns
CLKO HIGH to $\overline{FS}$/$\overline{DDA}$ change	t_{COD}	10	–	55	ns
$\overline{FS}$/$\overline{DDA}$ valid to CLKO rise	t_{DOC}	5	–	–	ns
F1 HIGH time (note 6)	t_{F1H}	400	500	580	ns
F1 LOW time (note 6)	t_{F1L}	400	500	580	ns
F6 HIGH time	t_{F6H}	40	83	120	ns
F6 LOW time	t_{F6L}	40	83	120	ns
$\overline{OD}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{OD}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 7, 8, 9 and Fig. 7)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
Cycle time	t_{cyc}	480	500	520	ns
$\overline{UDS}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{AS}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{AS}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{UDS}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time	t_{LDS}	200	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	320	–	–	ns
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	305	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	15	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	270	ns
Link-through buffers					
(notes 7, 8 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from EUROM					
(Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	40	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	250	–	350	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to EUROM (Fig. 10)					
Write cycle time (note 10)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/F6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/F6) rise	t_{UF6}	20	–	–	ns
F6 (component of F1/F6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. Pin 30 must be biased externally as it is internally a.c. coupled.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. CLKO, R, G, B, F1/F6, $\overline{VDS}$: C_L = 25 pF
   $\overline{FS}$/$\overline{DDA}$: C_L = 50 pF
5. CLKO, F1/F6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0,8 to 2,0 V
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2,7 V
6. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
7. C_L = 150 pF.
8. Reference levels = 0,8 to 2,0 V.
9. F6 input at 6 MHz.
10. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will then depend on the internal synchronization time.

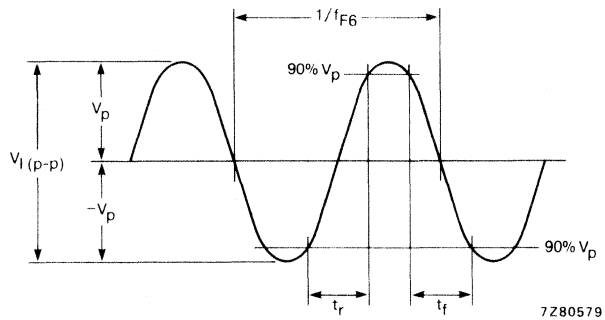
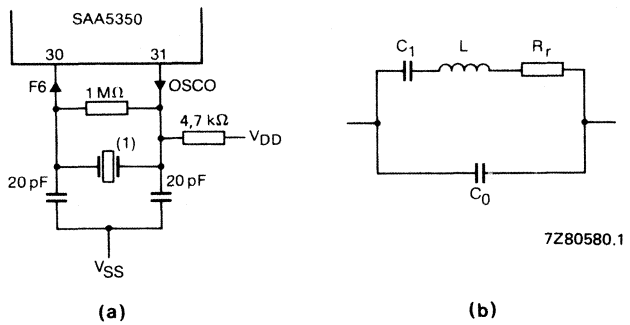


Fig. 3 F6 input waveform.



(1) Catalogue number of crystal: 4322 143 04101

Fig. 4(a) Oscillator circuit for SAA5350 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

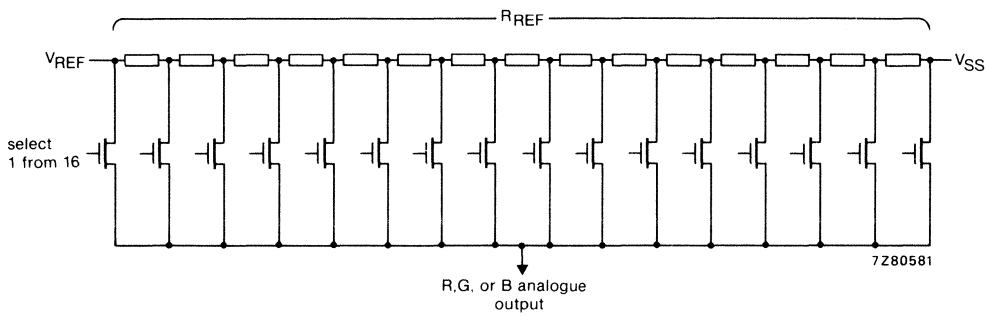


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

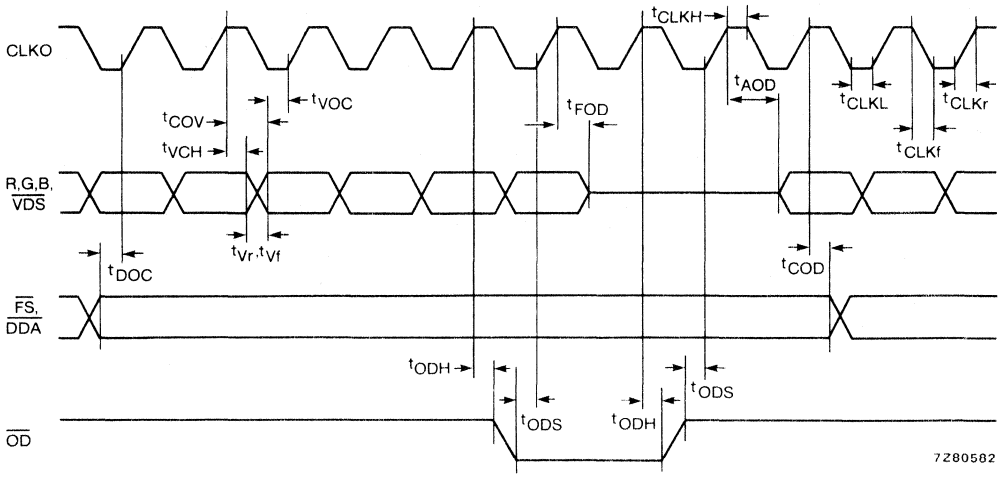


Fig. 6 Video timing.

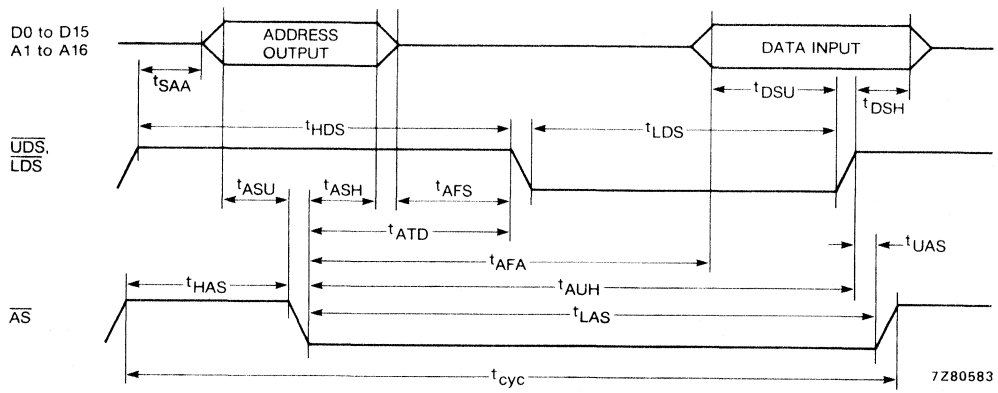


Fig. 7 Memory access timing.

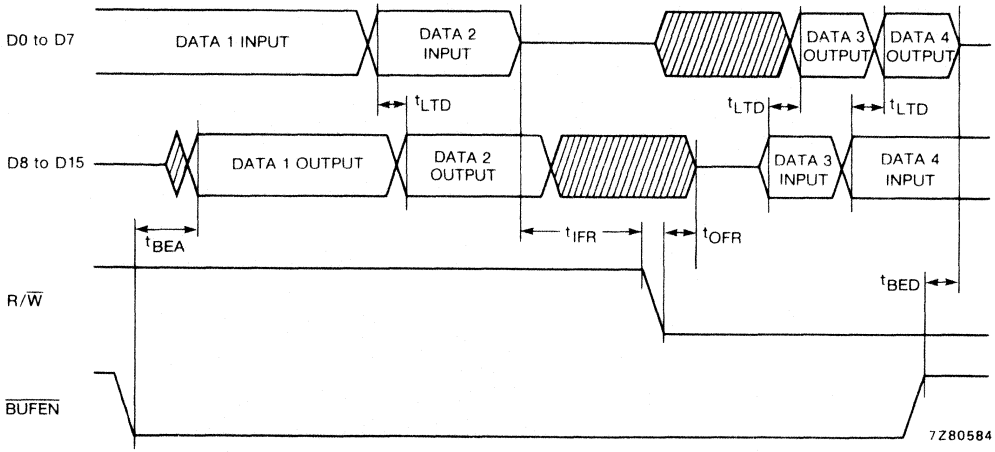


Fig. 8 Timing of link-through buffers.

DEVELOPMENT DATA

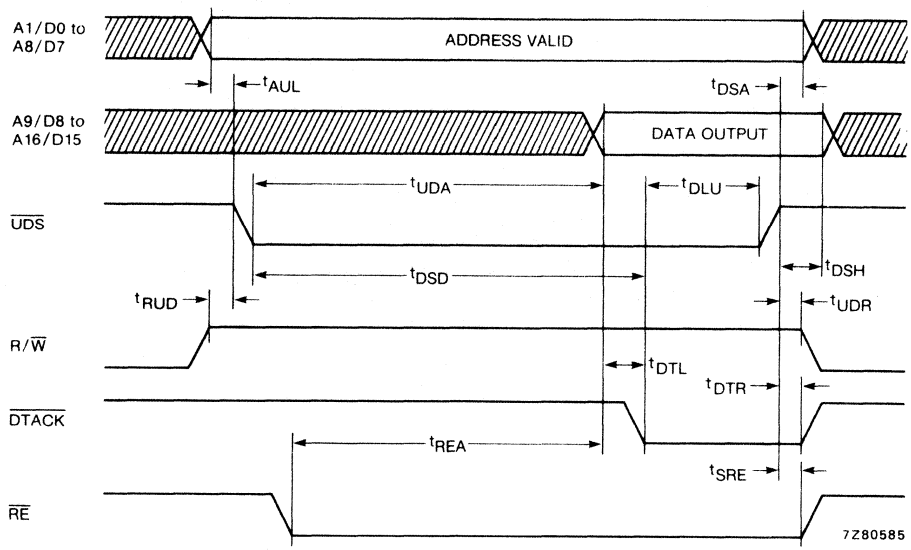


Fig. 9 Timing of microprocessor read from EUROM.

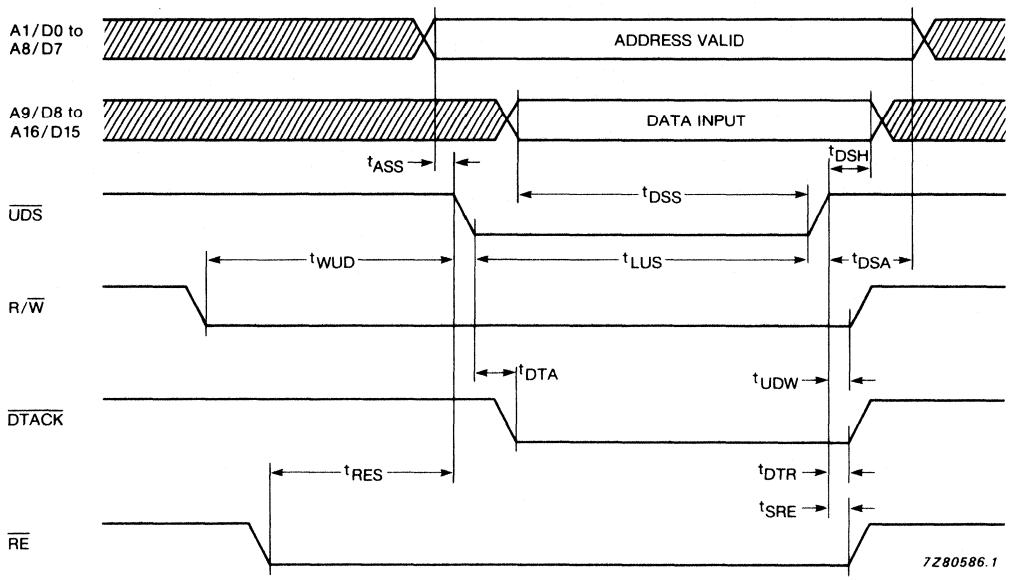


Fig. 10 Timing of microprocessor write to EUROM.

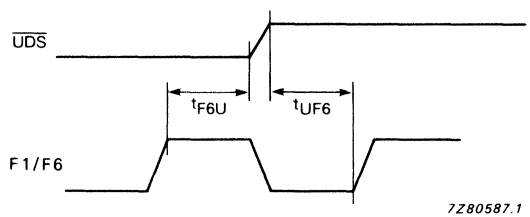


Fig. 11 Timing of F1/F6 to memory access cycle.

DEVELOPMENT DATA

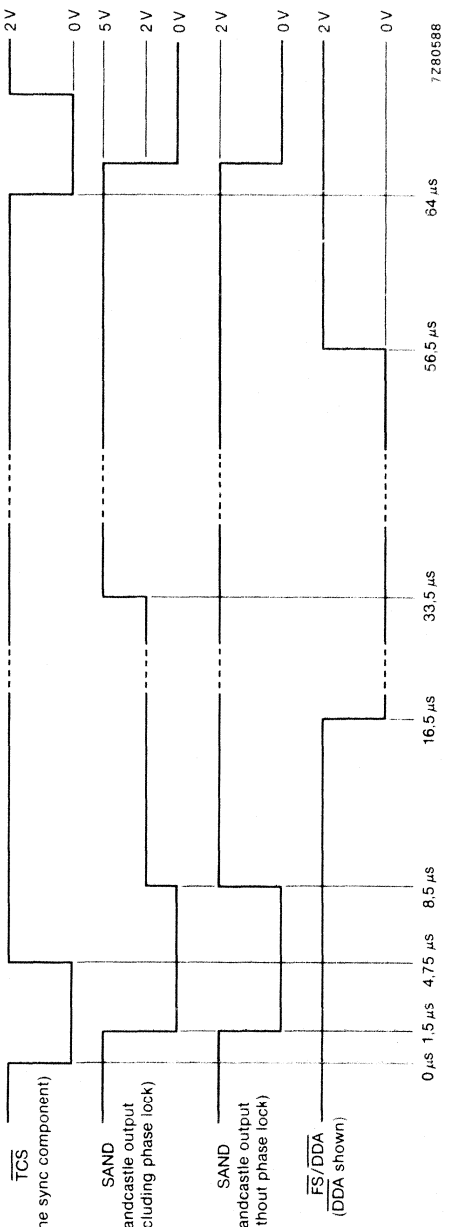


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume f_{F6} = 6 MHz.

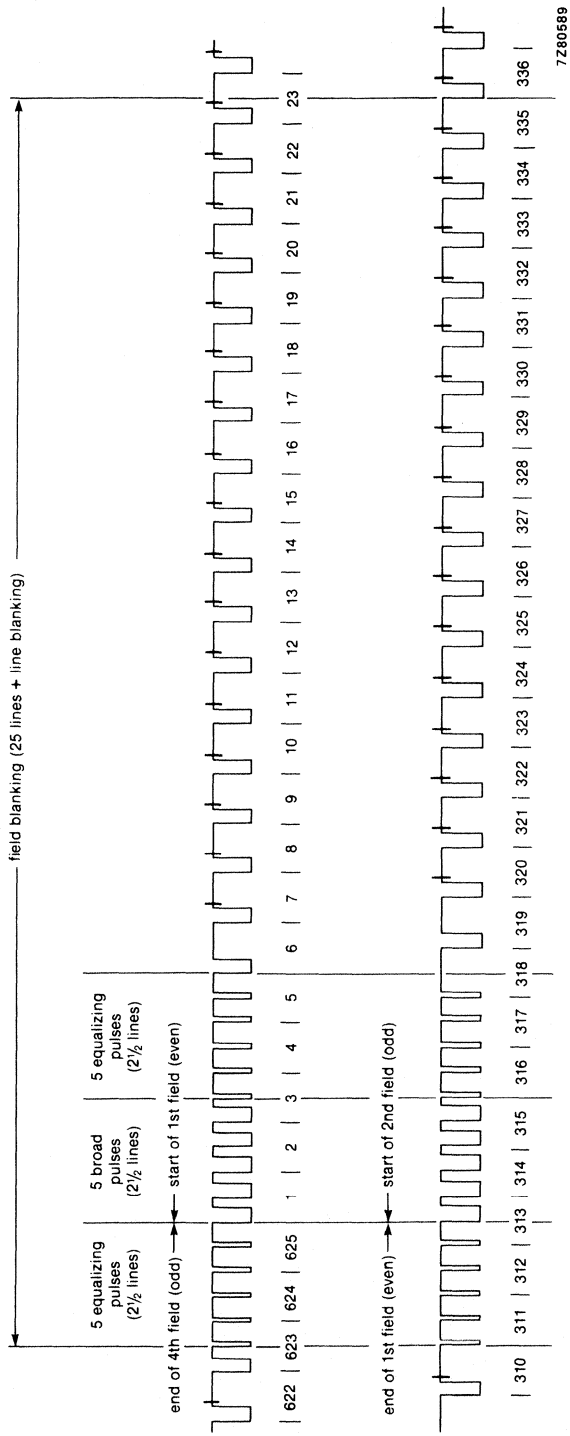


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4,75 μs; equalizing pulse widths = 2,25 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

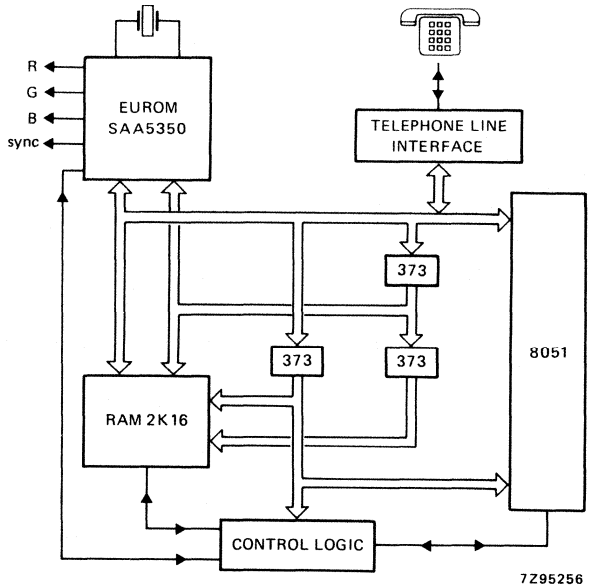


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows — each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

The timing chain operates from an external 6 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 24/25 rows per page and 10 video lines per row. EUROM will also operate with 20/21 rows per page and 12 video lines per row. The two extra lines per row are added symmetrically and contain background colour only for ROM-based alpha-numeric characters. DRCS characters, block and smooth mosaics and line drawing characters occupy all 12 lines.

The display is generated to the normal 625-line/50 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at 1 MHz or 6 MHz (pin 29) is available for driving other videotex devices, and a 12 MHz clock (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

APPLICATION INFORMATION (continued)

Character generation

EUROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The contents of the fixed character tables (Tables 0 to 3) are shown in Figs 15 and 16.

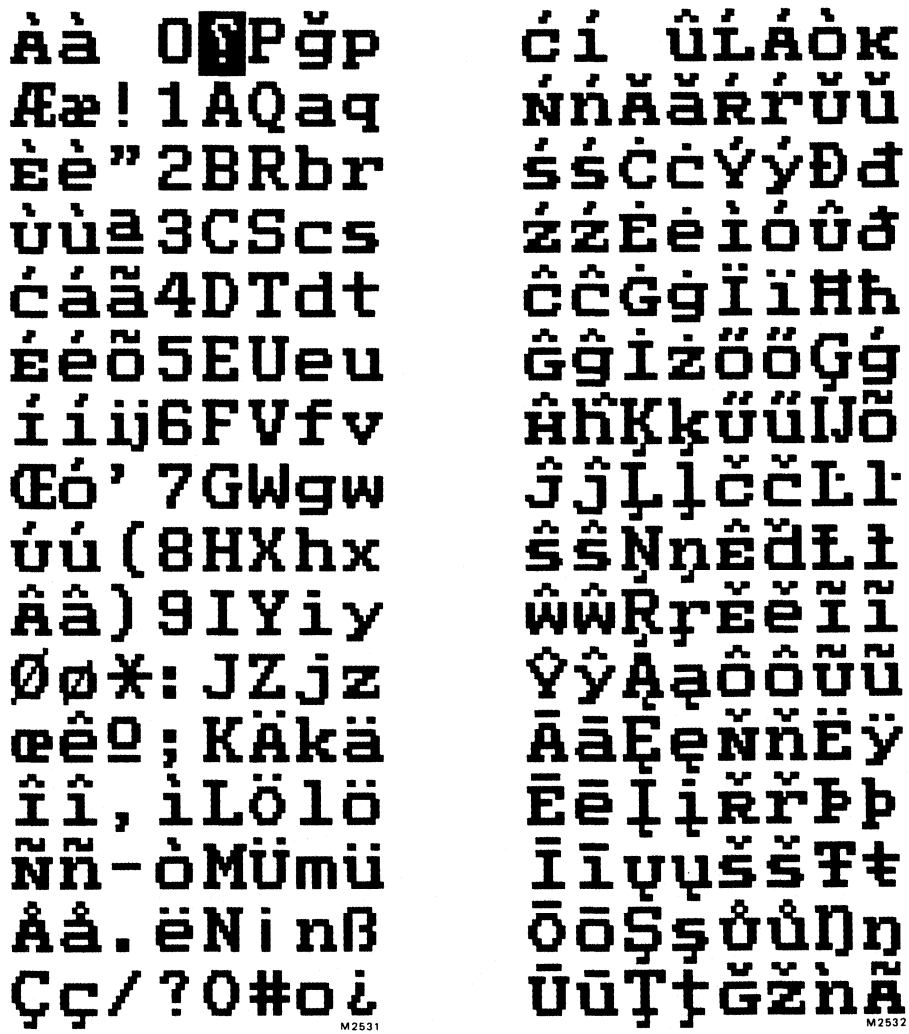
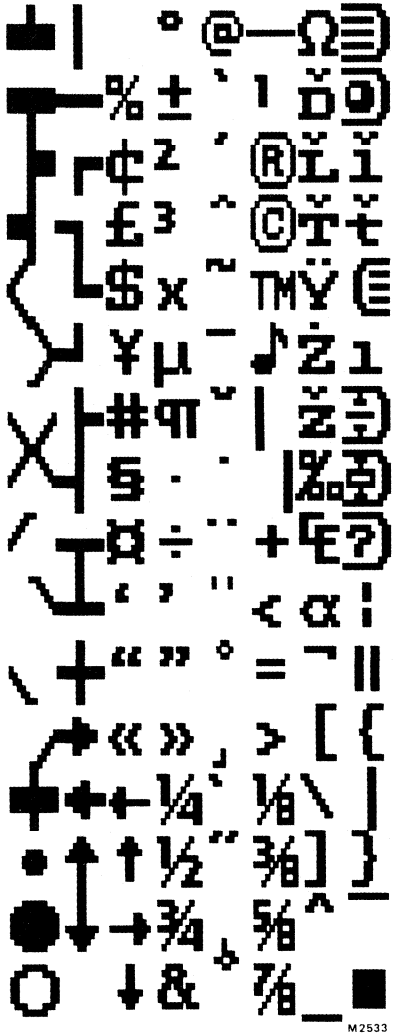
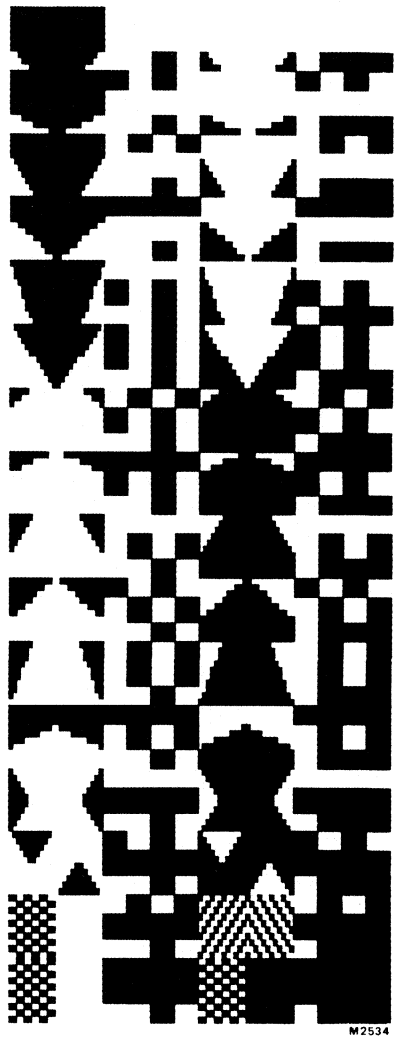


Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.



(a)



(b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

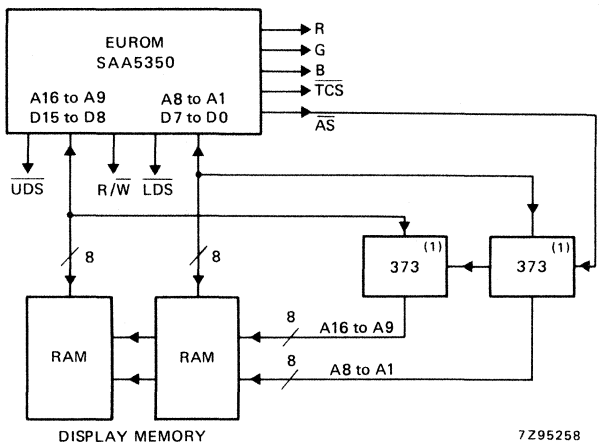
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- EUROM fetches data from the display memory
- The microprocessor reads from, or writes to, EUROM's internal register map
- The microprocessor accesses the display memory

EUROM access to display memory (Figs 17 and 18)

EUROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 500 ns. The address strobe ($\overline{AS}$) signal from EUROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although EUROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

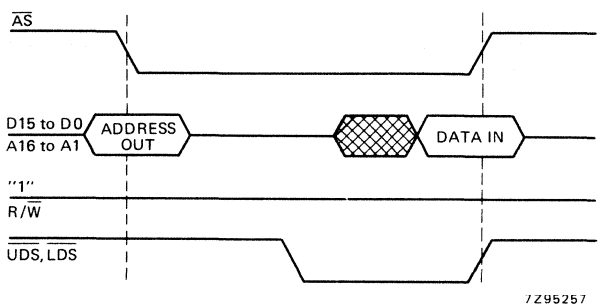


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

EUROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain — there are no odd-numbered word addresses.

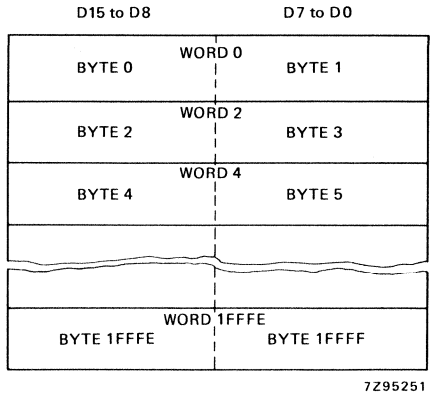


Fig. 19 Display memory word/byte organization.

Warning time

As EUROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by EUROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and EUROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that EUROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of EUROM's bus activity is programmable to be between 0 and 23 μs.

Microprocessor access to register map

EUROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

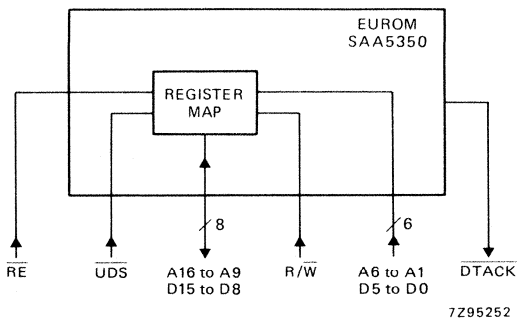


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to EUROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

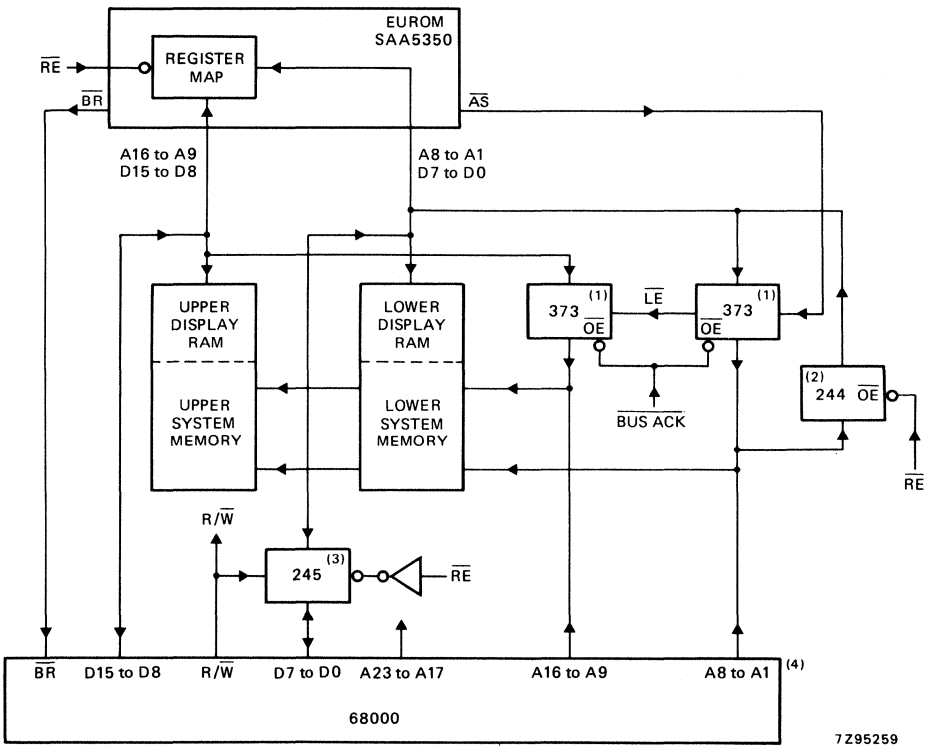
The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by EUROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of EUROM's scroll map contents at a location in its main memory.

8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, EUROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by EUROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

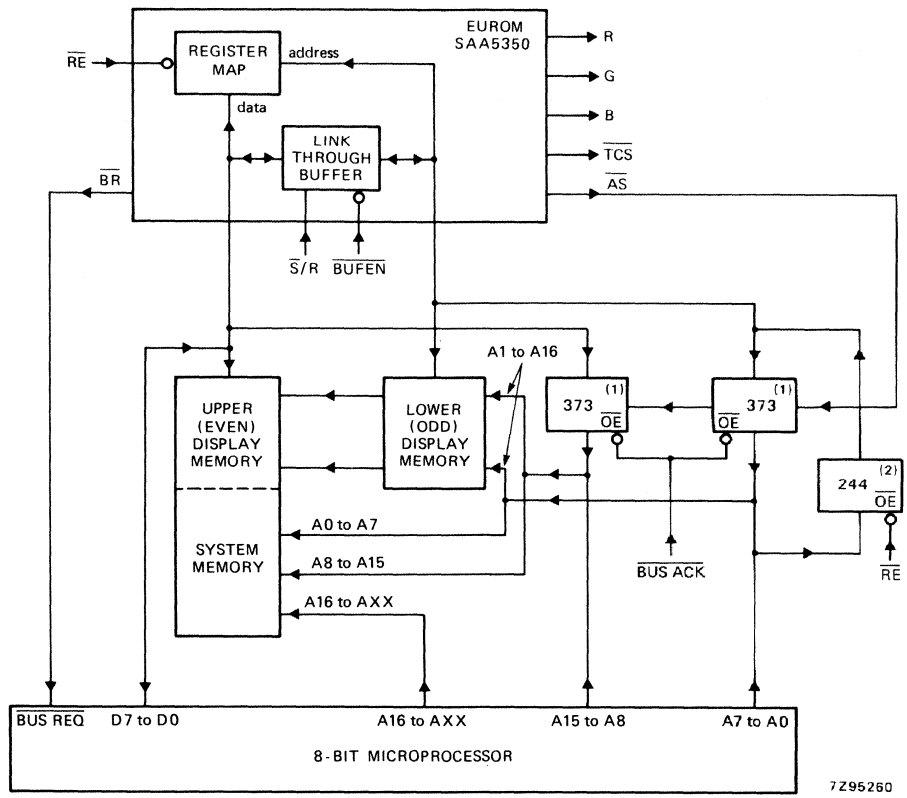
The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.



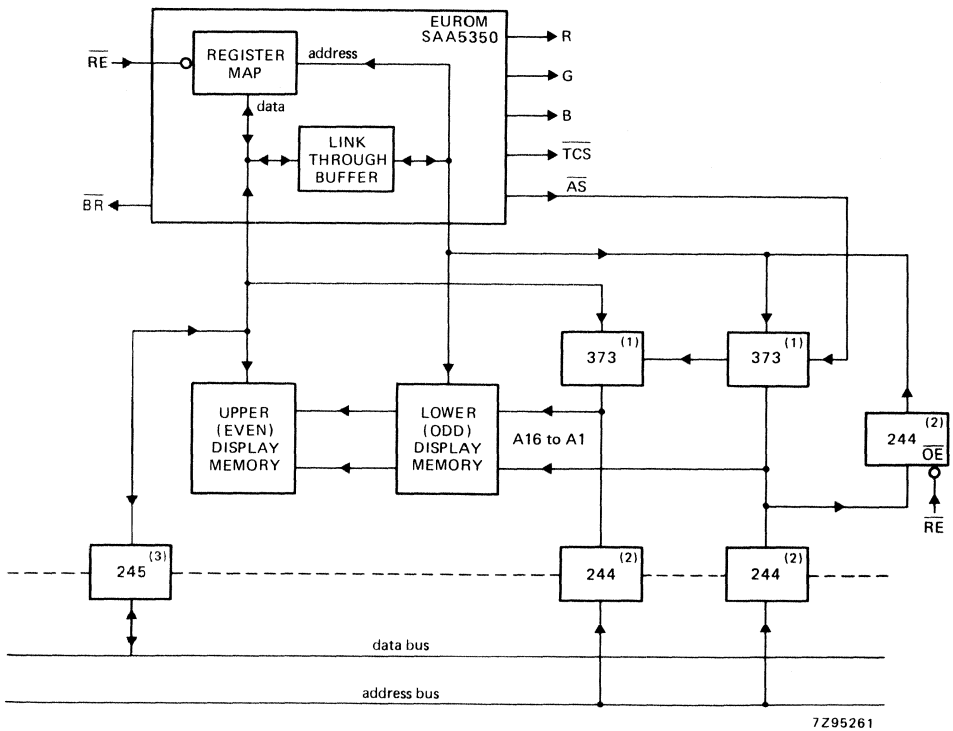
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect EUROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses EUROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 75LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) EUROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

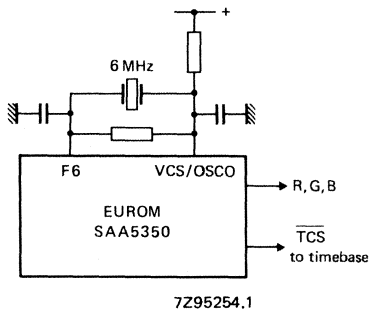


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode EUROM synchronizes directly to another device, such as to the $\overline{TCS}$ signal from the SAA5240 European computer-controlled teletext circuit (CCT) or from another EUROM as shown in Fig. 25. EUROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using EUROM's internal field sync separator.

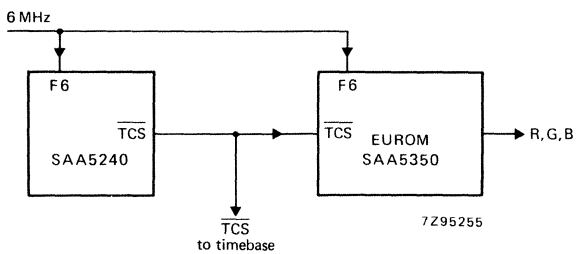


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. A phase-locked VCO in the SAA5230 teletext video processor provides sync to the timebases. When EUROM is active, its horizontal counter forms part of the phase control loop – a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to EUROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from EUROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possiblities.

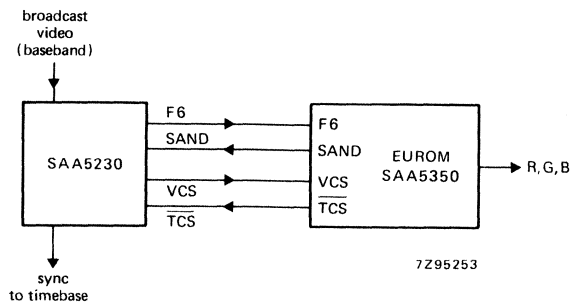


Fig. 26 Phase-locked slave (indirect sync) mode.

SINGLE-CHIP COLOUR CRT CONTROLLER (FTFROM)

GENERAL DESCRIPTION

The SAA5355 FTFROM (Five-Two-Five-ROM) is a single-chip VLSI NMOS crt controller capable of handling the display functions required for a 525-line, level-3 videotex decoder. Only minimal hardware is required to produce a videotex terminal using FTFROM – the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- 32 on-screen colours redefinable from a palette of 4096
- Three on-chip digital-to-analogue converters which compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. FTFROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 6,041957 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing with composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129).

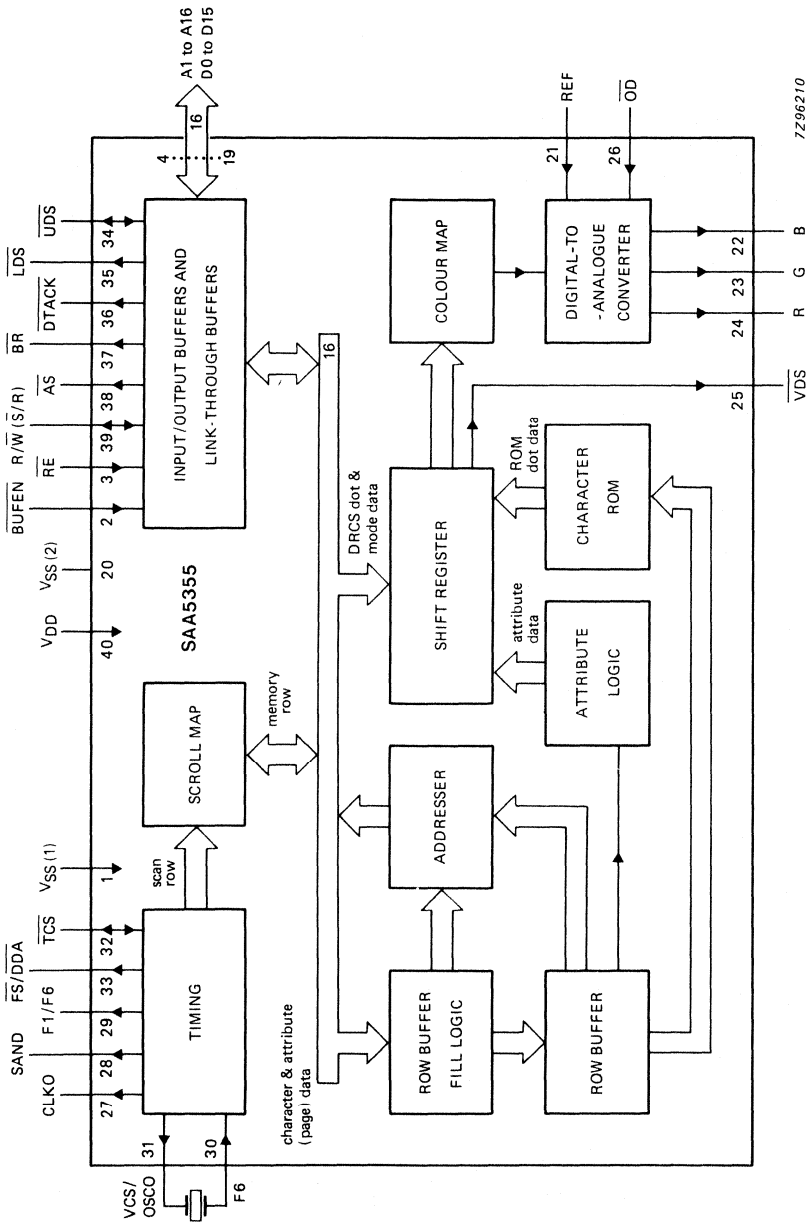


Fig. 1 Block diagram.

PINNING

1	$V_{SS(1)}$	Ground (0 V).
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	$V_{SS(2)}$	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3563, TDA3562A).
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/F6	1,00699 MHz or 6,041957 MHz output.
30	F6	6,041957 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	R/$\overline{W}$ ($\overline{S}$/R)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

DEVELOPMENT DATA

PINNING (continued)

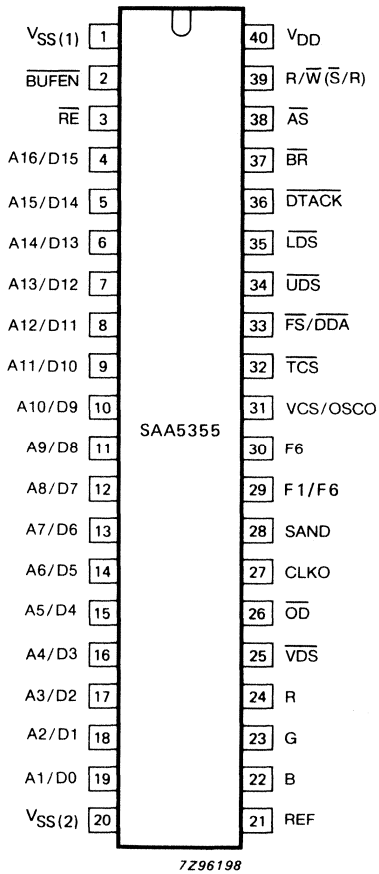


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0,3 to + 7,5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0,3 to + 7,5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0,3 to + 10,0 V
Maximum input voltage (REF)	V_{REF}	−0,3 to + 3,0 V
Maximum output voltage	V_{Omax}	−0,3 to + 7,5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4,75	5,0	5,25	V
Supply current (pin 40)	I_{DD}	–	–	350	mA
INPUTS					
F6 (note 1)					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	7,0	V
Input peaks relative to 50% duty factor	$\pm V_P$	0,2	–	3,5	V
Input leakage current at V_I = 0 to 10 V; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7,1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
Gain of circuit	G	–	–	*	V/V
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2,7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

* Value under investigation.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −10 μA	V_{OH}	4,2	–	V_{DD}	V
Output voltage intermediate level at I_O = −10 to + 10 μA	V_{OI}	1,3	2,0	2,7	V
Output voltage low level at I_O = 0,2 mA	V_{OL}	0	–	0,2	V
Load capacitance	C_L	–	–	130	pF
F1/F6, CLKO, $\overline{\text{DDA}}$/$\overline{\text{FS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
$\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF
$\overline{\text{DTACK}}$, $\overline{\text{BR}}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2,7 V	V_{OH}	2,4	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH at $I_{OH} = -250\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 2$ mA	V_{OL}	0	–	0,4	V
Output voltage LOW at $I_{OL} = 1$ mA	V_{OL}	0	–	0,2	V
Output leakage current (OFF state) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_{OFF}	−10	–	+ 10	μA
INPUT/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current (output OFF) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Load capacitance	C_L	–	–	50	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200$ to $100\ \mu A$	V_{OH}	2,4	–	6,0	V
Output voltage LOW at $V_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
A1/D0 to A16/D15, $\overline{UDS}$, R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING (note 4)					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5,9	–	6,1	MHz
CLKO, F1/F6, R, G, B, $\overline{VDS}$ $\overline{FS}/\overline{DDA}$, $\overline{OD}$ (notes 5, 6 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	25	–	–	ns
CLKO LOW time	t_{CLKL}	15	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ change	t_{VCH}	10	–	–	ns
R, G, B, $\overline{VDS}$ valid to CLKO rise	t_{VOC}	10	–	–	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ valid	t_{COV}	–	–	60	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall	t_{FOD}	0	–	30	ns
Skew between outputs R, G, B, $\overline{VDS}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{VDS}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	t_{UOD}	0	–	60	ns
CLKO HIGH to $\overline{FS}/\overline{DDA}$ change	t_{DCH}	10	–	60	ns
$\overline{FS}/\overline{DDA}$ valid to CLKO rise	t_{DOC}	5	–	–	ns
F1 HIGH time (note 7)	t_{F1H}	–	500	–	ns
F1 LOW time (note 7)	t_{F1L}	–	500	–	ns
F6 HIGH time	t_{F6H}	–	83	–	ns
F6 LOW time	t_{F6L}	–	83	–	ns
$\overline{OD}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{OD}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 8, 9 and Fig. 7)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
Cycle time	t_{cyc}	–	500	–	ns
$\overline{UDS}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{AS}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{AS}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{UDS}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time	t_{LDS}	200	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	320	–	–	ns
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	305	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	15	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	275	ns
Link-through buffers (notes 8, 9 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from FTFROM (Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	40	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	250	–	350	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to FTFROM (Fig. 10)					
Write cycle time (note 10)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/F6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/F6) rise	t_{UF6}	20	–	–	ns
F6 (component of F1/F6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. Pin 30 must be biased externally.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. All timings are related to a 6,00 MHz clock.
5. CLKO, R, G, B, F1/F6, $\overline{VDS}$: C_L = 25 pF.
   $\overline{FS}$/$\overline{DDA}$: C_L = 50 pF
6. CLKO, F1/F6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0,8 to 2,0 V
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2,7 V
7. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
8. C_L = 150 pF.
9. Reference levels = 0,8 to 2,0 V.
10. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will than depend on the internal synchronization time.

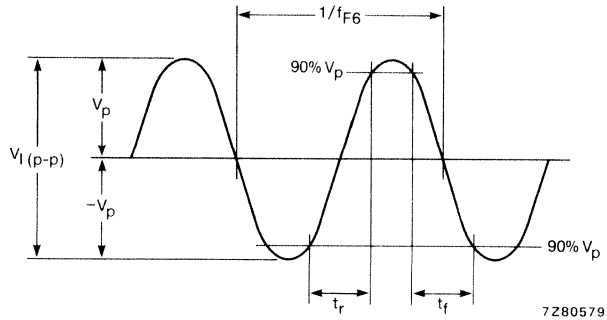
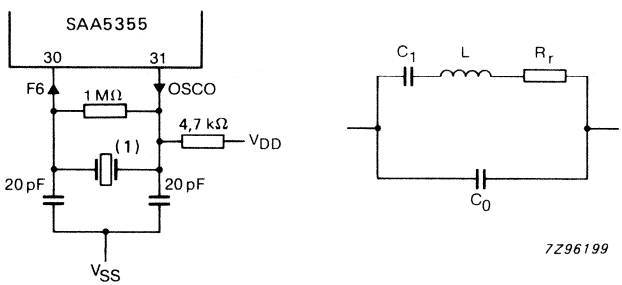


Fig. 3 F6 input waveform.



(1) for 525-line operation, frequency = 6,041957 MHz.

Fig. 4(a) Oscillator circuit for SAA5355 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

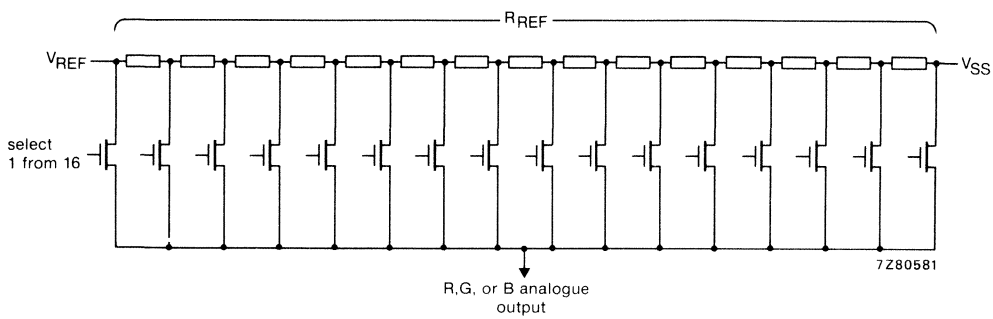


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

DEVELOPMENT DATA

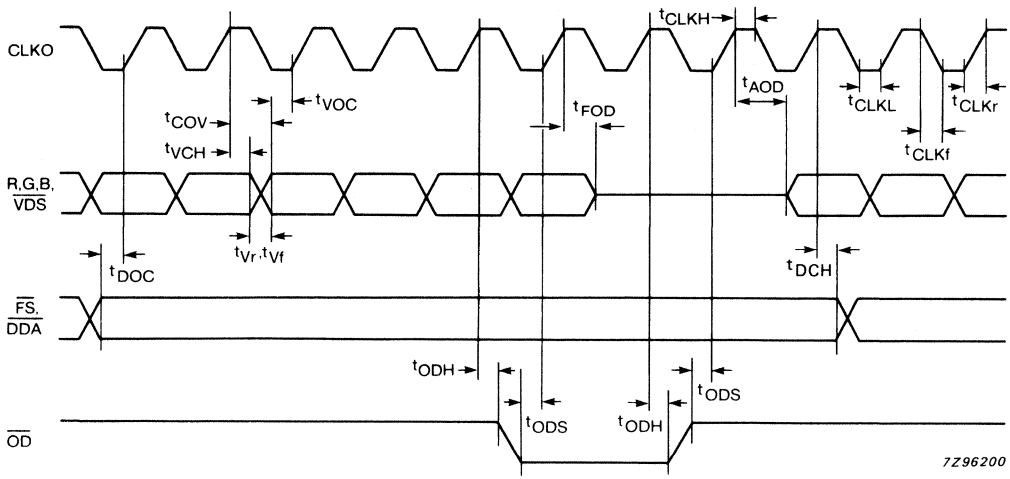


Fig. 6 Video timing.

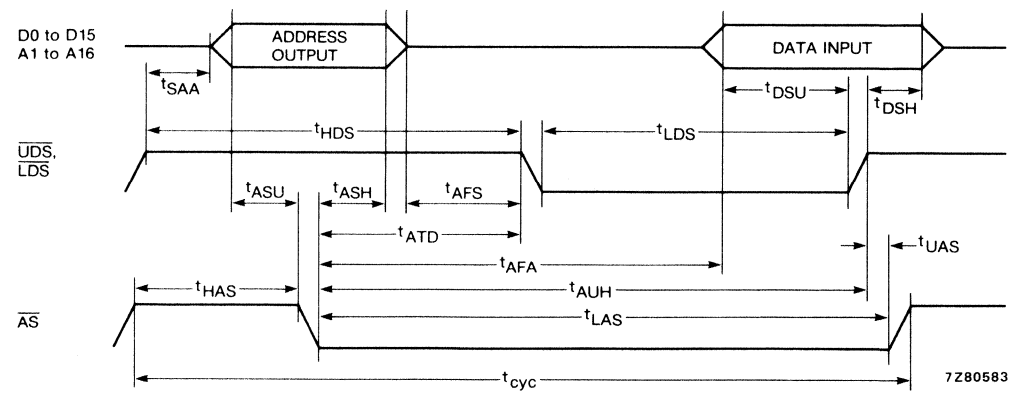


Fig. 7 Memory access timing.

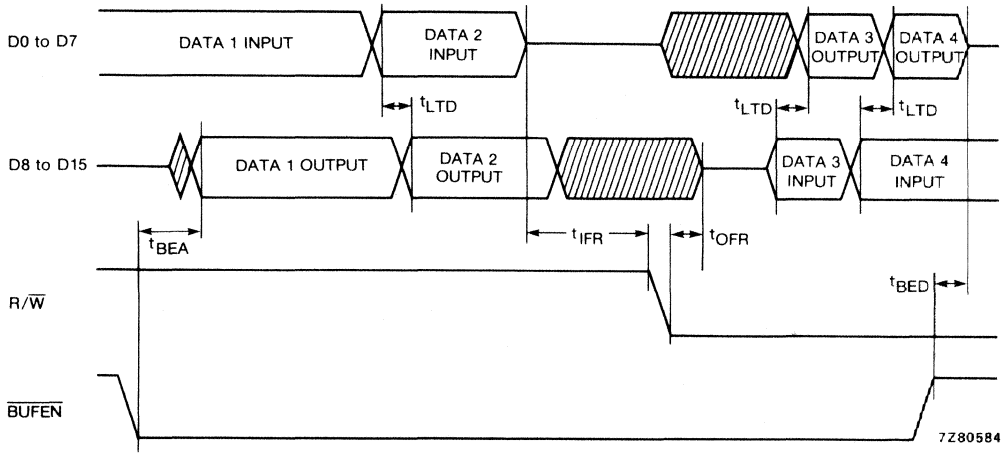


Fig. 8 Timing of link-through buffers.

DEVELOPMENT DATA

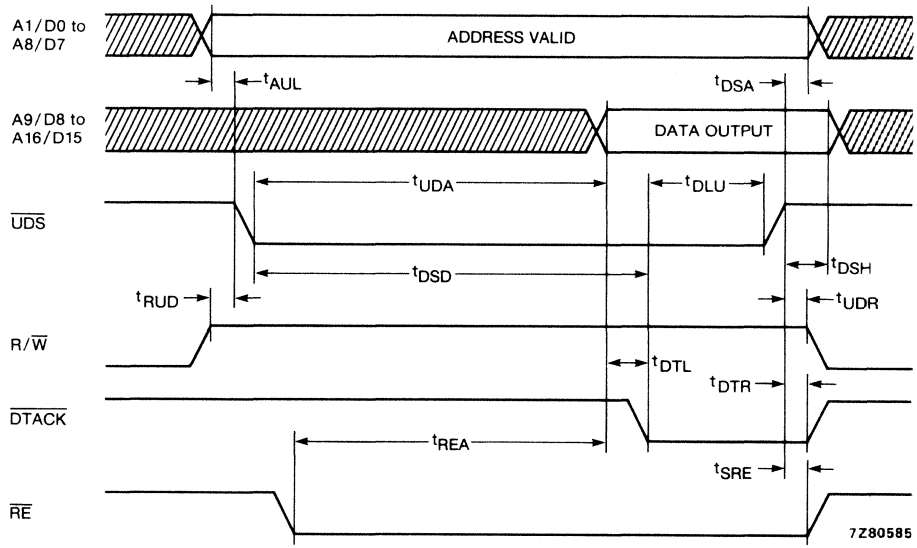


Fig. 9 Timing of microprocessor read from FTFROM.

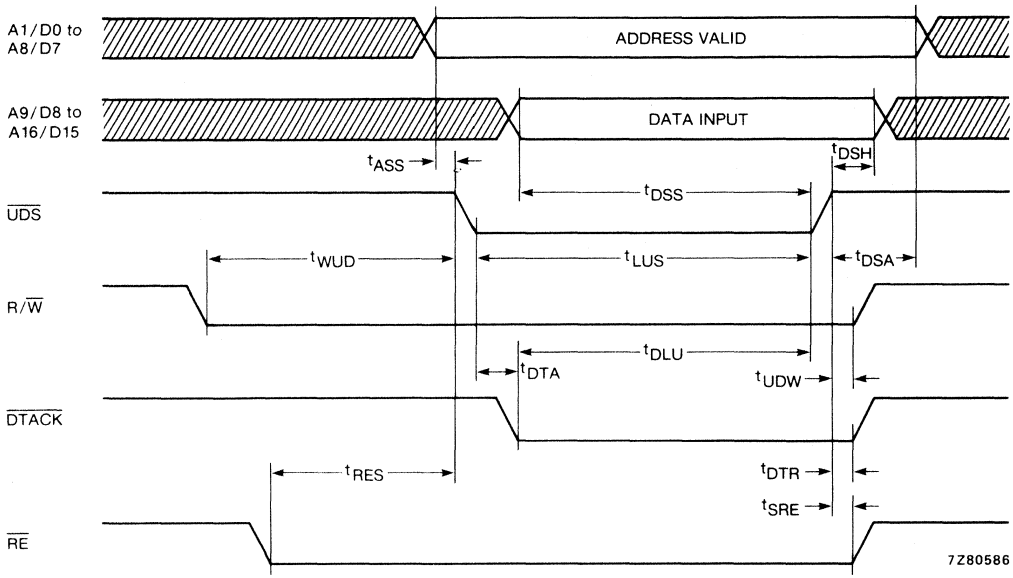


Fig. 10 Timing of microprocessor write to FTFROM.

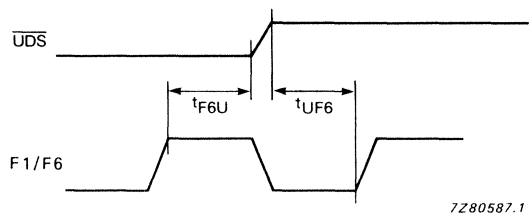


Fig. 11 Timing of F1/F6 to memory access cycle.

DEVELOPMENT DATA

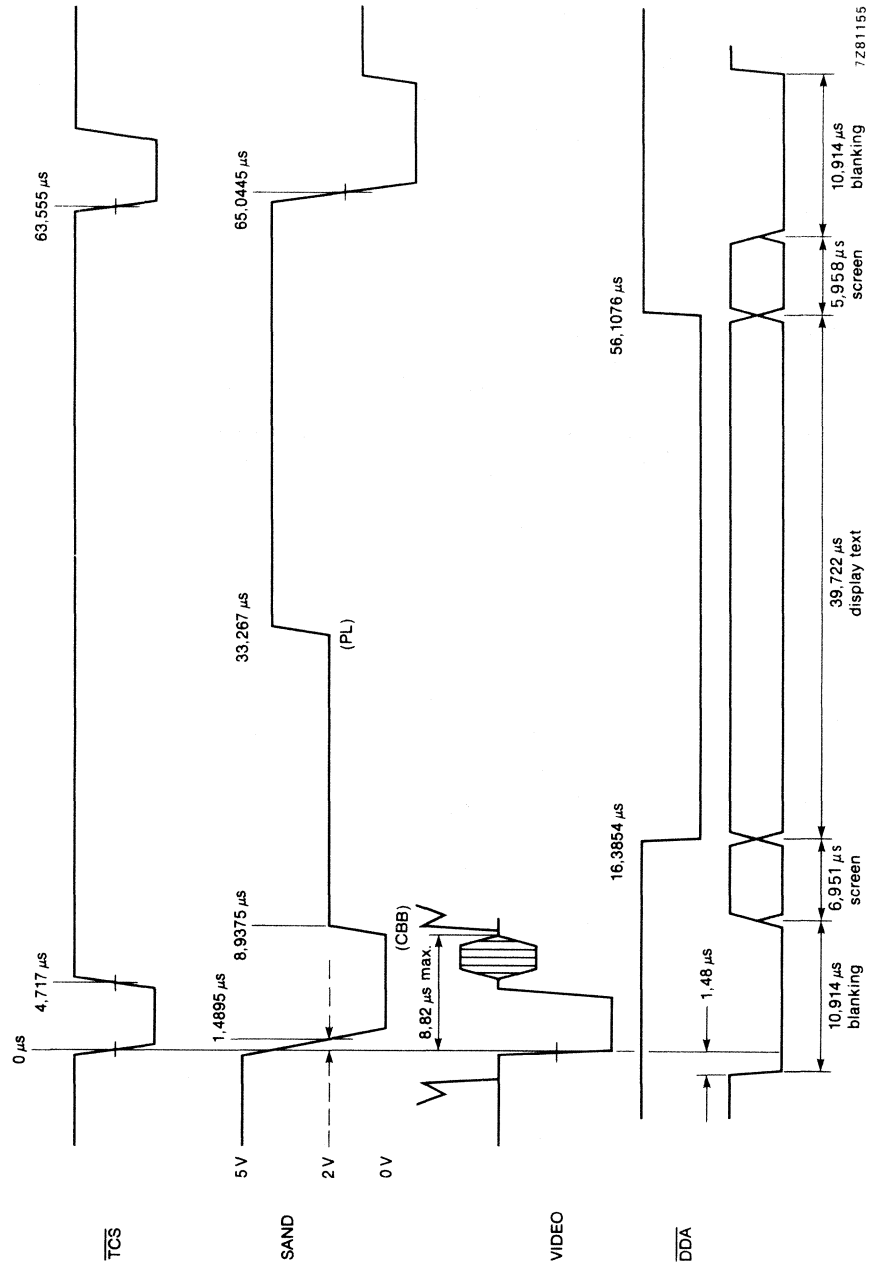


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume f_{F6} = 6,041957 MHz.

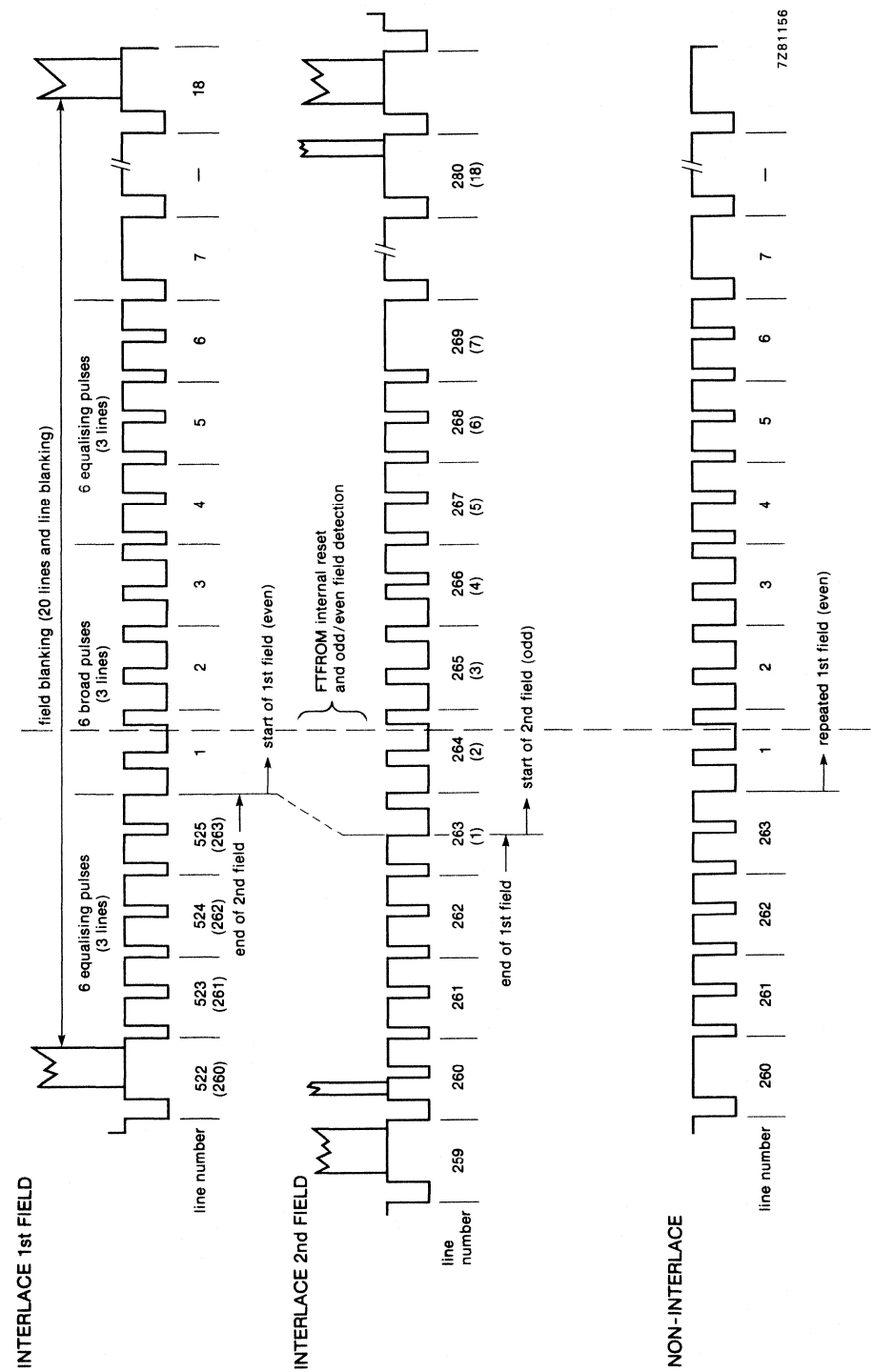


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4,717 μs; equalizing pulse widths = 2,23 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

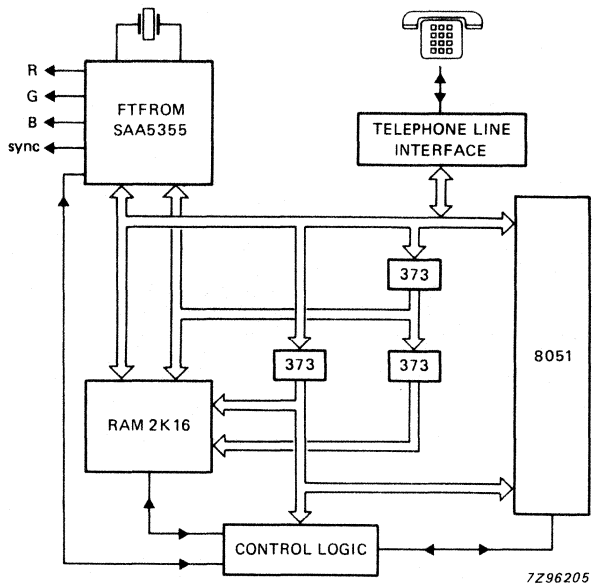


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows — each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

The timing chain operates from an external 6,041957 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 20/21 rows per page and 10 video lines per row. FTFROM will also operate with 25 rows per page and 9 video lines per row.

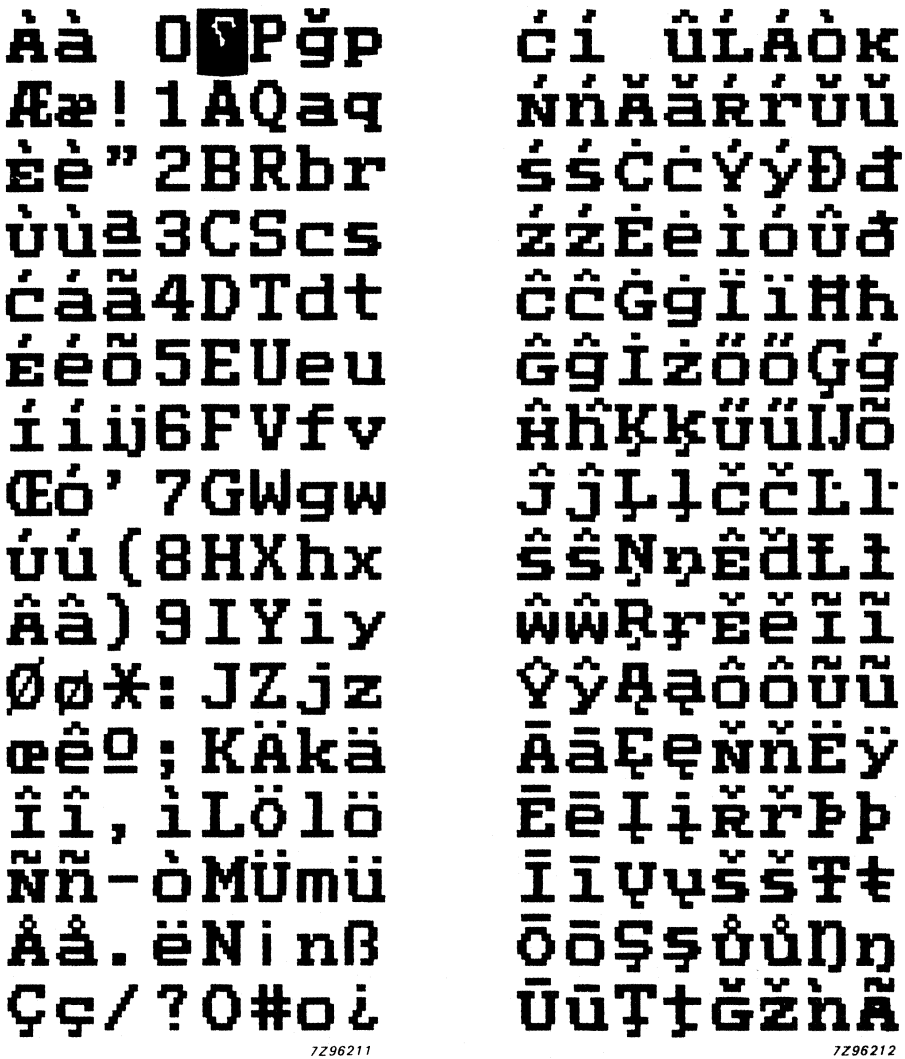
The display is generated to the normal 525-line/59,94 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at approximately 1 MHz or 6 MHz (pin 29) is available for driving other devices, and a clock output (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Character generation

FTFROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The fixed character tables (Tables 0 to 3), shown in Figs 15 and 16, are applicable to 10-lines-per-row applications. For 9 lines per row applications, the characters will be as shown but with the last line removed from alpha characters and line 5 (labelling 0 to 9) removed from mosaic and line drawing characters.



7Z96211

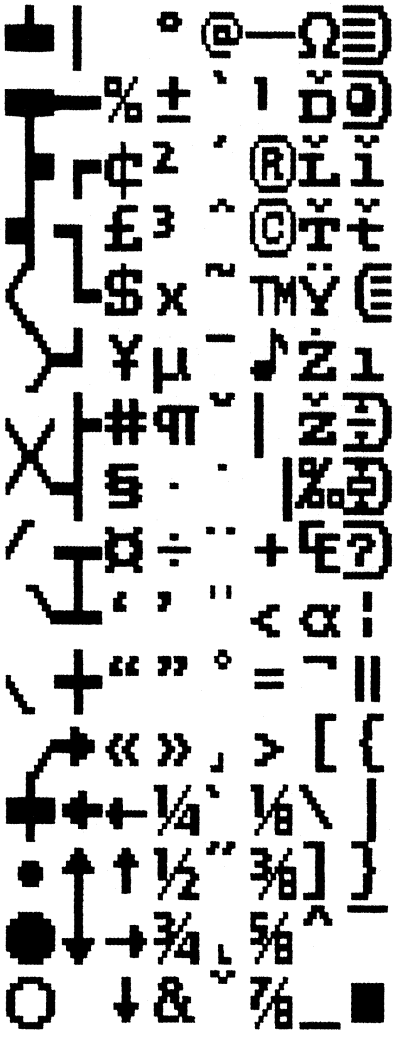
(a)

7Z96212

(b)

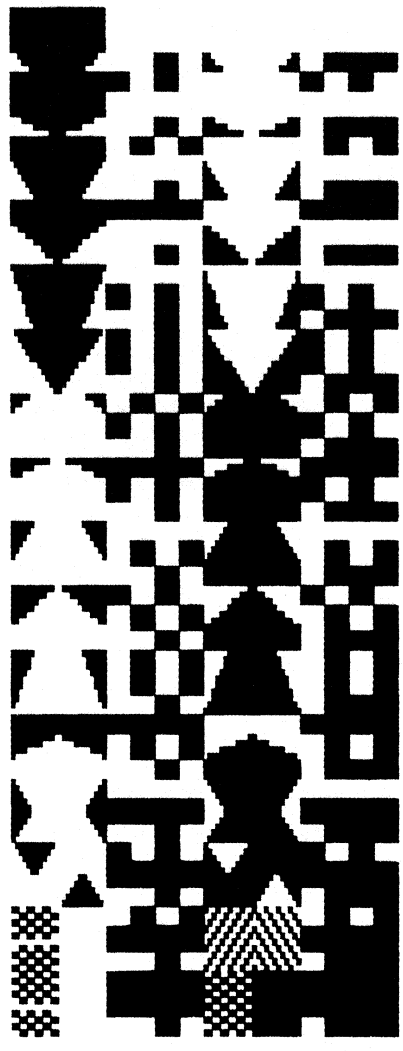
Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.

DEVELOPMENT DATA



7Z96213

(a)



7Z96214

(b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

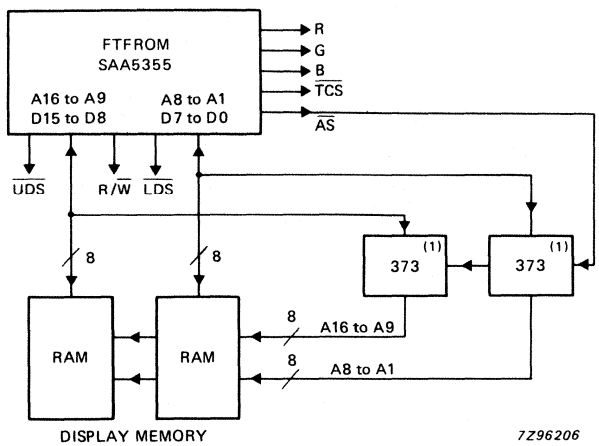
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- FTFROM fetches data from the display memory
- The microprocessor reads from, or writes to, FTFROM's internal register map
- The microprocessor accesses the display memory

FTFROM access to display memory (Figs 17 and 18)

FTFROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 496,5 ns (F6 = 6,041957 MHz). The address strobe ($\overline{AS}$) signal from FTFROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although FTFROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

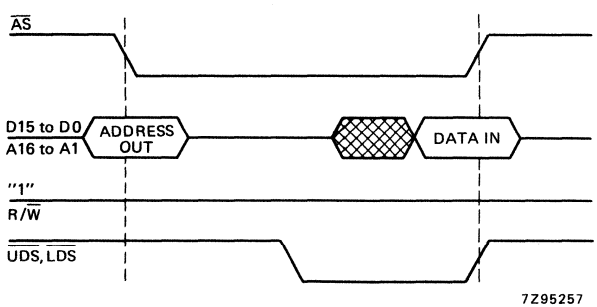


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

FTFROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain – there are no odd-numbered word addresses.

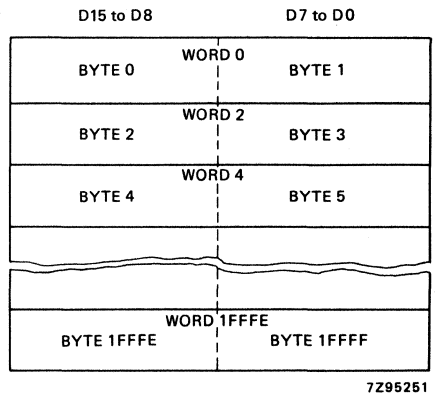


Fig. 19 Display memory word/byte organization.

Warning time

As FTFROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by FTFROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and FTFROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that FTFROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of FTFROM's bus activity is programmable to be between 0 and 22,84 μs.

Microprocessor access to register map

FTFROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

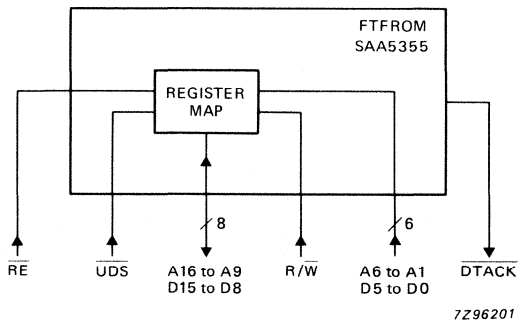


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to FTFROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by FTFROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of FTFROM's scroll map contents at a location in its main memory.

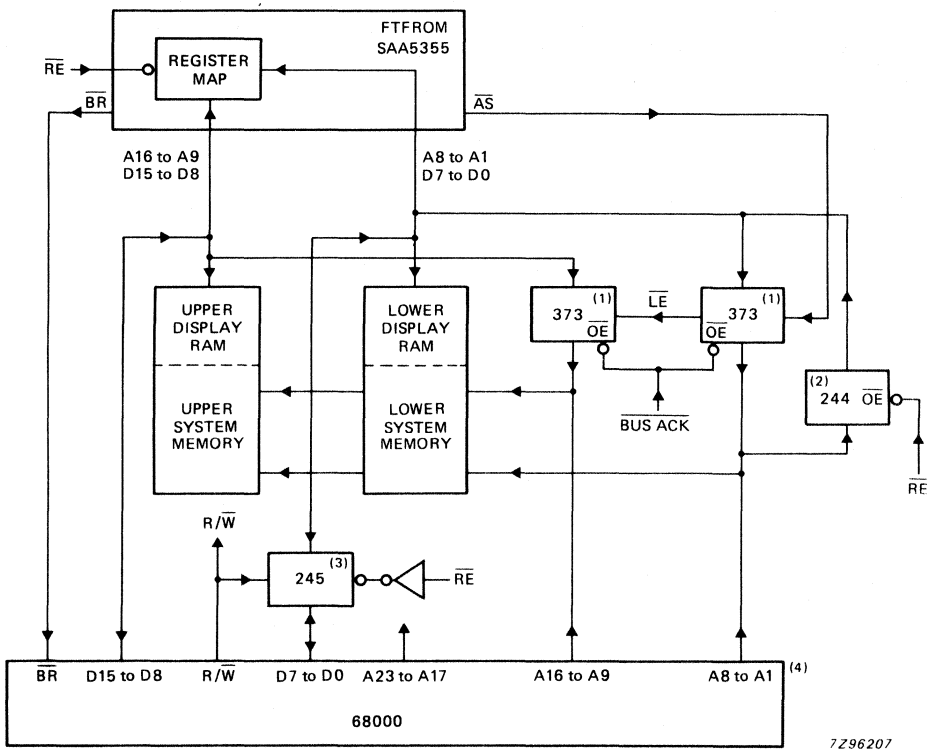
8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, FTFROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by FTFROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

DEVELOPMENT DATA

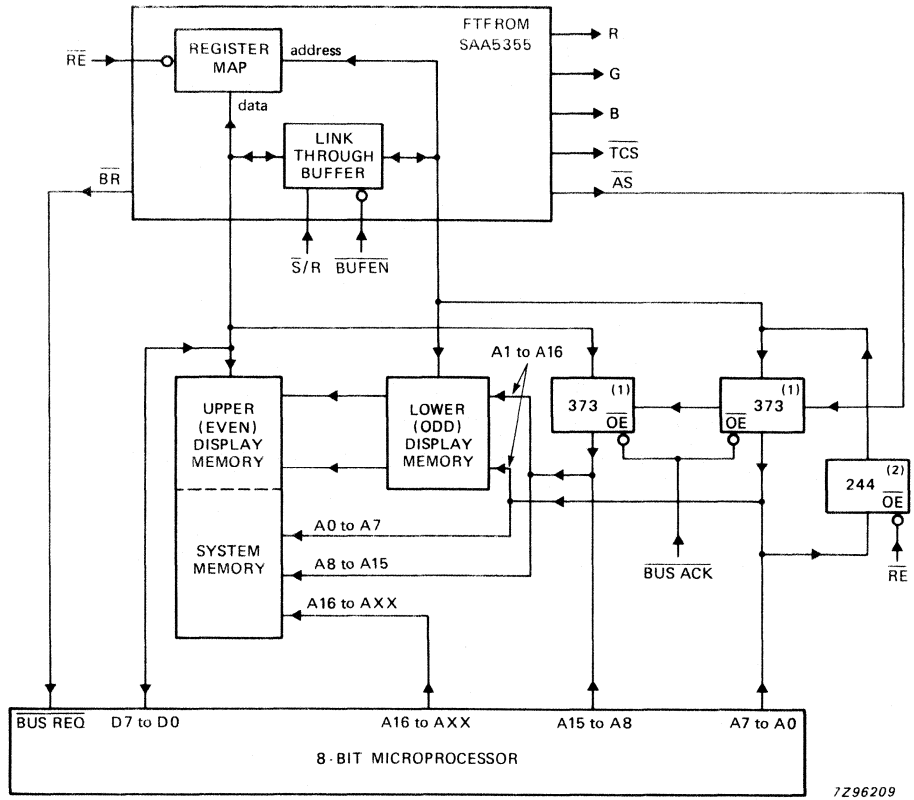
APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.

DEVELOPMENT DATA



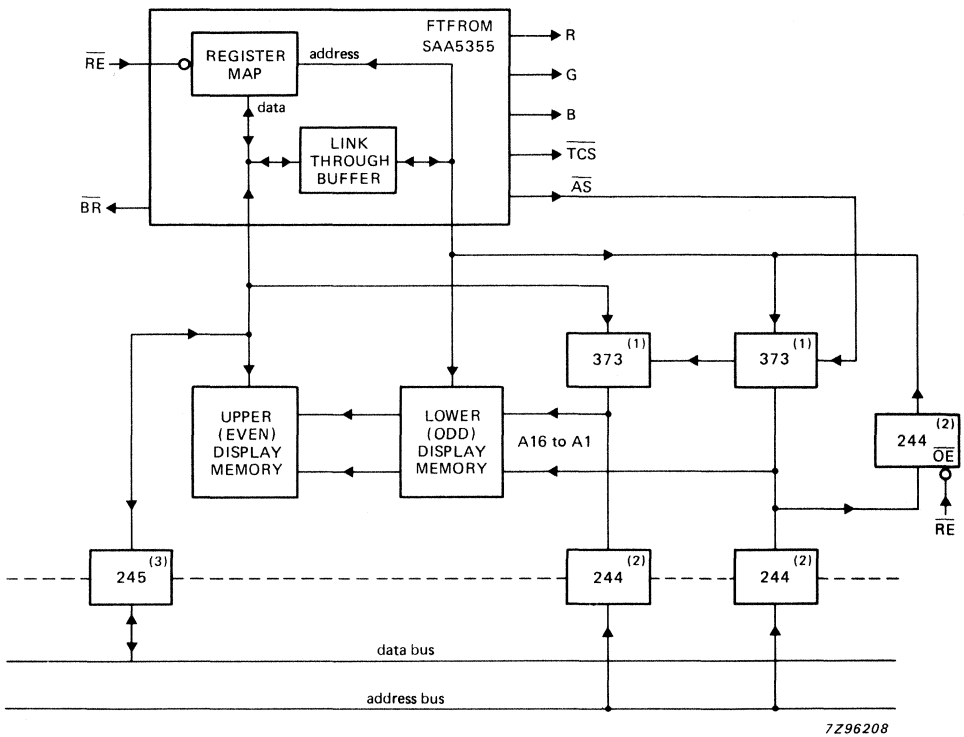
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect FTFROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses FTFROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) FTFROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6,041957 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

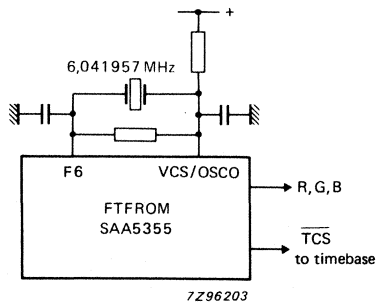


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode FTFROM synchronizes directly to another device as shown in Fig. 25. FTFROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using FTFROM's internal field sync separator.

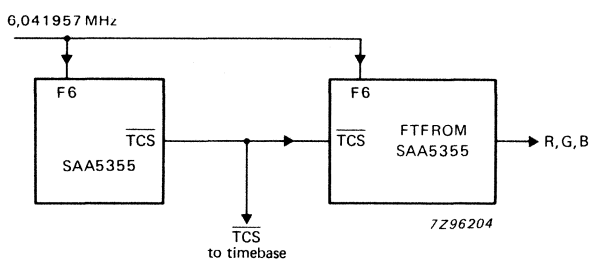


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. A phase-locked VCO in the SAA5230 teletext video processor provides sync to the timebases. When FTFROM is active, its horizontal counter forms part of the phase control loop – a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to FTFROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from FTFROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possibilities.

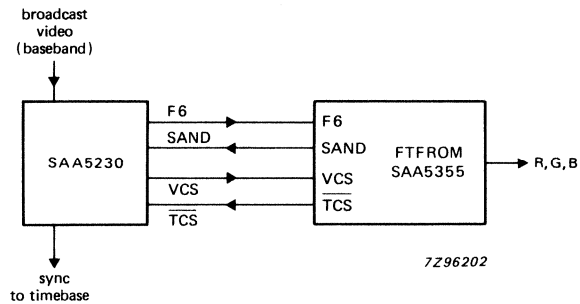


Fig. 26 Phase-locked slave (indirect sync) mode.

BACKGROUND MEMORY CONTROLLER

GENERAL DESCRIPTION

The SAA9030 background memory controller (BMC) is for application in memory-based feature tv receivers. It directs teletext data from the teletext video processor to a FIFO-organized CCD memory, refreshes the CCD memory arrays and, when in teletext mode, supplies the teletext data to a computer-controlled teletext decoder after a page request.

The background memory controller, together with the computer-controlled teletext extension (CCTE, SAA9040) can be used in a 'stand-alone' system or with a picture enhancement processor (PEP, SAA9010) in feature television applications. Inputs and outputs excepting F_6, TTDI and TTCI are TTL-compatible.

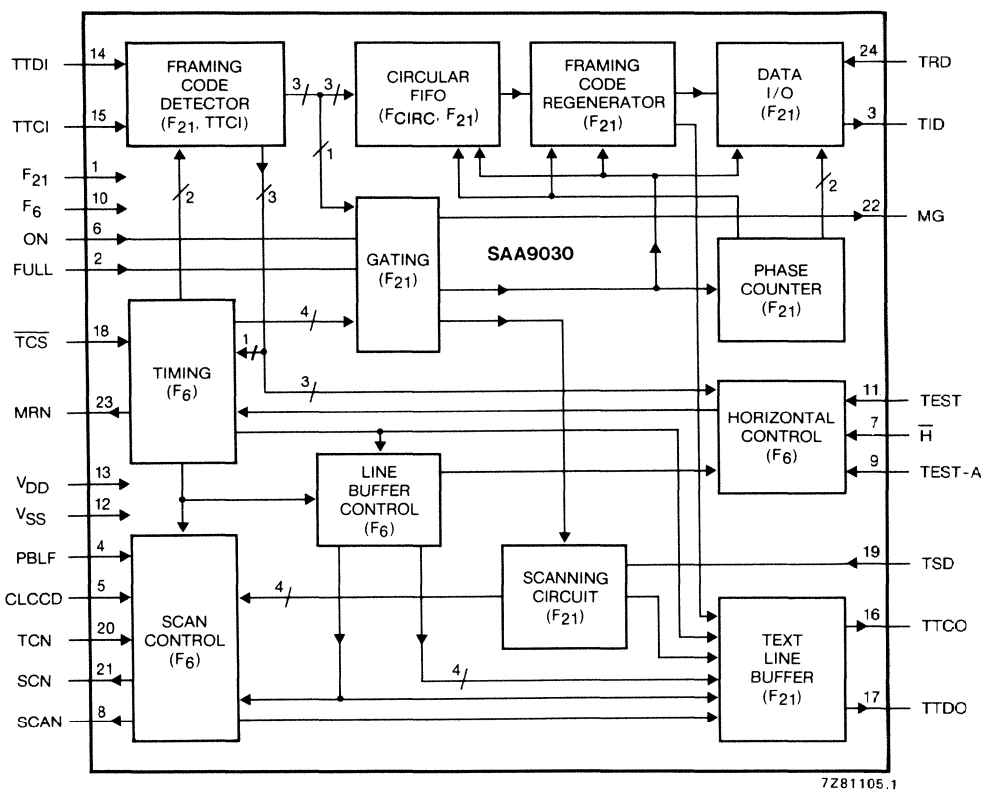


Fig. 1 Block diagram.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101B).

PINNING

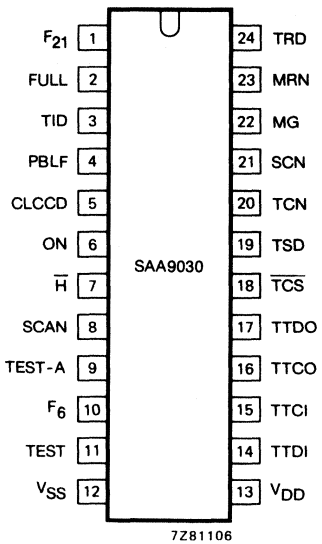


Fig. 2 Pinning diagram.

1	F_{21}	master clock input. 20,25 MHz line-locked in feature tv applications; 20,8 MHz (approx.) free-running in stand-alone applications
2	FULL	full channel mode select input. When HIGH, the BMC is in full channel mode
3	TID	teletext data to CCD memory. Bit rate of serial data stream is defined by F_{21}
4	PBLF	page-being-looked-for, command input
5	CLCCD	clear CCD, command input
6	ON	activate-BMC, command input. When LOW, MRN and MG are floating, and TTDI is resynchronized to $\overline{TCS}$ and routed to TTDO
7	$\overline{H}$	horizontal timing input at tv line frequency (from CCTE)
8	SCAN	output to indicate that memory scanning is in progress
9	TEST-A	test input. LOW for normal operation
10	F_6	6 MHz clock input. Internal a.c. coupling
11	TEST	test input. LOW for normal operation
12	V_{SS}	negative supply voltage (ground)
13	V_{DD}	positive supply voltage
14	TTDI	teletext data input. Serial bit stream from video input processor during active teletext lines in data entry window. Bit rate is defined by TTCI. External a.c. coupling, internal clamping
15	TTCI	teletext clock input. 6,9375 MHz. Internal a.c. coupling
16	TTCO	teletext clock output. Frequency = $^1/_3 F_{21}$; typical duty factor = 50%
17	TTDO	teletext data output. Serial bit stream active during CCD scanning and DEW (data entry window). Bit rate is defined by TTCO
18	$\overline{TCS}$	teletext composite sync. Defines BMC timing

19	TSD	teletext scanned memory data. Serial bit stream from one of the CCDs via the picture enhancement processor or multiplexer. Bit rate defined by F_{21}
20	TCN	terminal count input. Command from picture enhancement processor or external counter to start the second or third scan of the CCDs, or that a third scan is complete. Active LOW
21	SCN	start count output. Active LOW
22	MG	memory gating. Three-state output controlled by "ON" input. Active, if enabled, during reception of teletext data packets, and during memory recirculation
23	MRN	memory recirculate. Three-state output enabled by "ON" input. When enabled gives a HIGH during tv lines 7 to 22 and 320 to 335. Also used as scan clock for picture enhancement processor or external counter
24	TRD	teletext recirculated data. Serial bit stream from last CCD. Bit rate defined by F_{21}

FUNCTIONAL DESCRIPTION

Generation of MG and MRN signals

The background memory controller generates the memory gating (MG) and memory recirculate (MRN) signals required by the CCD memory arrays. These signals are available only when the "ON" input from the CCTE is HIGH (when "ON" is LOW, MG and MRN are in the high-impedance OFF-state).

Data storage during the vertical blanking interval

Teletext data packets (one data packet per tv line) are supplied from the video input processor at a bit rate of 6,9375 Mbits/s to pin TTDI. The incoming data is temporarily stored in a circular FIFO register from the start of the incoming line until the first bit can be stored in the CCD memory.

A valid data line carries a framing code that is recognized by the BMC. Detection of the framing code is performed during the Data Entry Window (DEW) which is a gate derived from the negative edge of the Text Composite Sync ($\overline{TCS}$) signal and is active during lines 7 to 22 and 320 to 335 of a tv picture. The time slot for detection (frame code window) is active from 12 to 15 μs in a tv line and this timing is derived from the horizontal timing pulse ($\overline{H}$). The framing code is regenerated within the BMC.

When valid teletext data is recognized, it is synchronized to one-third of the master clock frequency (F_{21}). As a line of teletext data is being shifted out via pin TID to the CCD memory input, it is interleaved with teletext recirculated data received at pin TRD from the last of the CCD memory stages. Interleaving is performed in three phases on a bit-by-bit basis.

During the data entry window all CCDs are set to the 'serpentine mode' in which a line of data leaving pin TID is written into the first CCD as the output data from the first CCD is written into the second CCD. This repeats through all the CCDs and results in a one-line shift of data through the whole memory, the last line becoming available at the TRD input.

When the 'full channel mode' is activated (FULL = HIGH):

- the BMC is forced to an internal OFF-state and incoming data lines are redirected to the computer-controlled teletext decoder (CCT, SAA5240), the data is not stored in the CCDs and no scan is made after a page request;
- the framing code can be recognized in all tv lines and not only during the data entry window.

FUNCTIONAL DESCRIPTION (continued)

Data scanning after a page request

The page-being-looked-for (PBLF) input from the CCTE originates in the CCT and indicates that the latter is searching for a requested page. As the PBLF input goes HIGH, the BMC activates the start scan output (SCN = LOW) and this presets an external counter and multiplexer (picture enhancement processor or TTL circuits). The preset value takes the multiplexer to the last CCD and therefore depends on the number of CCDs connected.

The multiplexer selects one CCD output at a time, starting with the last CCD (oldest information) and finishing with the first CCD (newest information). Three scans of the CCDs are required before all stored information is retrieved due to the three-phase interleaving (a memory with "n" CCDs will require a scanning period of 3n tv fields). Stepping of the counter/multiplexer occurs with the rising edge of MRN (at field flyback), and after each scan of all CCD outputs the external counter generates a terminal count signal TCN to initiate the next scan.

As each CCD is selected, the data is shifted from the memory by the clock F_{21} and supplied via the multiplexer to the teletext scan data pin TSD. A scanning circuit in the BMC selects one of the three phases from the CCD line for output, reducing the output bit-rate to one-third of F_{21}. The resulting bit stream is then synchronized to the CCT line-timing and fed to the CCT decoder that operates in the full-channel mode. The data packets retrieved by the scanning circuit are supplied at one packet per tv line via the output pin TTDO to the CCT decoder.

After the third scan of the CCDs, the BMC returns to the 'direct mode' in which it directs all incoming data lines to the CCT decoder and to the CCDs. This is necessary for updating a displayed page, or when a requested page was not found during the scan.

Repositioning of data

The BMC incorporates a variable length shift register in the output circuit supplying data TTDO. This accommodates a complete data line and introduces a delay that allows synchronization of the data to the CCT line-timing. The length of the delay depends on the position of the data in the tv line and on the RGB delay value that is programmed into the CCTE. In the BMC, the length of the delay is controlled automatically from the timing of $\overline{TCS}$ compared with the start of incoming data.

Refreshing CCD memories

CCD refreshing is required to maintain valid data and is done outside of the vertical blanking interval. At this time the 'serpentine mode' of the memory is broken and each CCD recirculates its contents once. To do this, the BMC supplies a sequence of 294 MG pulses (the number of memory lines per CCD) to all CCDs with recirculate activated (MRN = LOW). The MG signal is synchronized to the tv line frequency (one MG cycle per tv line) so that at the end of each tv field all data in the CCD arrays are returned to their original positions.

Clearing CCD memories

When a LOW-to-HIGH transition is detected at the CLCCD input, the scanning circuit is activated as follows:

- the memory recirculate control MRN is held HIGH except during the first line of the data entry window DEW (normally, MRN HIGH period is equal to DEW). This maintains the CCD serpentine mode during the recirculation time. The LOW on MRN during the first line of DEW acts as a clock input to the counter/multiplexer;
- the data output to the first CCD from pin TID is held LOW so that all CCDs are filled with zeros;
- the BMC is forced into the 'direct mode' so that no incoming teletext lines are missed during the CCD-clearing time.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range (pin 13)	V_{DD}	−0,5 to + 7,0	V
Maximum supply current (pin 13)	I_{DD}	max. ▲	mA
Maximum supply current (pin 12)	I_{SS}	max. ▲	mA
Input voltage range (not F_6, TTCI)	V_I	−0,5 to (V_{DD}+ 0,5)*	V
Input voltage range (F_6, TTCI)	V_I	−0,5 to + 12	V
Maximum input current	$\pm I_I$	max. 10	mA
Maximum output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	−25 to + 85	°C
Maximum power dissipation per output	P_O	▲	mW
Maximum power dissipation per package	P_{tot}	▲	W
Storage temperature range	T_{stg}	−55 to + 150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	–	5,5	V
Quiescent supply current at T_{amb} = 25 °C; all inputs at V_{DD} or V_{SS}; TEST and TEST-A at 4,6 V; I_O = 0 mA	I_{DD}	–	–	100	μA
Inputs					
F_6 clock (a.c. coupled)					
D.C. input voltage	V_I	4,0	–	8,0	V
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	3,0	V
Leakage current	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	6	pF

▲ Values under investigation.

* V_{DD}+ 0,5 V not to exceed 8,0 V.

D.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Inputs (continued)					
TTCI data clock (a.c. coupled)					
D.C. input voltage	V_I	4,0	–	8,0	V
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	3,0	V
Leakage current	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	6	pF
F_{21}, TRD, TSD, $\overline{H}$, PBLF, CLCCD, ON, $\overline{TCS}$, TCN, TEST, TEST-A					
Input voltage LOW	V_{IL}	–	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	–	V
Leakage current at V_{IL}	I_{LI}	–	–	10	μA
Leakage current at V_{IH}	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	5	pF
Outputs TTDO, TTCO, TID, SCAN, SCN					
Output voltage LOW at I_{OL} = 2,0 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at I_{OH} = 100 μA	V_{OH}	2,4	–	–	V
3-state outputs MRN, MG					
Output voltage LOW at I_{OL} = 2,0 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at I_{OH} = 0,5 mA	V_{OH}	2,4	–	–	V
Leakage current at V_{OL}	I_{LO}	–	–	10	μA
Leakage current at V_{OH}	I_{LO}	–	–	10	μA
Input/output TTDI (input incorporates an active clamping circuit)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2,4	–	4,0	V
Input leakage current	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	6	pF
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
External coupling capacitor	C_{ext}	–	10	–	nF

DEVELOPMENT DATA

A.C. CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Clocks F_6, TTCI (Fig. 3)					
F_6 frequency	f	–	6,0	–	MHz
F_6 rise and fall times (between 10% and 90% levels)	t_r, t_f	10	–	66	ns
TTCI frequency	f	–	6,9375	–	MHz
TTCI rise and fall times (between 10% and 90% levels)	t_r, t_f	10	–	57	ns
F_6, TTCI duty factor at d.c. level		30	50	70	%
Clock F_{21} (Fig. 4)					
Frequency	f	20,2	–	20,9	MHz
HIGH time	t_{CH}	17	–	–	ns
LOW time	t_{CL}	17	–	–	ns
Rise and fall times (between 0,8 and 2,0 V levels)	t_r, t_f	–	–	3	ns
Video processor interface (Fig. 3)					
Set-up time input to TTCI	t_{SU}	40	–	–	ns
Hold time TTCI to input	t_{IH}	40	–	–	ns
CCT decoder interface (Figs 3 and 5)					
TTCO clock output					
Frequency	f	–	$^1/_3 F_{21}$	–	MHz
Duty factor		40	–	60	%
Rise and fall times (between 10% and 90% levels)	t_r, t_f	–	–	40	ns
Load capacitance	C_L	–	–	50	pF
TTDO output, $\overline{TCS}$ input					
Set-up time $\overline{TCS}$ to F_6	t_{SU}	40	–	–	ns
Hold time F_6 to $\overline{TCS}$	t_{IH}	40	–	–	ns
Relative delay TTDO to TTCO	t_{RD1}	40	–	–	ns
Relative delay TTCO to TTDO	t_{RD2}	40	–	–	ns

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
CCTE interface (Fig. 3)					
Inputs $\overline{H}$, PBLF, CLCCD, ON; output SCAN					
Set-up time input to F_6	t_{SU}	40	–	–	ns
Hold time F_6 to input	t_{IH}	40	–	–	ns
Output delay F_6 to output	t_{OD}	–	–	40	ns
Load capacitance	C_L	–	–	50	pF
PEP, TTL, CCD interface (Figs 3 and 4)					
Inputs TRD, TSD; outputs TID, MG					
Set-up time input to F_{21}	t_{SU}	8	–	–	ns
Hold time F_{21} to input	t_{IH}	0	–	–	ns
Output delay F_{21} to output	t_{OD}	6	–	33	ns
TID load capacitance	C_L	–	–	25	pF
MG load capacitance	C_L	–	–	60	pF
Input TCN; outputs SCN, MRN					
Set-up time input to F_6	t_{SU}	40	–	–	ns
Hold time F_6 to input	t_{IH}	40	–	–	ns
Output delay F_6 to output	t_{OD}	–	–	40	ns
MRN load capacitance	C_L	–	–	70	pF
SC load capacitance	C_L	–	–	50	pF

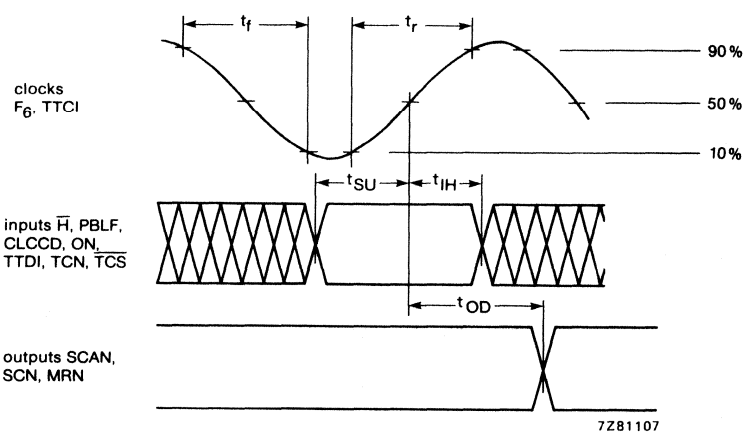


Fig. 3 Timing with respect to clocks F_6 and TTCI.

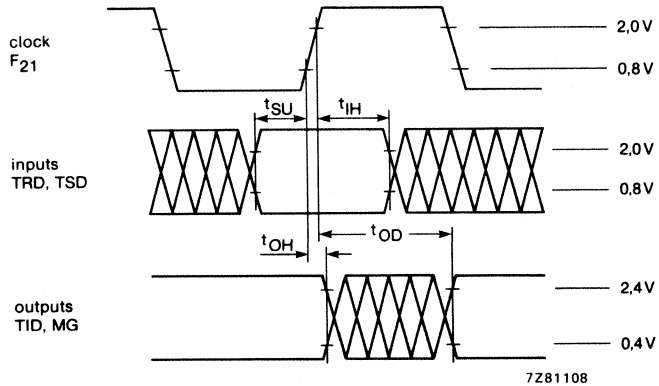


Fig. 4 Timing with respect to clock F_{21}.

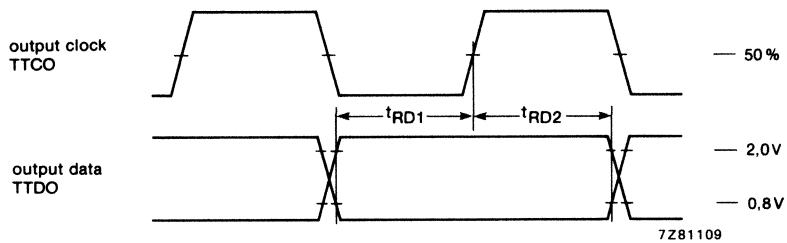


Fig. 5 Timing with respect to clock TTCO.

COMPUTER-CONTROLLED TELETEXT EXTENSION

GENERAL DESCRIPTION

The SAA9040 computer-controlled teletext extension (CCTE) for memory-based feature tv receivers is used together with a background memory controller (BMC, SAA9030) to organize the storage of teletext data in a field memory before processing by a CCT decoder (CCT, SAA5240). The CCTE shares the address and data buses of the CCT and a single-page display RAM and transfers commands indirectly from the I^2C bus to the BMC; it blanks the display for non-transmitted rows and provides the required delays for video/teletext operation.

The CCTE, together with the BMC, can be used in a 'stand-alone' system or with a picture enhancement processor (PEP, SAA9010) in feature television applications.

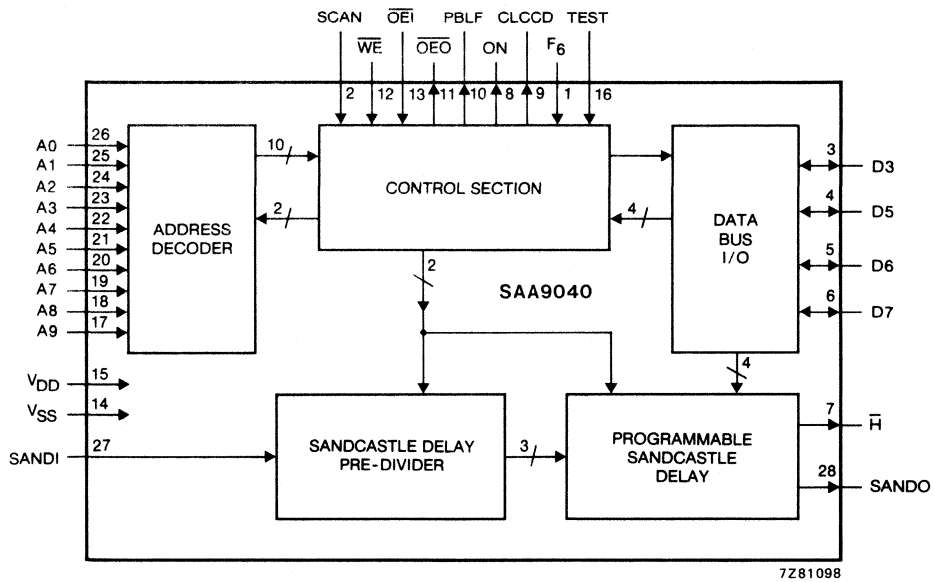


Fig. 1 Block diagram.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

PINNING

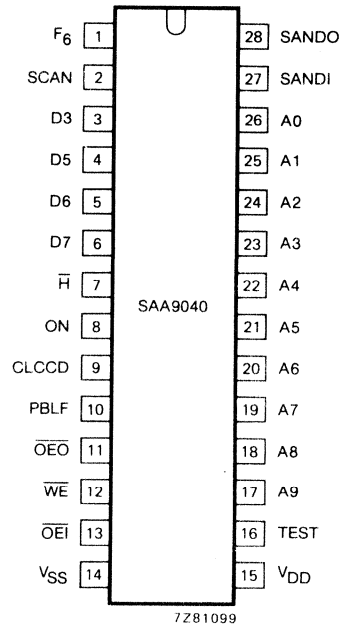


Fig. 2 Pinning diagram.

1	F_6	6 MHz clock input from the video input processor. Internal a.c. coupling
2	SCAN	input from BMC indicating that memory scanning is in progress
3 4 5 6	D3 D5 D6 D7	I/O data bus. Input used for commands into CCTE. Output if RAM address indicates rows not received from the page display RAM, D3, D5, D6 and D7 then force character codes on the data to effect an empty row
7	$\overline{H}$	horizontal timing output at tv line frequency. Derived from sandcastle pulse SANDO
8	ON	command output to activate BMC/CCD interface. Controlled initially by I^2C command. LOW after power-on
9	CLCCD	clear CCD command, output to BMC. Controlled initially by I^2C command
10	PBLF	page-being-looked-for, command output to BMC. This signal is a copy of the PBLF bit written into the page display RAM by the CCT
11	$\overline{OEO}$	output enable to page display RAM. Disables the RAM output if a row is not allowed for display
12	$\overline{WE}$	write enable input. Indicates that the CCT writes into the page display RAM. Is used in the control section of the CCTE to access the row-found register during acquisition and command transfer
13	$\overline{OEI}$	output enable input. Indicates that the CCT reads from the page display RAM. Is used in the control section of the CCTE to access the row-found flag register during display
14	V_{SS}	negative supply voltage (ground)

15	V_{DD}	positive supply voltage
16	TEST	test input. HIGH for normal operation
17	A9	address bus from the CCT to the page display RAM and CCTE. Decoding is performed in the CCTE control section to address the row-found flag and command registers
18	A8	
19	A7	
20	A6	
21	A5	
22	A4	
23	A3	
24	A2	
25	A1	
26	A0	
27	SANDI	sandcastle pulse input. A three-level signal from the CCT decoder giving phase lock and colour burst blanking information
28	SANDO	sandcastle pulse output to the teletext video processor. This pulse is a copy of SANDI delayed according to commands on the I^2C bus and is used to adjust the timing of the RGB signal.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

General

The CCTE shares data and address buses with the CCT and page display RAM. This allows indirect transfer of I^2C commands for system control, the I^2C commands being written to the RAM by the CCT and read from the RAM by the CCTE.

The following information is written to/read from the page display RAM:

information	*RAM location*	
received page	rows 0 to 23	
status row	row 24	
page-being-looked-for	row 25, col. 9, D5	additional page-related data
clear page bit from page header	row 25, col. 3, D3	additional page-related data
RGB delay	row 25, col. 11, D3, D5, D6, D7	data written to/read from RAM via CCT I^2C bus
CLCCD (clear CCDs)	row 25, col. 12, D5	data written to/read from RAM via CCT I^2C bus
ON (activate BMC)	row 25, col. 12, D3	data written to/read from RAM via CCT I^2C bus

Row-found flags

In the full channel acquisition mode, the CCT does not clear the page display RAM after it receives a requested page and does not respond to the page clear bit (C4) in page headers. These functions are performed by the CCTE which has 23 row-found flags (RFFs) for this purpose, one for each of the page display RAM rows 1 to 23. All RFFs are cleared on the rising edge of PBLF and on detection by CCTE of the page clear bit (C4 = 1) in the header of the requested page. An RFF is set when the CCT writes a character into the corresponding row of the RAM. During display, the CCT reads the row's contents sequentially from the RAM. Normally the RAM output enable ($\overline{OEO}$) is a copy of the output enable of the CCT ($\overline{OEI}$).

If a row is read and the corresponding RFF is not set, the output enable $\overline{OEO}$ is suppressed and the data bits D3, D5, D6 and D7 are forced LOW giving the effect of a row of spaces on the screen.

RGB delay

To compensate for delays in the video signal path, the CCTE regenerates the incoming sandcastle pulse with a delay that matches the timing of the CCT to that of the delayed (processed) video. The delay must be programmed into the page display RAM in the format shown in Table 1. The programmable values are in steps of 1 μs. For the combination CCTE + BMC only delays between 0 and 9 μs are applicable.

Table 1 RGB delay programming

address	row 25, column 11							
data bus	D7	D6	D5	D4	D3	D2	D1	D0
delay value (μs)	+ 8	+ 4	+ 2	–	+ 1	–	–	–

ON and CLCCD outputs

These signals are generated in the CCTE and fed to the BMC. When ON is LOW, the BMC/CCD memory interface is in its high impedance OFF-state. When CLCCD is HIGH, this instructs the BMC to clear the CCD memories. Both signals are initiated by the CCT software control with instructions sent via the I^2C bus and the CCT. The instructions are written into specific locations in the page display RAM which are accessed by the CCTE. The page display RAM locations are shown in Table 2.

Table 2 ON and CLCCD locations

address	row 25, column 12							
data bus	D7	D6	D5	D4	D3	D2	D1	D0
bit contents	–	–	CLCCD	–	ON	–	–	–

SCAN

This signal originates in the BMC. When HIGH, SCAN suppresses the output enable ($\overline{OEO}$) to the page display RAM causing the display to be blanked during a scan of the BMC. SCAN acts upon a complete page (excluding the status row and the page header) in the same way as an RFF acts upon a single row.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range (pin 15)	V_{DD}	−0,5 to + 7,0	V
Maximum supply current (pin 15)	I_{DD}	max. ▲	mA
Maximum supply current (pin 14)	I_{SS}	max. ▲	mA
Input voltage range (not F_6)	V_I	−0,5 to (V_{DD}+ 0,5)*	V
Input voltage range (F_6)	V_I	−0,5 to + 12	V
Maximum input current	$\pm I_I$	max. 10	mA
Maximum output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	−25 to + 85	°C
Maximum power dissipation per output	P_O	▲	mW
Maximum power dissipation per package	P_{tot}	▲	W
Storage temperature range	T_{stg}	−55 to + 150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	–	5,5	V
Quiescent supply current at T_{amb} = 25 °C; all inputs at V_{DD} or V_{SS}; TEST and $\overline{OEI}$ at V_{DD}; I_O = 0 mA	I_{DD}	–	–	100	μA
Inputs					
F_6 clock (a.c. coupled)					
D.C. input voltage	V_I	4,0	–	8,0	V
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	3,0	V
Leakage current	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	6	pF

▲ Value under investigation.

* V_{DD}+ 0,5 V not to exceed 8,0 V.

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
$\overline{OEI}$, $\overline{WE}$, A0 to A9, SCAN					
Input voltage LOW	V_{IL}	–	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	–	V
Leakage current at V_{IL}	I_{LI}	–	–	10	μA
Leakage current at V_{IH}	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	5	pF
SANDI (multilevel signal, see Fig. 3)					
LOW tripping level (colour burst blanking)					
Input voltage LOW	V_{IL}	–	–	0,5	V
Input voltage HIGH	V_{IH}	1,0	–	–	V
HIGH tripping level (phase-lock)					
Input voltage LOW	V_{IL}	–	–	3,0	V
Input voltage HIGH	V_{IH}	3,9	–	–	V
Leakage current LOW	I_{LI}	–	–	10	μA
Leakage current INTERMEDIATE	I_{LI}	–	–	10	μA
Leakage current HIGH	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	5	pF
TEST					
Input voltage HIGH	V_{IH}	V_{DD}	–	–	V
Input current HIGH	I_{IH}	–	–	100	μA
Outputs					
$\overline{H}$, PBLF, ON, $\overline{OEO}$, CLCCD					
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at I_{OH} = 100 μA	V_{OH}	2,4	–	–	V
SANDO (multilevel signal, see Fig. 3)					
Output voltage LOW at I_{OL} = 0,5 mA	V_{OL}	–	–	0,2	V
Output voltage INTERMEDIATE at I_{OI} = ± 30 μA	V_{OI}	0,4 V_{DD} −0,5	0,4 V_{DD}	0,4 V_{DD} +0,5	V
Output voltage HIGH at I_{OH} = 30 μA	V_{OH}	V_{DD}−0,3	V_{DD}−0,15	V_{DD}	V
Inputs/outputs D3, D5, D6, D7					
Input voltage LOW	V_{IL}	–	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	–	V
Input leakage current at V_{IL}	I_{LI}	–	–	10	μA
Input leakage current at V_{IH}	I_{LI}	–	–	10	μA
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V

A.C. CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
ADDRESS and DATA to $\overline{WE}$ (Fig. 4)					
Set-up time from address change to start $\overline{WE}$	t_{SA}	50	–	–	ns
Hold time from end $\overline{WE}$ to address change	t_{HA}	0	–	–	ns
Set-up time from data stable to end $\overline{WE}$	t_{SD}	50	–	–	ns
Hold time from end $\overline{WE}$ to data change	t_{HD}	0	–	–	ns
$\overline{OEO}$ to ADDRESS and $\overline{OEI}$ (Figs 5 and 6)					
Delay from address change to negative edge of $\overline{OEO}$	t_{AOL}	–	–	50	ns
Delay from $\overline{OEI}$ to negative edge of $\overline{OEO}$	t_{IOL}	–	–	50	ns
Delay from address change to positive edge of $\overline{OEO}$	t_{AOH}	–	–	50	ns
Delay from $\overline{OEI}$ to positive edge of $\overline{OEO}$	t_{IOH}	–	–	50	ns
DATA to ADDRESS (Fig. 6)					
Address change to data valid	t_{OD}	50	–	–	ns
Hold time data to address change	t_{IZ}	0	–	–	ns
INPUTS and OUTPUTS to F_6 (Fig. 7)					
Set-up time input to F_6	t_{SU}	50	–	–	ns
Hold time input to F_6	t_{IH}	0	–	–	ns
Delay F_6 to output	t_{DO}	–	–	50	ns
Rise and fall times					
Inputs (except SANDI) reference levels 0,8 and 2,0 V	t_r, t_f	–	–	45	ns
Outputs (except SANDO) reference levels 0,4 and 2,4 V	t_r, t_f	–	–	25	ns
SANDI, SANDO (Fig. 3)					
rise time V_{OL} to V_{OI} reference levels 0,4 and 1,4 V	t_r	–	–	250	ns
rise time V_{OI} to V_{OH} reference levels 2,8 and 4,0 V	t_r	–	–	100	ns
fall time V_{OH} to V_{OL} reference levels 4,0 and 0,4 V	t_f	–	–	25	ns
Clock F_6					
Frequency	f	–	6,0	–	MHz

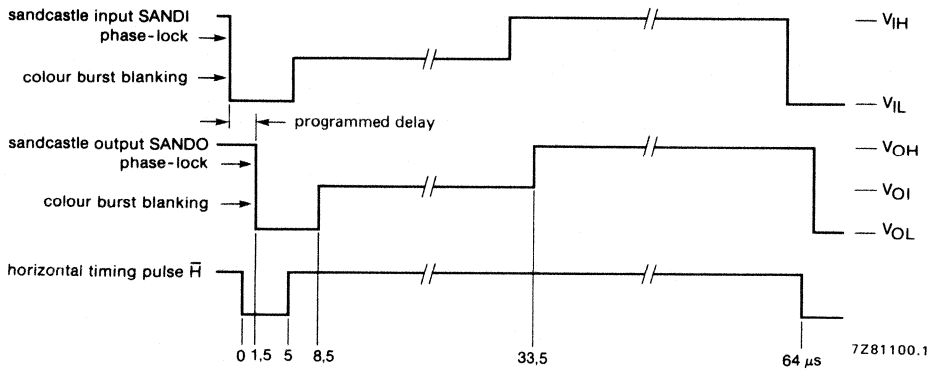


Fig. 3 Timing of sandcastle pulses.

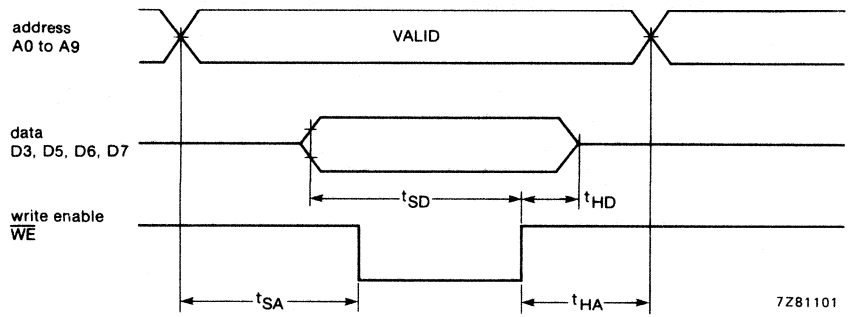


Fig. 4 Address/write enable/data timing.

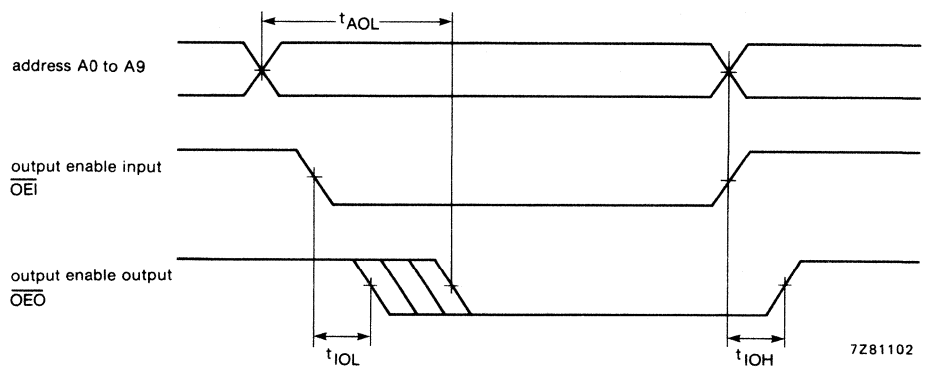


Fig. 5 Address/output enable timing.

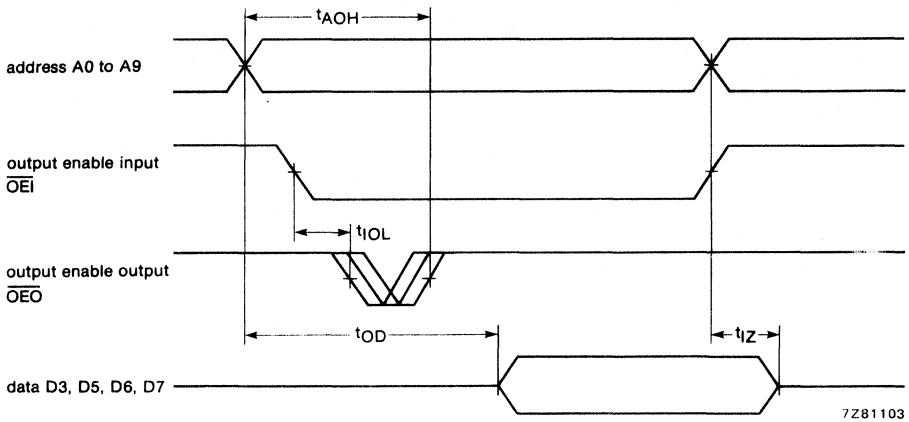


Fig. 6 Address/output enable/data timing.

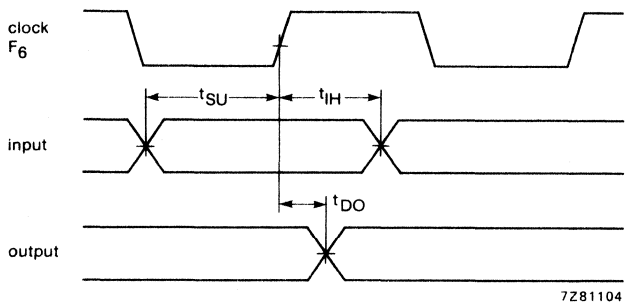


Fig. 7 Timing of inputs and outputs to F_6 clock.

DIGITAL MULTISTANDARD TV DECODER

GENERAL DESCRIPTION

The SAA9050 digital multistandard decoder (DMSD) performs demodulation and decoding of all quadrature modulated colour tv standards, and contains luminance and part-synchronization processing for all tv standards.

Features

- Luminance signal processing for all tv standards (PAL, NTSC, SECAM, B/W)
- Horizontal and vertical sync detection for all standards (525/625 lines)
- Chrominance signal processing for all quadrature amplitude modulated colour-carrier signals (PAL-B, G, H, I, M, N; NTSC-M)
- Requires only one crystal (24,576 MHz), which may also be used for audio processing
- Functions, settings and adjustments programmable under software control via the I^2C bus
- User-programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Multiplexed output format selectable (U, V, Y, Y, Y, Y)
- Parallel (nibble) output format selectable (Y/U6, U5, V6, V5; U4, U3, V4, V3; U2, U1, V2, V1; U0, CS, V0, X)
- SECAM interface
- Cross-colour reduction by chrominance comb-filtering (NTSC)
- Comb-filters adapt automatically to line frequency
- Internal overflow protection
- Selectable chrominance amplitude control protection for non-standard signals
- Programmable horizontal position of the active video signal in each line
- Indirect I^2C control capability to select input from one of four video sources
- Indirect I^2C control capability for automatic flesh-tone correction
- Wide range hue control
- Internal coincidence detection

PACKAGE OUTLINE

40-lead DIL; plastic with internal heat spreader (SOT-129).

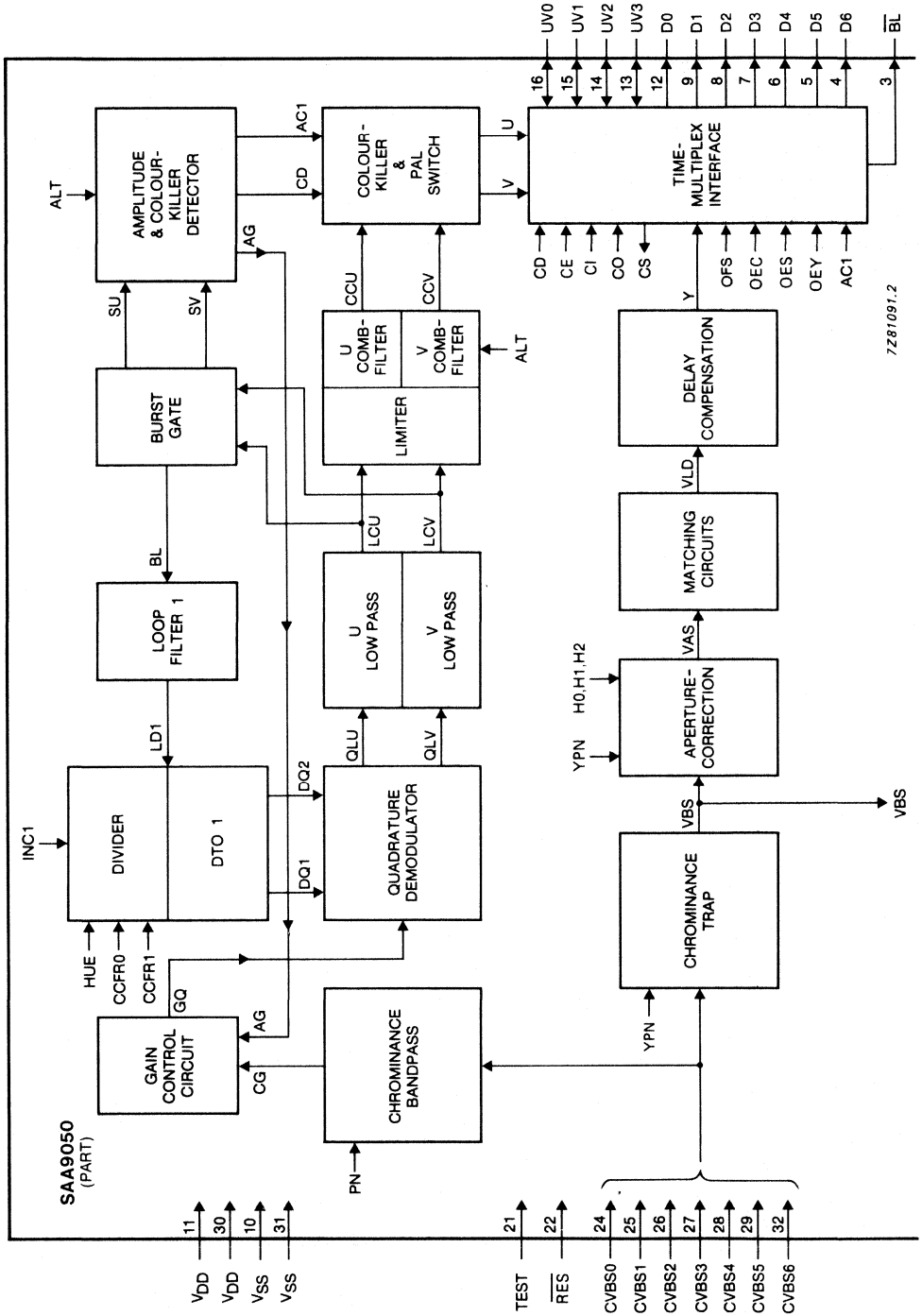


Fig. 1a Block diagram; continued in Fig. 1b.

DEVELOPMENT DATA

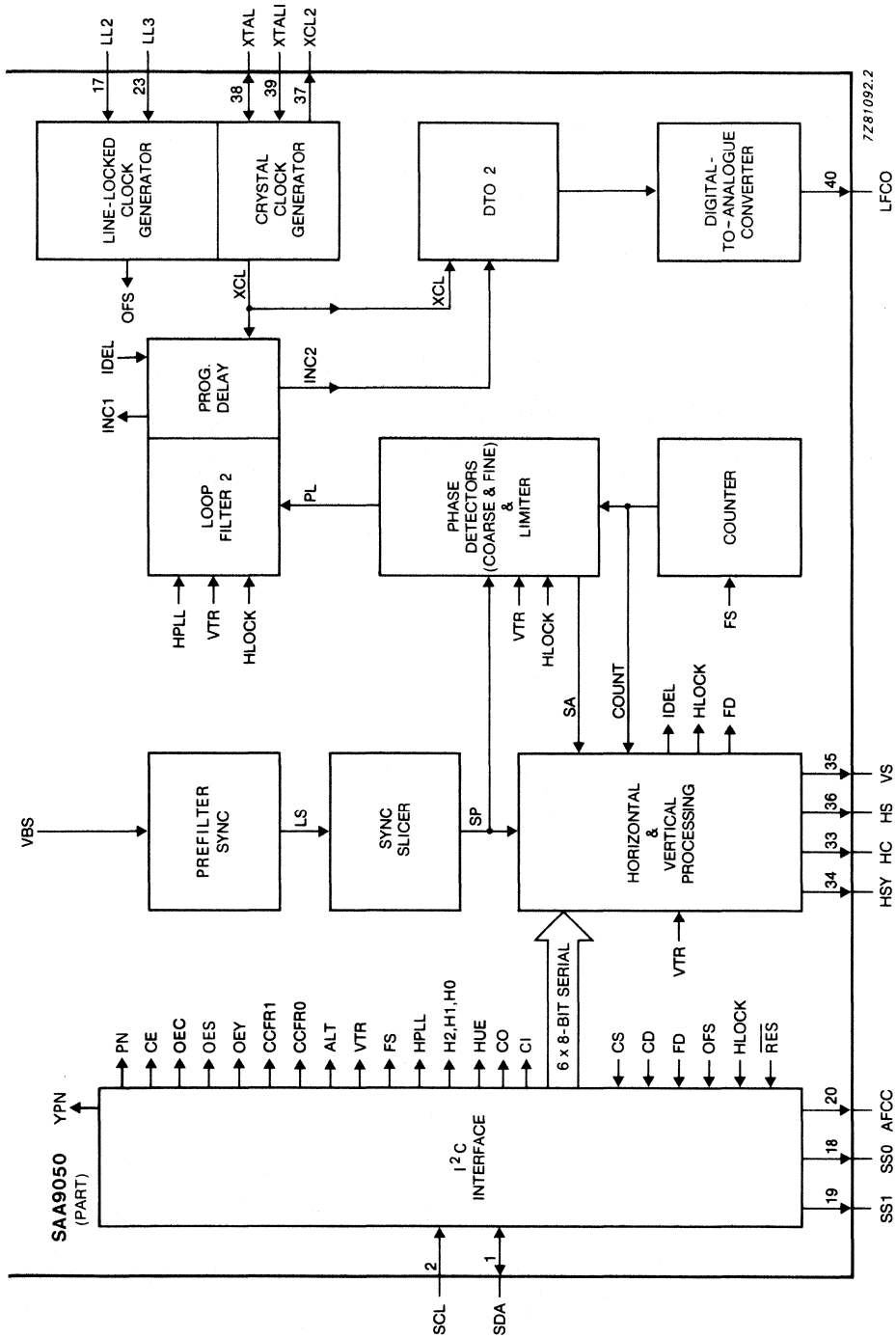


Fig. 1b Block diagram; from Fig. 1a.

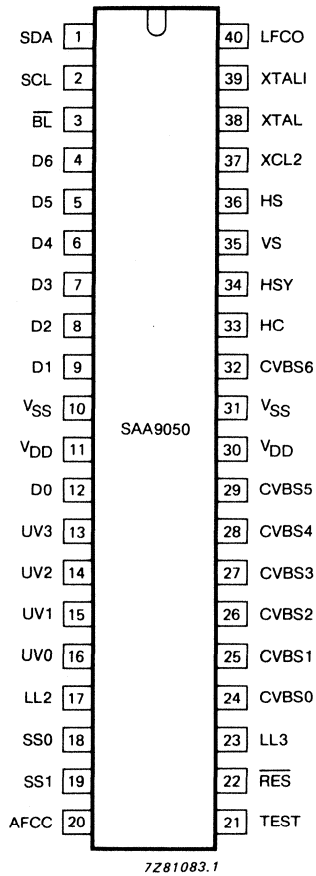


Fig. 2 Pinning diagram.

1	SDA	I²C bus serial data input/output
2	SCL	I²C bus serial clock input
3	$\overline{BL}$	Blanking output to indicate the active video and line blanking periods. Active LOW
4	D6(MSB)	Colour difference outputs (U, V) with positive polarity plus luminance (Y) outputs, transmitted in a 20,25 MHz data stream with U, V, Y, Y, Y, Y serial format. The chrominance data is two's complement and luminance is unipolar. The transmission is synchronized externally by $\overline{BL}$. The delay from CVBS input to D0-D6 output is 55 LL3 + 2 LL2 clocks in multiplexed format, and 58 LL3 clocks in semi-parallel format. Luminance only is transmitted when LL2 = LL3 = 13,5 MHz
5	D5	
6	D4	
7	D3	
8	D2	
9	D1	
12	D0(LSB)	
10; 31	V_{SS}	Ground (0 V)
11; 30	V_{DD}	Positive supply voltage (+ 5 V)

DEVELOPMENT DATA

13 14 15 16	UV3 UV2 UV1 UV0	SECAM colour difference signal input/PAL or NTSC colour difference signal output. In the input mode, SECAM U, V and CS (colour-SECAM) signals are received from the SECAM decoder. The output mode occurs when LL2 = LL3, then U and V signals are transmitted at 13,5 MHz. Input and output data formats are two's complement with positive polarity
17	LL2	20,25 MHz line-locked clock input used for multiplexed UVY format. LL2 frequency is 13,5 MHz for semi-parallel format
18 19	SS0 SS1	Source select output signals, set via the I^2C bus to control the input switch (e.g. TDA9045)
20	AFCC	Automatic flesh-tone correction control activated via the I^2C bus to control the colour track circuit of NTSC systems
21	TEST	Test input, when HIGH enables the scan-test mode
22	$\overline{\text{RES}}$	Reset input, active LOW, causes control registers 1 and 2 to be reset during the reset phase. The minimum LOW period of $\overline{\text{RES}}$ is 120 LL3 clocks
23	LL3	13,5 MHz line-locked system clock
24 25 26 27 28 29 32	CVBS0(LSB) CVBS1 CVBS2 CVBS3 CVBS4 CVBS5 CVBS6(MSB)	Digitized composite video, blanking and synchronization signal containing luminance, chrominance and all synchronization information. Two's complement format
33	HC	Horizontal clamping signal that indicates the black-level position before analogue-to-digital conversion. The start and stop time is programmable via the I^2C bus in the range of −9,4 to + 9,5 μs in steps of 74 ns
34	HSY	Horizontal synchronization signal that indicates the sync pulse position before analogue-to-digital conversion. The start and stop time is programmable via the I^2C bus in the range of −14,2 to + 4,7 μs in steps of 74 ns
35	VS	Vertical synchronization output that indicates the vertical position of the picture for 50 or 60 Hz field frequency
36	HS	Horizontal synchronization pulse output. Duration = 16 LL3 clocks. Synchronizes the horizontal position of the active video signal in each line and is programmable via the I^2C bus in the range of −32 to + 32 μs in steps of 300 ns
37	XCL2	Clock output at half the crystal clock frequency (12,288 MHz). In phase with XTAL (pin 38)
38	XTAL	Crystal input/output. Input to the internal clock generator (from an external oscillator, when used), or output of the inverting amplifier to an external crystal (24,576 MHz)
39	XTALI	Input to the inverting amplifier from the external crystal (24,576 MHz); connected to ground when an external oscillator is used
40	LFCO	Line frequency control. Analogue output representing a multiple of the line frequency (6,75 MHz) with a 4-bit resolution, the phase of which is compared with the system clock by the clock generator circuit (SAA9057)

FUNCTIONAL DESCRIPTION (Fig. 1)

The DMSD performs demodulation and decoding for PAL-B, G, H, I, M, N, NTSC-M tv standards and contains luminance and parts of the synchronization processing for all PAL, NTSC and SECAM tv standards. All of the controllable functions of the DMSD, user controls as well as factory adjustments, are accessed via the two-line, bidirectional I^2C bus, so enhancing the adaptability of the digital tv concept.

Operation is based on a line-locked sampling frequency of 13,5 MHz, making the system fully adaptable to all line frequencies and requiring only one crystal for all tv standards.

Output formats (Fig. 3)

There are two output formats available via the time-multiplex interface that are controlled by the LL2 and LL3 clocks. The interface can also be used to incorporate an optional SECAM decoder.

LL2 = 20,25 MHz LL3 = 13,5 MHz	A multiplexed output data stream in the format U, V, Y, Y, Y, Y is transmitted from D0-D6 at a sample rate of 20,25 MHz, giving full compatibility with memory-based feature tv concepts.
LL2 = LL3 = 13,5 MHz	The Y and U, V signals are transmitted separately, the Y signals in a data stream of 13,5 MHz from D0-D6 and the U, V signals in a nibble format from UV0-UV3. The SECAM-decoder option also uses this clock mode.

Processing

The digital CVBS input is separated into its luminance (VBS) and chrominance (CG) parts by chrominance trap and chrominance bandpass circuits, which can be switched by the standard identification signals (PN/YPN) according to the detected PN centre frequency (3,58 or 4,43 MHz). The range of binary values for input/output signals are shown in Fig. 4.

The separated luminance signal (VBS) is passed to an aperture-correction circuit that has programmable horizontal peaking. The corrected signal (VAS) is then matched to the full-scale of the appropriate word-width and limited to prevent overflow. The signal (now VLD) undergoes delay compensation to equalize the delays of the luminance and chrominance channels. Differences of delay compensation requirements in PAL and NTSC modes are catered for when switching is performed by the standard identification signal (PN).

In the chrominance channel, the amplitude of the chrominance signal (CG) is controlled to give a signal with constant burst amplitude (CQ). The control signal (AG) for gain-control is derived in the amplitude and colour-killer detection circuit. If there is a non-standard ratio between burst and chrominance amplitudes (−17% in the NTSC mode), an automatic colour-levelling circuit takes the function of amplitude detection to ensure correct chrominance amplitude and to avoid overflow and limiter defects.

Demodulation of the square-modulated chrominance signal (CQ) is performed by the quadrature demodulator which gives the baseband colour difference signals (LCU and LCV). The comb-filter stage then separates remaining luminance components from these signals and (for PAL) corrects their phase to give the signals CCU and CCV. The number of delay elements required in the comb-filter is minimized by the use of a reduced, blanked, line-locked clock. The comb-filter structure is changeable under the control of the standard-identification signal (ALT).
The colour-killer, under the control of amplitude and colour-killer detection (AC1 and CD), removes incoming signals that do not comply with the chosen standard. The PAL switch restores the correct phasing of the V signal when in PAL mode.

Regeneration of the colour carrier frequency is done by the phase-locked-loop comprising quadrature modulator, low pass filter, burst gate, loop filter 1 and discrete time oscillator (DTO 1). The latter is controlled by standard identification signals (CCFR0, CCFR1) and a signal (HUE) that influences the demodulation phase of the chrominance signal.

In the synchronization circuit, prefilter synchronization is implemented to normalize sync slopes. A sync-slicer provides the detected sync pulses (SP) to the H, V processing and phase detector stages.

The H and V processing comprises part of a PLL circuit for the regeneration of the horizontal synchronization (HS) and an adaptive filter for the detection of vertical sync (VS), see Fig. 5. The H, V processing also generates the coincidence signal (HLOCK) which controls the mute function, and a standard identification signal (FD) which identifies nominal 625 or 525 lines per picture.

The phase detectors that receive the SP signal, also part of the PLL, control the generation of the line-locked clock (PL). Loop filter 2, which has a changeable bandwidth controlled by the video recorder/tv time constant signal (VTR), generates two increment signals (INC1 and INC2) with different delays. INC2 is programmable via the increment-delay signal (IDEL). INC1 corrects the regenerated subcarrier frequency at DTO 1 and INC2 performs phase incrementing of DTO 2. The crystal clock generator provides a stable 24,576 MHz clock input to DTO 2 which in turn supplies the 4-bit DAC with a digital control signal of 432 or 429-times the line frequency. The analogue output (LFCO) from the DAC goes to the clock generator (SAA9057).

The output signals D0-D6 can be multiplexed under the control of an internal blanking and format signal. It is a time-multiplex interface that also provides an external blanking and format signal ($\overline{BL}$).

For real-time inputs to the DMSD, the line-locked clocks LL2 and LL3 are required as well as the digital CVBS signal (CVBS0-CVBS6). As an option, a nibble-format colour difference input to UV0-UV3 can be used for interfacing a digital SECAM decoder. Under the control of the I^2C bus this interface can be switched into an output mode for outward transmission of colour difference signals U, V (LL2 = LL3 = 13,5 MHz).

PAL-B, G, H, I and NTSC detection

The current version of the DSMD is unable to distinguish between the PAL-B, G, H, I and NTSC 4,4 standards, if the NTSC 4,4 standard is chosen. To overcome this problem in automatic standard routine it is necessary to:

- check the NTSC 4,4 standard before the PAL-B, G, H and I standards

or

- cross check the PAL-B, G, H and I, if the NTSC 4,4 standard is detected.

FUNCTIONAL DESCRIPTION (continued)

I²C bus interface

The following control signals are received via the I²C bus (SDA and SCL) and the I²C bus interface:

- standard identification signals (CCFR0, CCFR1, ALT, FS, CE, YPN)
- time constant VTR/TV (VTR)
- hue control (HUE)
- delay programming of the horizontal signals (HS, HC, HSY)
- increment-delay (IDEL)
- aperture-correction control (H0, H1, H2)
- fixed clock generation command (HPLL)
- internal colour ON/OFF (CO)
- internal colour forced ON for test purposes (CI)
- sync output enable (OES)
- luminance output enable (OEY)
- chrominance output enable (OEC)
- source select signal (SS0, SS1)
- automatic flesh-tone control (AFCC)

Signals transmitted from the DMSD via the I²C bus are:

- standard identification signals (FD, CS)
- colour-killer status signal (CD)
- coincidence information (HLOCK)
- selected output format indicator (OFS)
- power-on-reset of DMSD (PONRES)

Time-multiplex interface (Fig. 6)

The UV0-UV3 signals from the SECAM decoder are received in a 13,5 MHz data stream in the following format:

input signal	sample 0	1	2	3	0	1	2	3
UV3	U6	U4	U2	U0	repeating			
UV2	U5	U3	U1	CS	repeating			
UV1	V6	V4	V2	V0	repeating			
UV0	V5	V3	V1	X	repeating			

The signal CS is an information bit from the SECAM decoder:

CS = logic 0 indicates colour not detected in SECAM
CS = logic 1 indicates colour detected in SECAM
X = don't care

This bit is latched in the DMSD. The CS bit is transmitted to control circuits via the I²C bus.

Commands that control the outputs of the time-multiplex interface are OES, OEY, OEC, CO and CI which are received via the I^2C bus, and CD which is detected in the DMSD. The start condition of OES, OEY, OEC, CO and CI after initialization is always zero. The outputs are controlled as follows:

OES	OEY	OEC	outputs	output status
0 1	X X	X X	HS and VS	HIGH-impedance OFF-state active
X X	0 1	X X	D0-D6 and $\overline{BL}$	HIGH-impedance OFF-state active
X X	X X	0 1	UV0-UV3	HIGH-impedance OFF-state active

CO	CI	CD	outputs	output status
0	X	X	UV0-UV3 or UV samples of 'multiplexed output format (U, V, Y, Y, Y, Y)'	colour OFF (zero)
1 1	0 0	0 1		colour OFF } controlled colour ON } by CD
1	1	X		colour forced ON

X = don't care.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

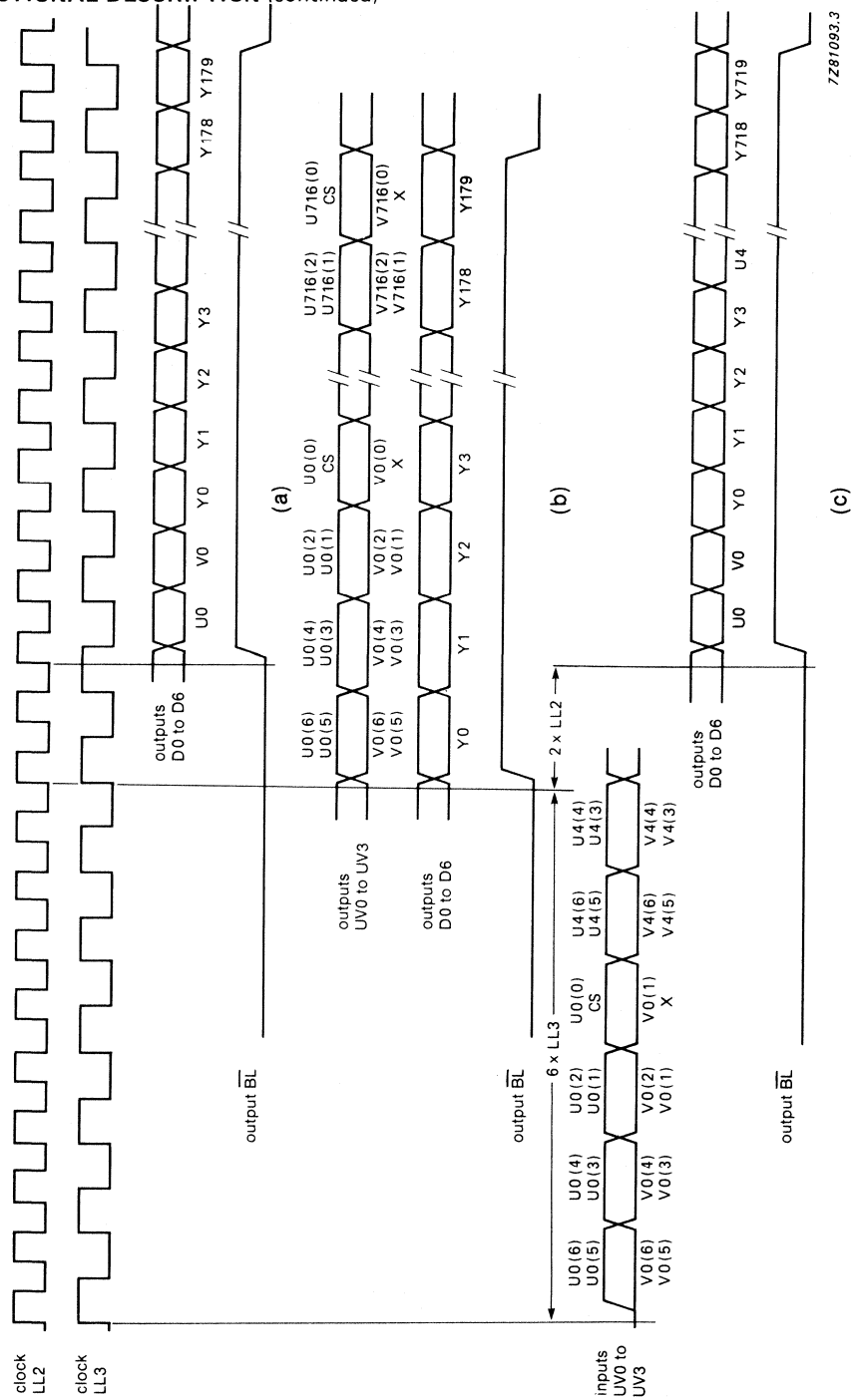
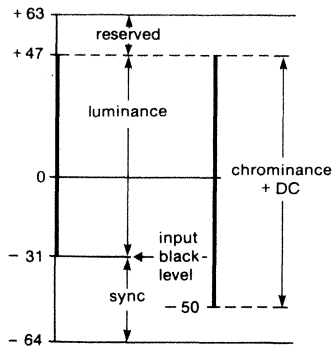
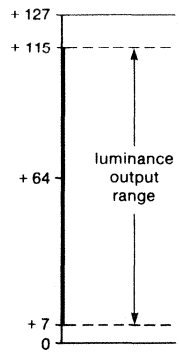


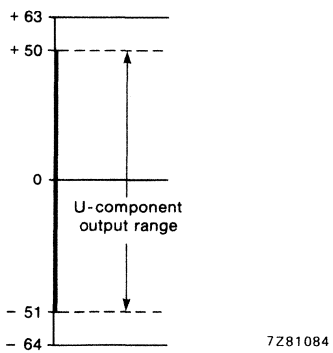
Fig. 3 Correlation of signals: (a) serial mode; (b) parallel (nibble) mode when LL2 = LL3 = 13,5 MHz; (c) serial mode in which SECAM chrominance signals (received via UV0-UV3 from a SECAM decoder) are combined with DMSD luminance signals.



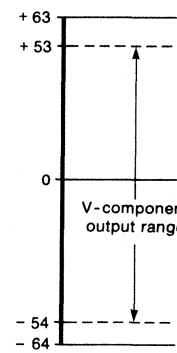
(a) CVBS0 to CVBS6 input range with 75% colour bar.



(b) Y output range.



(c) U output range (B–Y).



(d) V output range (R–Y).

Fig. 4 Diagram showing input/output range of the DMSD (levels are given in binary values).

FUNCTIONAL DESCRIPTION (continued)

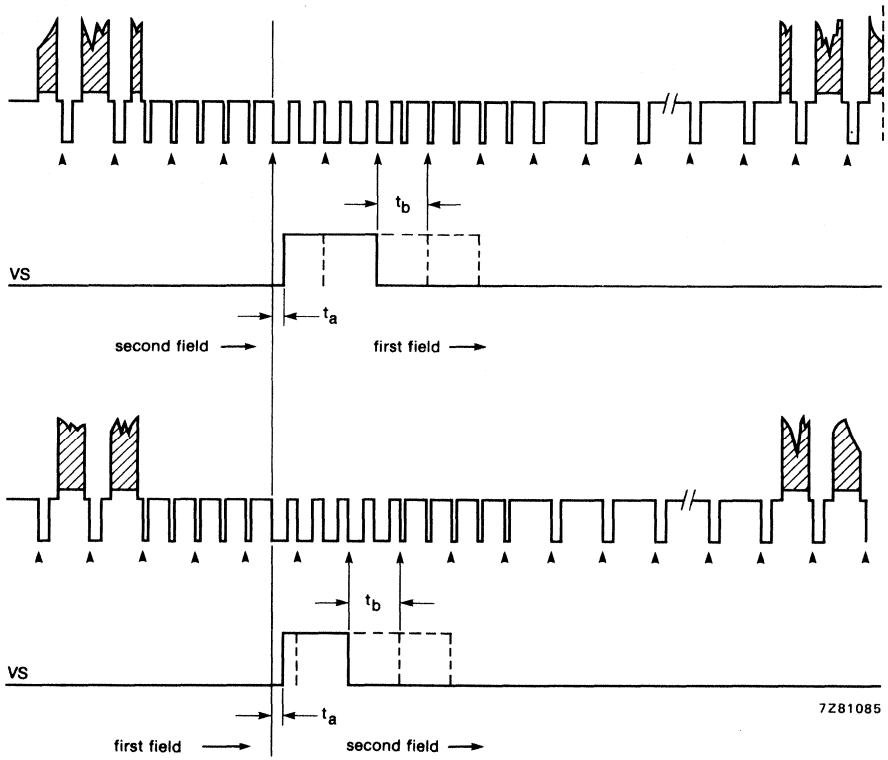


Fig. 5 Vertical sync (VS): time t_a is approximately 24 μs; time t_b = 64 μs (the minimum vertical sync pulse length is 75 μs).

DEVELOPMENT DATA

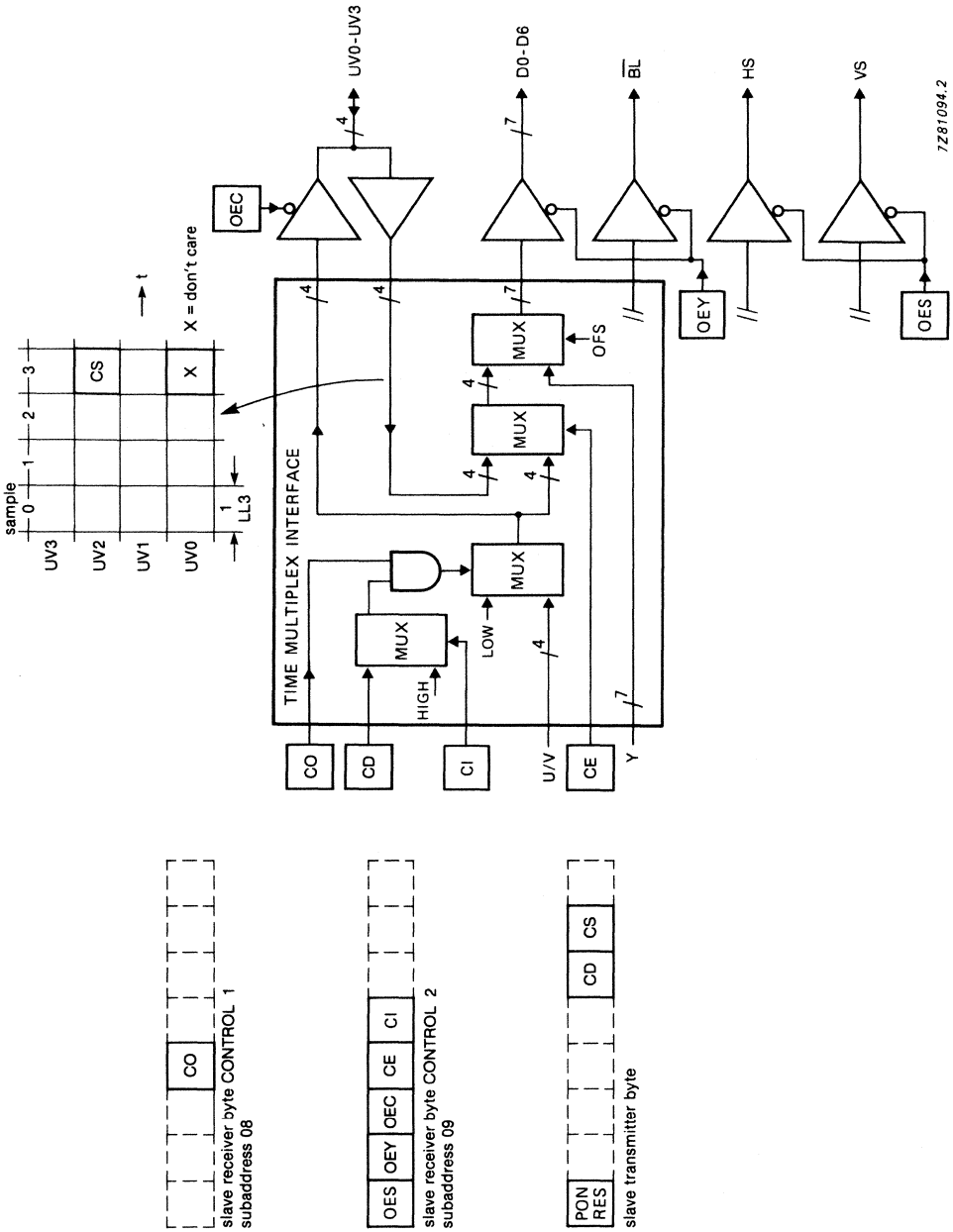


Fig. 6 Schematic diagram of control signals at the time-multiplex interface and output stages.

SLAVE RECEIVER ORGANIZATION

Slave address and receiver format

Slave address for the digital multistandard decoder is:

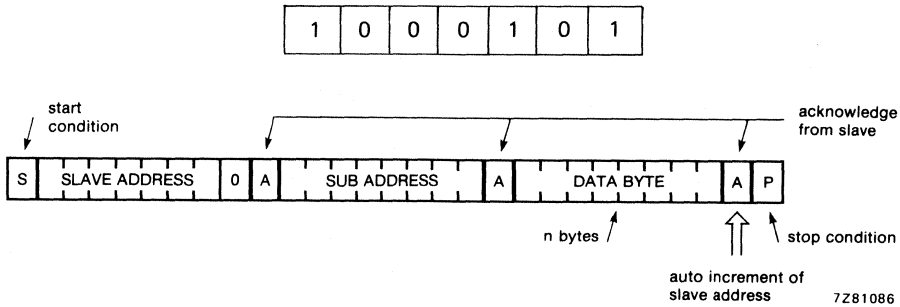


Fig. 7 Slave receiver format.

Subaddress byte and data byte formats

register function	sub address	data byte D7	D6	D5	D4	D3	D2	D1	D0
Increment delay IDEL	00	A07	A06	A05	A04	A03	A02	A01	A00
Horizontal sync									
HSY start time	01	A17	A16	A15	A14	A13	A12	A11	A10
HSY stop time	02	A27	A26	A25	A24	A23	A22	A21	A20
Horizontal clamp									
HC start time	03	A37	A36	A35	A34	A33	A32	A31	A30
HC stop time	04	A47	A46	A45	A44	A43	A42	A41	A40
Horiz. sync after PHI1									
HS start time	05	A57	A56	A55	A54	A53	A52	A51	A50
Horizontal peaking	06	X	X	X	X	X	H2	H1	H0
Hue control	07	A77	A76	A75	A74	A73	A72	A71	A70
Control 1	08	HPLL	FS	VTR	CO	ALT	YPN	CCFR1	CCFR0
Control 2	09	OES	OEY	OEC	CE	CI	AFCC	SS1	SS0
Reserved	0A to 0F	X	X	X	X	X	X	X	X

Notes

The subaddress is automatically incremented. This enables quick initialization by the I^2C bus controller within one transmission.

All eight bits of the subaddress have to be decoded by the device.

The subaddresses shown are acknowledged by the device. Subaddresses 10 to 1F (reserved for the SECAM decoder SAA9055) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.

X = don't care.

After power-on-reset the control registers 1 and 2 (subaddresses 08 and 09) are set to logic 0, all other registers are undefined.

The least significant bit of an analogue control or alignment register is defined as AX0.

Increment delay control IDEL (application dependent)

decimal multiplier	delay time (step size = 2/13,5 MHz = 148 ns)	control bits* A07	A06	A05	A04	A03	A02	A01	A00
−1	−148 ns (min. value)	1	1	1	1	1	1	1	1
to									
−110	−16,3 μs (outside available range)	1	0	0	1	0	0	1	0
−111	−16,44 μs	1	0	0	1	0	0	0	1
to									
−214	−31,7 μs (max. value if FS = logic 1)	0	0	1	0	1	0	1	0
−215	−31,85 μs (outside central counter if FS = logic 1)**	0	0	1	0	1	0	0	1
−216	−32 μs (max. value if FS = logic 0)	0	0	1	0	1	0	0	0
−217	−32,148 μs (outside central counter if FS = logic 0)**	0	0	1	0	0	1	1	1
to									
−256	−37,9 μs (outside central counter)**	0	0	0	0	0	0	0	0

* A sign bit, designated A08 and internally set to HIGH, indicates values are always negative.

** The horizontal PLL does not function in this condition: the system clock frequency is set to a value fixed by the last update and is within ± 7,1% of the nominal frequency.

Horizontal sync HSY start time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A17	A16	A15	A14	A13	A12	A11	A10
+ 191	−14,2 μs (max. negative value)	1	0	1	1	1	1	1	1
to									
+ 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0,074 μs	1	1	1	1	1	1	1	1
to									
−64	+ 4,7 μs (max. positive value)	1	1	0	0	0	0	0	0

DEVELOPMENT DATA

SLAVE RECEIVER ORGANIZATION (continued)

Horizontal sync HSY stop time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A27	A26	A25	A24	A23	A22	A21	A20
+ 191	−14,2 μs (max. negative value)	1	0	1	1	1	1	1	1
to									
+ 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0,074 μs	1	1	1	1	1	1	1	1
to									
−64	+ 4,7 μs (max. positive value)	1	1	0	0	0	0	0	0

Horizontal clamp HC start time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A37	A36	A35	A34	A33	A32	A31	A30
+ 127	−9,4 μs (max. negative value)	0	1	1	1	1	1	1	1
to									
+ 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0,074 μs	1	1	1	1	1	1	1	1
to									
−128	+ 9,5 μs (max. positive value)	1	0	0	0	0	0	0	0

Horizontal clamp HC stop time (application dependent)

decimal multiplier	delay time (step size = 1/13,5 MHz = 74 ns)	control bits A47	A46	A45	A44	A43	A42	A41	A40
+ 127	−9,4 μs (max. negative value)	0	1	1	1	1	1	1	1
to									
+ 1	−0,074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1	+ 0,074 μs	1	1	1	1	1	1	1	1
to									
−128	+ 9,5 μs (max. positive value)	1	0	0	0	0	0	0	0

Horizontal sync after PHI1 HS start time (application dependent)

50 Hz; 625-line mode and FS = logic 0

decimal multiplier	delay time (step size = 4/13,5 MHz = 296 ns)	control bits A57	A56	A55	A54	A53	A52	A51	A50
+ 127 to + 109	forbidden; outside available central counter range	0	1	1	1	1	1	1	1
		0	1	1	0	1	1	0	1
+ 108 to + 1	−32 μs (max. neg. value)	0	1	1	0	1	1	0	0
	−0,296 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −107	+ 0,296 μs	1	1	1	1	1	1	1	1
	+ 31,7 μs (max. pos. value)	1	0	0	1	0	1	0	1
−108 to −128	forbidden; outside available central counter range	1	0	0	1	0	1	0	0
		1	0	0	0	0	0	0	0

60 Hz; 525-line mode and FS = logic 1

decimal multiplier	delay time (step size = 4/13,5 MHz = 296 ns)	control bits A57	A56	A55	A54	A53	A52	A51	A50
+ 127 to + 107	forbidden; outside available central counter range	0	1	1	1	1	1	1	1
		0	1	1	0	1	0	1	1
+ 106 to + 1	−31,8 μs (max. neg. value)	0	1	1	0	1	1	0	0
	−0,294 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −107	+ 0,294 μs	1	1	1	1	1	1	1	1
	+ 31,5 μs (max. pos. value)	1	0	0	1	0	1	0	1
−108 to −128	forbidden; outside available central counter range	1	0	0	1	0	1	0	0
		1	0	0	0	0	0	0	0

DEVELOPMENT DATA

SLAVE RECEIVER ORGANIZATION (continued)

Horizontal peaking H2, H1, H0, PN (user dependent) (see Fig. 13)

aperture factor (af)	control bits H2	H1	H0	YPN
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

Chrominance trap select (system mode dependent)

YPN	chrominance trap
0	4,43 MHz
1	3,58 MHz

Hue phase (user dependent)

hue phase	control bits A77	A76	A75	A74	A73	A72	A71	A70
+ 178,6 deg to	1	1	1	1	1	1	1	1
0 deg to	1	0	0	0	0	0	0	0
−180 deg	0	0	0	0	0	0	0	0

Step size per least-significant bit (A70) = 1,4 deg.

Reference point for positive colour difference signals = 0 deg.

The hue phase may be shifted ± 180 deg from the reference point using bit A77, the colour difference signals are then switched from normal positive to negative polarity.

Horizontal clock PLL (application dependent)

function	HPLL control bit
horizontal clock PLL open, horizontal frequency fixed	1
horizontal clock PLL closed	0

Field frequency select (system mode dependent)

function	FS control bit
60 Hz; 525-line mode	1
50 Hz; 625-line mode	0

VTR/TV mode select (system mode dependent)

function	VTR control bit
VTR mode	1
TV mode	0

DEVELOPMENT DATA

SLAVE RECEIVER ORGANIZATION (continued)

Colour-on control (system mode dependent)

function	CO control bit
colour ON	1
colour OFF (all colour output samples zero)	0

Alternate/non-alternate mode (system mode dependent)

function	ALT control bit
alternate mode (PAL)	1
non-alternate mode (NTSC)	0

Colour carrier frequency control (system mode dependent)

colour carrier frequency	control bits CCFR1	CCFR0
4 433 618,75 Hz (PAL-B, G, H, I; NTSC-4,43)	0	0
3 575 611,49 Hz (PAL-M)	0	1
3 582 056,25 Hz (PAL-N)	1	0
3 579 545 Hz (NTSC-M)	1	1

Colour decoding table

colour standard	control bits FS				ALT		CCFR1	CCFR0
PAL-B, G, H, I		0			1		0	0
NTSC-4,43; 50 Hz		0			0		0	0
NTSC-4,43; 60 Hz		1			0		0	0
PAL-M	HPLL	1	VTR	CO	1	YPN	0	1
PAL-N		0			1		1	0
NTSC-M		1			0		1	1

Sync output enable (system mode dependent)

function	control bit OES
outputs HS and VS active	1
outputs HS and VS HIGH-Z	0

Y output enable (system mode dependent)

function	control bit OEY
outputs D0-D6 and $\overline{BL}$ active	1
outputs D0-D6 and $\overline{BL}$ HIGH-Z	0

Chrominance output enable (system mode dependent)

function	control bit OEC
outputs UV0-UV3 active; chrominance signal when CD = logic 1; zero signal when CD = logic 0	1
outputs UV0-UV3 HIGH-Z	0

External colour select (system mode dependent)

function	control bit CE
select external colour channel; serial format via inputs UV0-UV3	1
select internal colour channel	0

Internal colour forced ON/OFF (for test or service requirements only)

function	control bit CI
colour forced ON if CO = logic 1 (CD = X) colour OFF if CO = logic 0 (CD = X)	1
colour OFF if CO = logic 0 (CD = X) colour controlled by CD if CO = logic 1	0

X = don't care

Automatic flesh-tone corrector (colour track) (user dependent)

function	AFCC control bit
colour track ON	1
colour track OFF	0

Source select (system mode dependent)

function	control bits SS1	SS0
select input CVBS0	0	0
select input CVBS1*	0	1
select input CVBS2	1	0
select input CVBS3	1	1

* not allowed when operating with TDA9045.

DEVELOPMENT DATA

SLAVE TRANSMITTER ORGANIZATION

Slave transmitter format

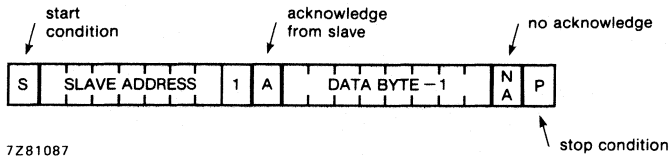


Fig. 8 Slave transmitter format (a general call address is not acknowledged).

The format of data byte 1 is:

PONRES	HLOCK	OFS	FD	0	CD	CS	0

PONRES — Status bit for power-on-reset ($\overline{RES}$) and after a power failure:

logic 1 after the first power-on-reset and after a power failure. Also set to logic 1 after a severe voltage dip that may have disturbed slave receiver data in the PAL/NTSC decoder (SAA9050). PONRES sets all data bits of control registers 1 and 2 to zero.

logic 0 after a successful read of the PAL/NTSC decoder status byte.

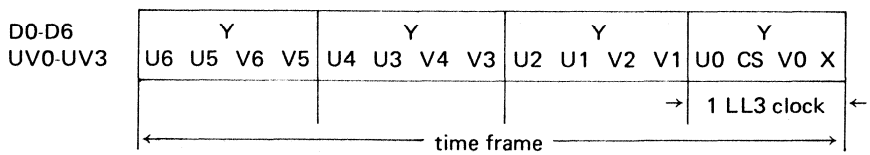
HLOCK — Status bit for horizontal frequency lock (transmitter identification, stop or mute bit):

logic 1 if horizontal frequency is not locked (no transmitter available);

logic 0 if horizontal frequency is locked (transmitter received).

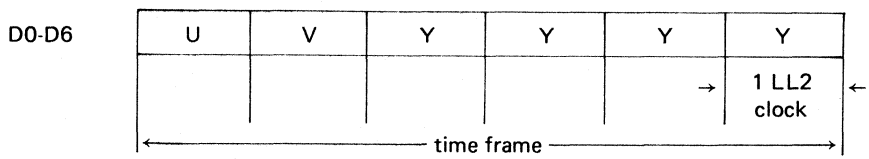
OFS — Status bit for output format selection:

logic 1 when quasi-parallel format is selected:



X = don't care

logic 0 when serial output format is selected:



FD — Detected field frequency status bit:
logic 1 when received signal has 60 Hz sync pulses;
logic 0 when received signal has 50 Hz sync pulses.

CD — PAL/NTSC colour-detected status bit:
logic 1 when PAL/NTSC colour signal is detected;
logic 0 when no PAL/NTSC colour signal is detected.

CS — SECAM colour-detected status bit:
logic 1 when SECAM colour signal is detected;
logic 0 when no SECAM colour signal is detected.

PROGRAMMING IDEL, HSY, HC and HS

These variables are programmed via data words on the I²C bus. In the following examples decreasing numbers correspond to increasing time.

IDEL (Fig. 9)

The IDEL data word compensates for the time delays in data processing between loop filter 2 and the quadrature demodulator and includes internal and external (system) signal paths. The internal path from loop filter 2 takes INC1 to the divider and DTO 1. This delay (t_{REF}) corrects the relationship between the subcarrier frequency and the line frequency. The external path accounts for the following time delays:

t_{IDEL}	programmable delay time	in LL3 periods
t_a	processing time of DTO 2 and the D-A converter	
t_b	chrominance bandpass and gain control stage delay times	
t_{CGC}	clock generator circuit delay time	
t_{ADC}	analogue-to-digital converter delay time	
t_{SRC}	sample-rate converter delay time	
t_{SECAM}	SECAM colour decoder delay time	

As the delays t_a and t_b are known constants, t_{IDEL} is programmed as follows:

$t_{IDEL} = -115 - 0{,}5\,(99 - t_{CGC} - t_{ADC} - t_{SRC}^{*} - t_{SECAM}^{*})$

Programming range: −115 to −214/−216.

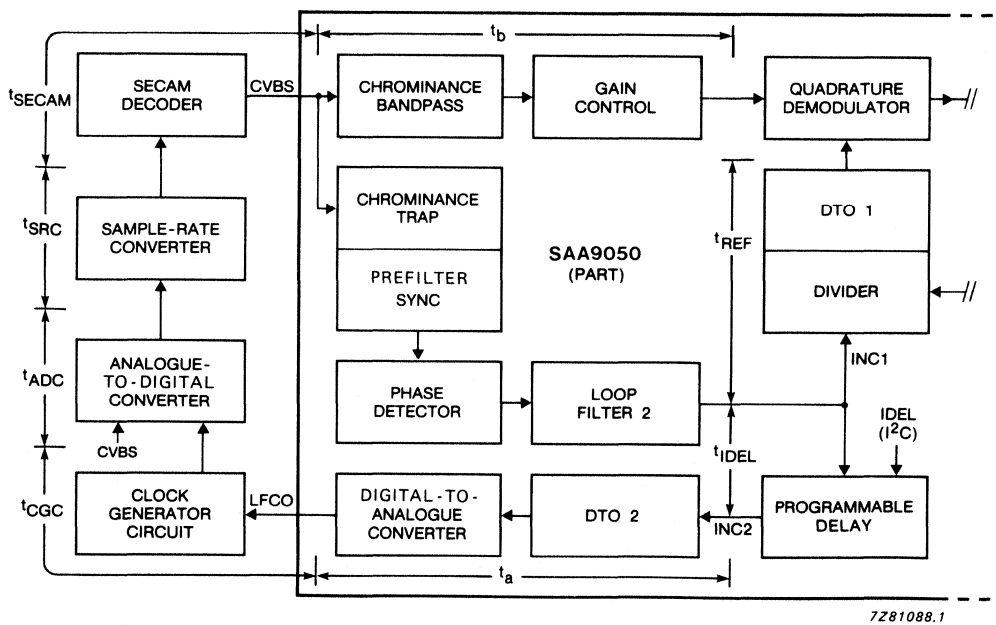


Fig. 9 Compensation of delay times by increment delay control IDEL.

* When included in the application.

PROGRAMMING IDEL, HSY, HC and HS (continued)

HSY (Fig. 10)

Referring to Fig. 10 points (1), (2) and periods a, b:

HSY start time $= T_{(1)-(2)} + 42 - a$ LL3 clock periods

HSY stop time $= T_{(1)-(2)} + 42 - b$ LL3 clock periods

Programming range of HSY start/stop time: + 191 to −64 LL3 clock periods.

HC (Fig. 10)

Referring to Fig. 10 points (1), (2) and periods c, d:

HC start time $= T_{(1)-(2)} + 42 - c$ LL3 clock periods

HC stop time $= T_{(1)-(2)} + 42 - d$ LL3 clock periods

Programming range of HC start/stop time: + 127 to −128 LL3 clock periods.

HS (Fig. 10)

The reference positions of HS in PAL and NTSC modes are shown in Fig. 10 at points (4) and (5) respectively. To move the HS pulse to the centre of blanking pulse $\overline{BL}$ the following equation is used:

$$\text{HS (NTSC)} : \frac{-[\text{position of HS relative to point (3)} + 17\ \text{LL3}]}{4\ \text{LL3}}$$

$$\text{HS (PAL)} : \frac{-[\text{position of HS relative to point (3)} + 14\ \text{LL3}]}{4\ \text{LL3}}$$

In the example given in Fig. 10:

HS (NTSC) : $-[55 + 17]/4 = -18$ (decimal) = 1110 1110 (binary)

HS (PAL) : $-[62 + 14]/4 = -19$ (decimal) = 1110 1101 (binary)

DEVELOPMENT DATA

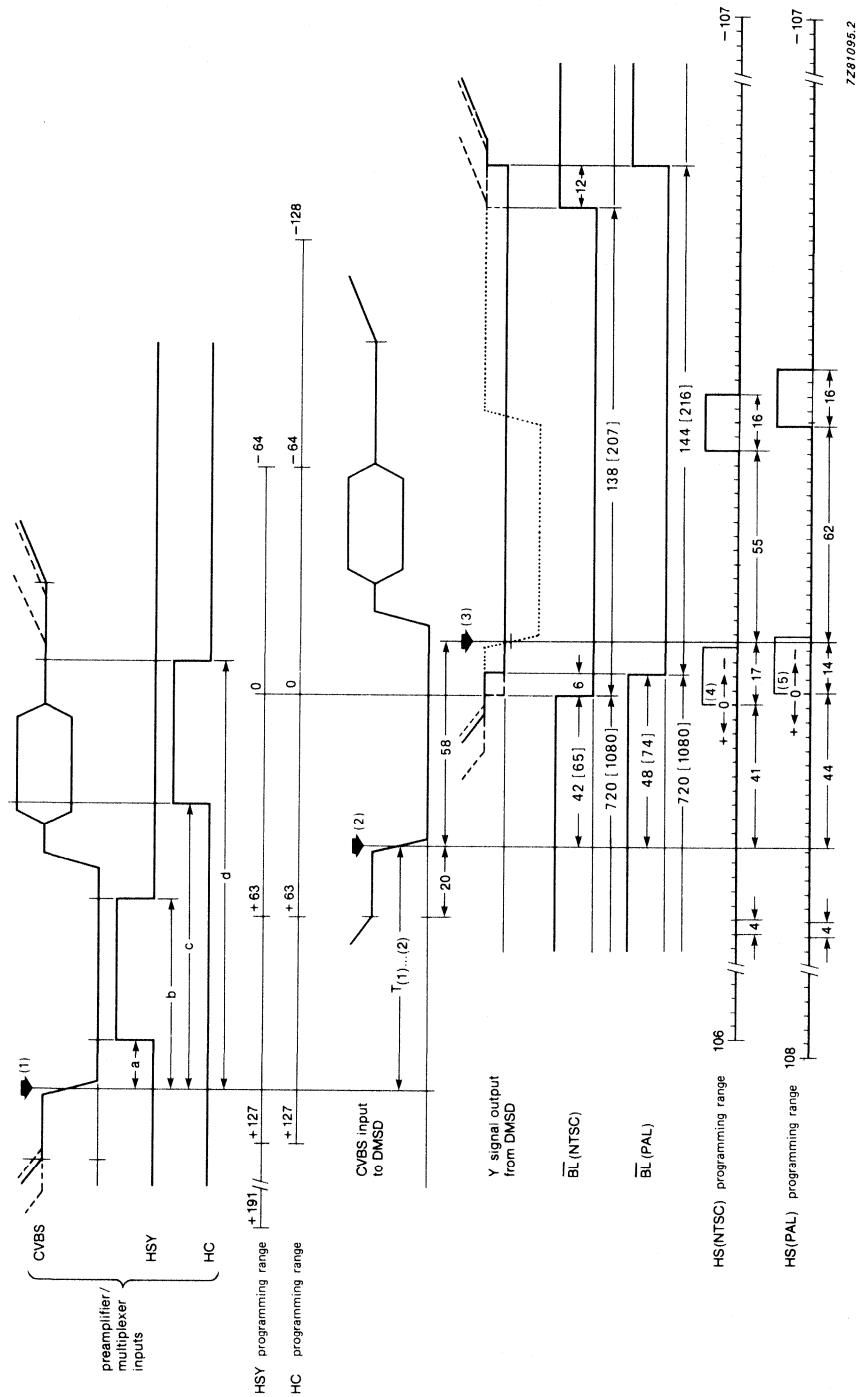


Fig. 10 Signal correlation (see notes on next page).

Notes to Fig. 10

———— represents PAL signals
– – – – – represents NTSC signals (showing tolerance of active video)

HSY and HC inputs are referenced to the analogue input CVBS (1)

$\overline{BL}$ and HS outputs are referenced to the digital input CVBS (2) or to the DMSD output (3).

Waveform timing is indicated in numbers (n) of LL3 cycles (n x $1/f_{LL3}$), where n = 1 for HSY, HC, CVBS input to DMSD and $\overline{BL}$, and n = 4 for HS. In the serial mode the waveform is indicated in numbers of LL2 cycles written in square brackets.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 7,0 V
Input voltage range	V_I	−0,5 to + 7,0 V
Output voltage range (max. output current $I_{O\ max}$ = 20 mA)	V_O	−0,5 to + 7,0 V
Maximum power dissipation per package	P_{tot}	* W
Operating ambient temperature range	T_{amb}	0 to + 70 °C
Storage temperature range	T_{stg}	−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; T_{amb} = 0 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	350	*	mA
Inputs					
Input voltage LOW:					
pins 13 to 17, 21 to 29, 32 and 38	V_{IL}	−0,5	–	+ 0,8	V
pins 1 and 2	V_{IL}	−0,5	–	+ 1,5	V
Input voltage HIGH:					
pins 13 to 16, 21, 22, 24 to 29 and 32	V_{IH}	2,0	–	V_{DD}	V
pins 1, 2 and 38	V_{IH}	3	–	V_{DD}	V
pins 17 and 23	V_{IH}	2,4	–	V_{DD}	V
Input leakage current:					
pins 1, 2, 13 to 17, 21 to 29 and 32	I_I	–	–	10	μA
Input capacitance:					
pins 13 to 16	C_I	–	–	5	pF
pin 17	C_I	–	–	15	pF
pin 23	C_I	–	–	30	pF
pin 38	C_I	8	–	–	pF
pins 1, 2, 21, 22, 24 to 29 and 32	C_I	–	–	7,5	pF
Outputs					
Output capacitance pins 4 to 9 and 12	C_O		*		pF
Output voltage LOW:					
pins 3 to 9, 12 to 16, 18 to 20 and 33 to 37 at I_{OL} = 2,0 mA	V_{OL}	0	–	0,6	V
pin 1 at I_{OL} = 5 mA	V_{OL}	0	–	0,45	V

* Value to be fixed

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Outputs (continued)					
Output voltage HIGH: pins 1, 3 to 9, 12 to 16, 18 to 20 and 33 to 37 at $I_{OH} = -0,5$ mA	V_{OH}	2,2	–	V_{DD}	V
LFCO output (pin 40, AC coupled) 4-bit triangular waveform clocked at 24,576 MHz (peak-to-peak value):					
$R_L \geqslant 10$ kΩ; $C_L < 15$ pF	$V_{O(p-p)}$	1	–	–	V
$R_L \geqslant 1$ kΩ; $C_L < 15$ pF	$V_{O(p-p)}$	0,5	–	–	V
Timing (Fig. 11)					
LL2 cycle time	t_{C2}	46**	–	53**	ns
LL2 duty factor	t_{C2H}/t_{C2}	45	–	55	%
LL2 rise and fall times▲	t_r, t_f	–	–	6	ns
LL3 cycle time	t_{C3}	69**	–	80**	ns
LL3 duty factor	t_{C3H}/t_{C3}	45	–	55	%
LL3 rise and fall times▲	t_r, t_f	–	–	6	ns
Skew time LL2/LL3	t_{skew}	−2	–	+ 2	ns
Input set-up time	t_{SU}	12	–	–	ns
Input hold time	t_{IH}	3	–	–	ns
Output hold time at C_L = 7,5 to 15 pF	t_{OH}	3	–	–	ns
Output delay time at C_L = 7,5 to 15 pF	t_{OD}	–	–	33	ns
Crystal oscillator (Fig. 12)					
Nominal frequency (third harmonic)	f_n	–	24,576	–	MHz
Permissible deviation from nominal frequency (adjustment tolerance)	$\Delta f/f_n$	−50	–	+ 50	10^{-6}
Temperature deviation	$\Delta f/f_n$	−20	–	+ 20	10^{-6}
Temperature range	T_{XTAL}	0	–	+ 70	°C
Load capacitance	C_L	8	–	–	pF
Resonance resistance	R_r	–	40	–	Ω
Motional inductance	L_1	–	*	–	mH
Motional capacitance	C_1	–	*	–	fF
Parallel capacitance	C_0	–	*	–	pF

* Value to be fixed.

** For min. and max. cycle times $\Delta f = \pm 7,1\%$ of typical frequency value.

▲ Difference between t_r and t_f of LL3 must be less than 1 ns; rising and falling edge are assumed to be smooth due to low pass filtering.

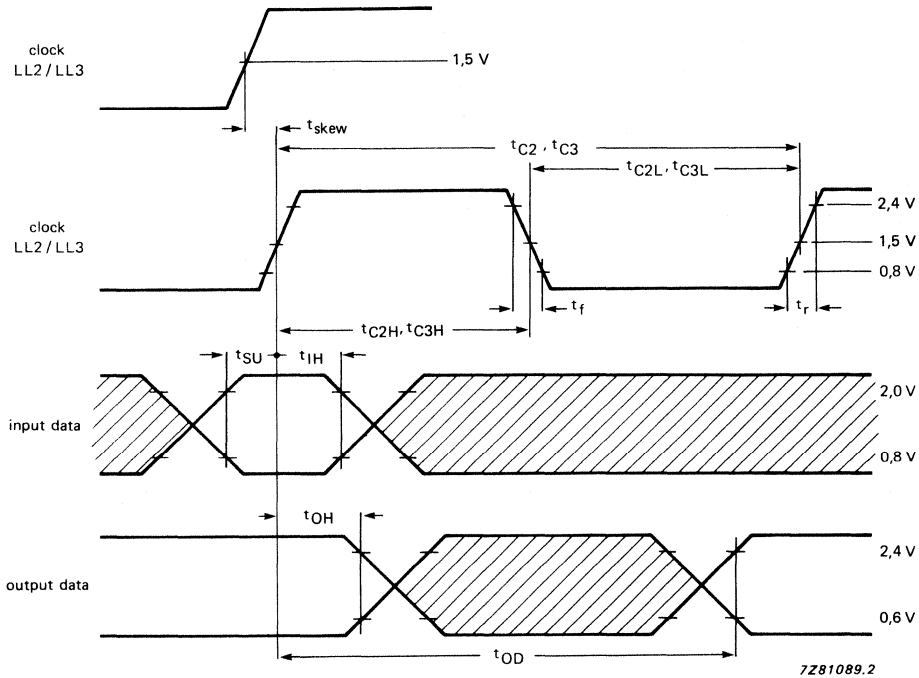


Fig. 11 Timing diagram.

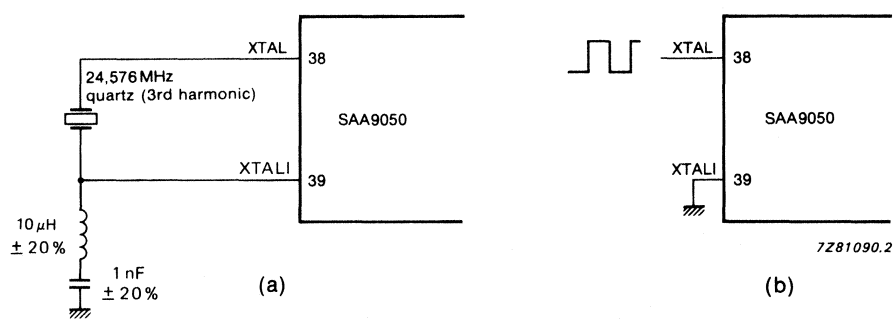
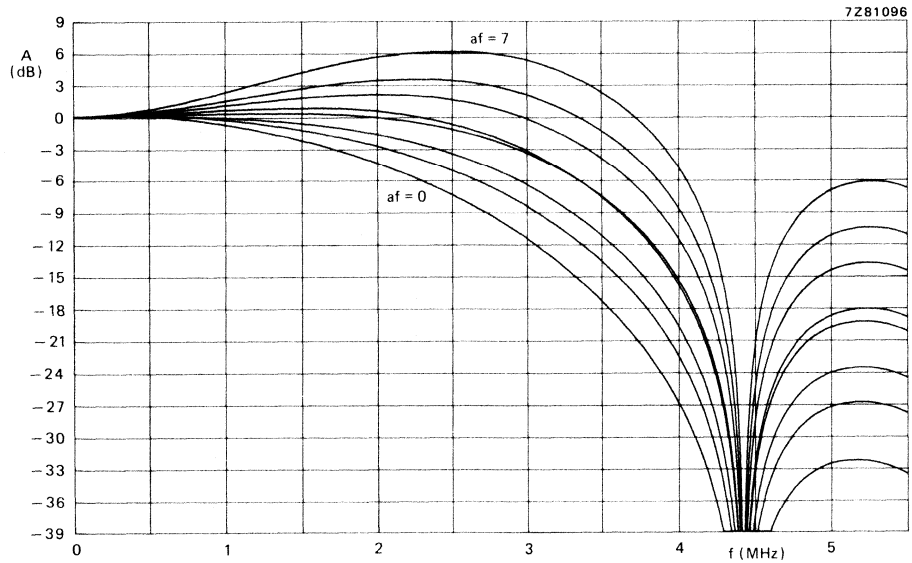


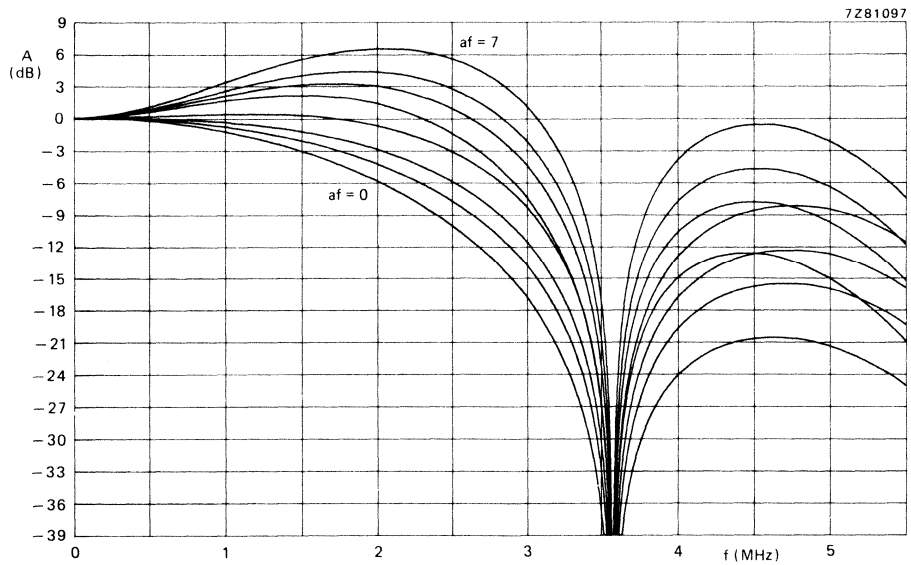
Fig. 12 Oscillator circuit requirements: (a) with quartz crystal; (b) with external clock.

DEVELOPMENT DATA

(a)



(b)



Aperture factor selection:

af	H2	H1	H0
0	0	0	0
————	through to	————	
7	1	1	1

Fig. 13 Horizontal peaking aperture factors (af): (a) YPN = logic 0 (colour subcarrier = 4,43 MHz); (b) YPN = logic 1 (colour subcarrier = 3,58 MHz).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CLOCK GENERATOR CIRCUIT

GENERAL DESCRIPTION

The SAA9057 clock generator circuit is for application in memory-based feature tv receivers and in digital tv concepts with line-locked sampling. The circuit employs a PLL frequency multiplier to give three different line-locked clock output frequencies, a bypass switch for the PLL is provided. All clock outputs have high driving capability. Skew control and power-fail detection circuits are included.

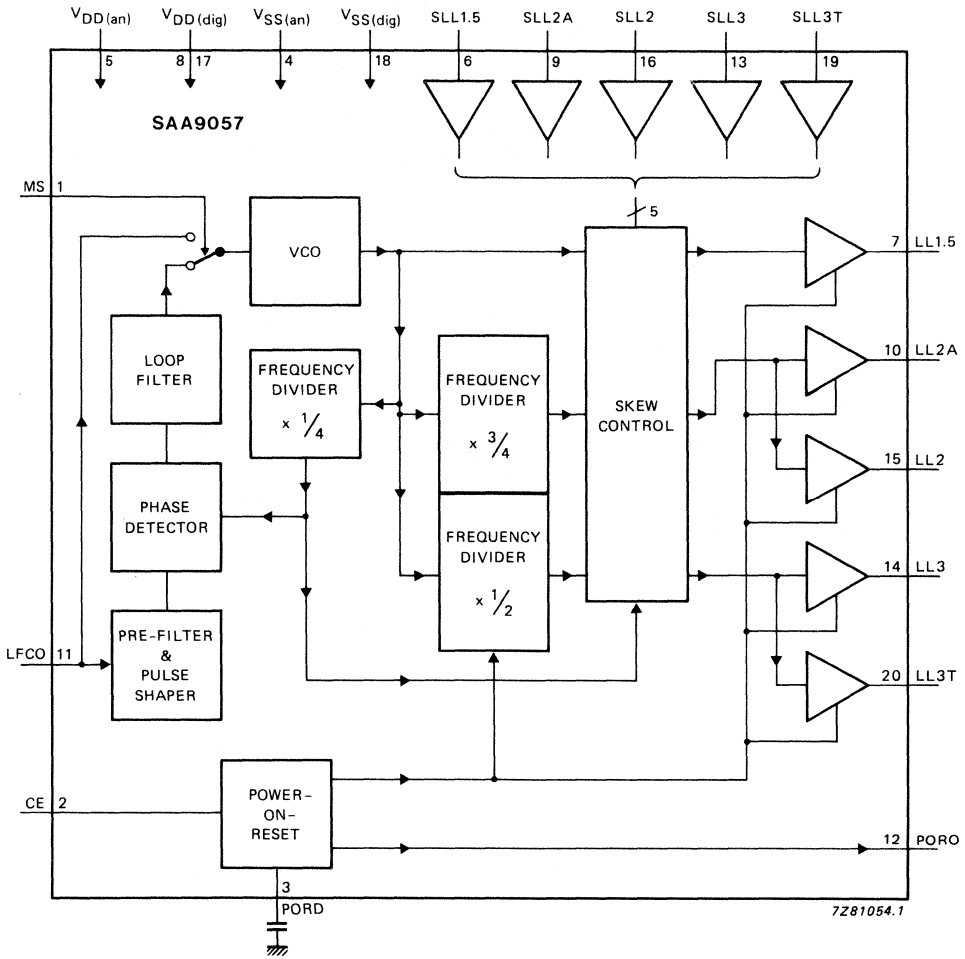


Fig. 1 Block diagram.

PACKAGE OUTLINE

20-lead DIL; plastic (SOT-146).

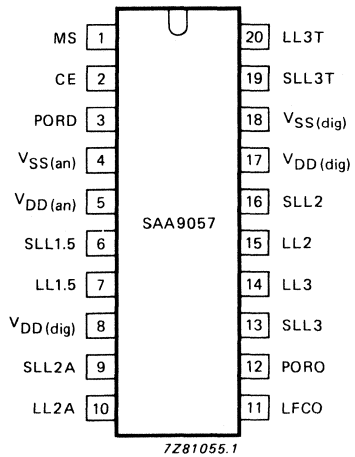


Fig. 2 Pinning diagram.

PINNING

1	MS	mode select input. MS = LOW for normal operation in which the CGC generates clocks with reference to LFCO MS = HIGH disables the PLL and connects the LFCO input to the control input of the VCO, providing VCO, frequency divider and buffer facilities only
2	CE	chip enable. CE = HIGH enables the VCO and the output buffers; CE = LOW sets the buffers to high impedance off-state and inhibits VCO oscillation
3	PORD	power-on-reset delay. Duration of delay is determined by an external capacitor at this pin
4	$V_{SS(an)}$	ground (0 V) for analogue circuits
5	$V_{DD(an)}$	positive supply voltage (+ 5 V) for analogue circuits
6	SLL1.5	sensing input for LL1.5 skew control. Pin 6 input amplifier can handle low-level sinusoidal clock waveforms. Strap to pin 7 when not using external clock drivers or low-level clocks
7	LL1.5	27 MHz line-locked clock. The waveform is rectangular and the duty factor is 50%
8	$V_{DD(dig)}$	positive supply voltage (+ 5 V) for digital circuits (no internal connection to pin 17)
9	SLL2A	sensing input for LL2A skew control. Pin 9 input amplifier can handle low-level sinusoidal clock waveforms. Strap to pin 10 when not using external clock drivers or low-level clocks
10	LL2A	20,25 MHz line-locked clock. The waveform is rectangular and the duty factor is 50%
11	LFCO	line frequency control input to which all internal clocks are referred. The waveform is triangular with 4-bit quantization and 24,576 MHz sample rate

12	PORO b	power-on-reset output. Goes LOW following power-on or power fail. Remains LOW for a period determined by external capacitor at pin 3. It is also activated by a slow or fast fall of supply voltage to below operating level. PORO can be used as a reset signal for the whole digital tv system.
13	SLL3	sensing input for LL3 skew control. Pin 13 input amplifier can handle low-level sinusoidal waveforms. Strap to pin 14 when not using external clock drivers or low-level clocks
14	LL3	13,5 MHz line-locked clock. The waveform is rectangular and the duty factor is 50%
15	LL2	20,25 MHz line-locked clock. The waveform is rectangular and the duty factor is 50%
16	SLL2	sensing input for LL2 skew control. Pin 16 input amplifier can handle low-level sinusoidal waveforms. Strap to pin 15 when not using external clock drivers or low-level clocks
17	$V_{DD(dig)}$	positive supply voltage (+ 5 V) for digital circuits
18	$V_{SS(dig)}$	ground (0 V) for digital circuits (no internal connection to pin 8)
19	SLL3T	sensing input for LL3T skew control. Pin 19 input amplifier can handle low-level sinusoidal waveforms. Strap to pin 20 when not using external clock drivers or low-level clocks
20	LL3T	13,5 MHz line-locked clock. The waveform is rectangular and the duty factor is 50%

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The SAA9057 provides all the clock waveforms required in a typical digital tv system. This can comprise an analogue-to-digital converter (ADC, PNA7509), a sample-rate converter (SRC, SAA9058), a digital multi-standard decoder (DMSD, SAA9050), a digital deflection controller (DDC, SAA9060) with single or double line-frequency, plus extensions to add to the features available in the system.

The frequency of the reference input LFCO (a 6,75 MHz triangular waveform from the DMSD) is multiplied to 27 MHz by the PLL. All clock outputs are derived from this by frequency dividers with ratios as shown in Figs 1 and 3.

Each clock output is skew-controlled so that a temperature and load-independent phase relationship is maintained between the clock outputs.

The LL1.5, LL2 and LL3 outputs are rectangular waveforms with a 50% duty factor.

The clock outputs are inhibited from power-on until the circuit has stabilized. The inhibit time is determined by the capacitor at pin 3. A power-fail detector is combined with the inhibit circuit so that the DDC is protected from unspecified clock frequencies that could occur in the event of a power failure. The PORO output (pin 12) indicates that the power supply is stable and can be used to drive other power-on-reset circuits.

The phase detector and loop filter are disabled by the mode select input at pin 1 which internally connects the VCO control input to the LFCO input at pin 11. The circuit now operates as an oscillator followed by stages of frequency division, uses for which may be found in analogue environments of feature tv applications.

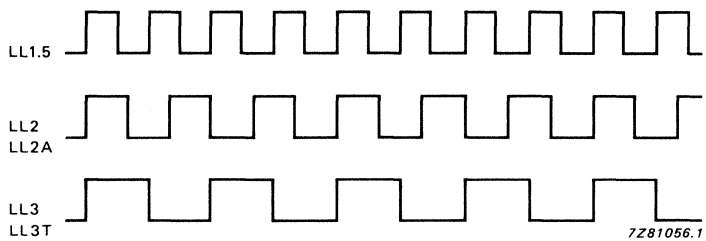


Fig. 3 Relationship between clock outputs.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage range	$V_{DD(dig)}$	−0,5 to + 0,7	V
	$V_{DD(an)}$	−0,5 to + 7,0	V
Input voltage at any pin with respect to ground	V_I	−0,5 to + 7,0	V
Input/output current	I_I, I_O	max. *	mA
Total power dissipation	P_{tot}	*	W
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Storage temperature range	T_{stg}	−65 to −150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	*	*	mA
Input LFCO (triangular waveform; resolution = 4 bits)					
Frequency	f_{LFCO}	6,0	6,75	7,4	MHz
Amplitude (peak-to-peak value)	$V_{LFCO(p-p)}$	1,0	2,0	V_{DD}	V
PLL					
Natural frequency	f_n	55	80	115	kHz
Damping coefficient	D	0,5	0,7	1,0	
Jitter		–	–	*	ns
Clock outputs					
Rise time (all clocks)	t_r	–	–	3	ns
Fall time (all clocks)	t_f	–	–	3	ns
Skew (all clocks)	t_{skew}	−2	–	+ 2	ns
Output voltage HIGH (except LL2A)	V_{OH}	2,8	–	V_{DD}	V
Output voltage HIGH (LL2A only)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (all clocks)	V_{OL}	0	–	0,4	V
Duty factor	δ	45	50	55	%

* Values not yet available.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Load capacitance:					
LL1.5	C_L	–	–	30	pF
LL2	C_L	–	–	50	pF
LL2A	C_L	–	–	20	pF
LL3T	C_L	–	–	20	pF
LL3	C_L	–	–	50	pF

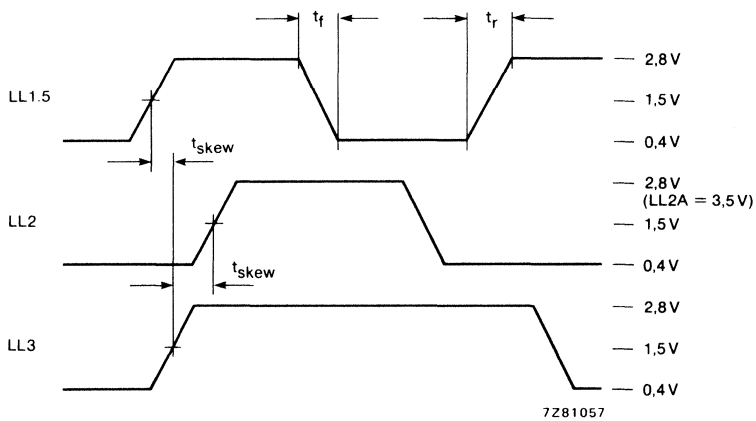


Fig. 4 Timing diagram.

SAMPLE-RATE CONVERTER

GENERAL DESCRIPTION

The SAA9058 sample-rate converter (SRC) is for use in digital TV receiver applications. It converts the sampling rate of digital signals by a factor of 2/3, e.g. from 20,25 to 13,5 MHz, using a phase-linear, finite impulse response (FIR) filter with time-varying coefficients. Only two clocks are required; the data format is two's complement, and the word length at both input and output is seven bits.

The FIR filter creates a filter-algorithm to interpolate digitized composite video signals (DCVBS) into a slower sample rate that is suitable for video decoding. The circuit gives low attenuation of colour subcarrier, gives high rejection of aliasing components and has unity DC gain.

It is intended for use with the 7-bit analogue-to-digital converter PNA7509 and the digital multistandard decoder SAA9050, with DCVBS in PAL, NTSC or SECAM. Other applications are digital anti-aliasing filtering, rejection of harmonics caused by analogue-to-digital conversion and data reduction.

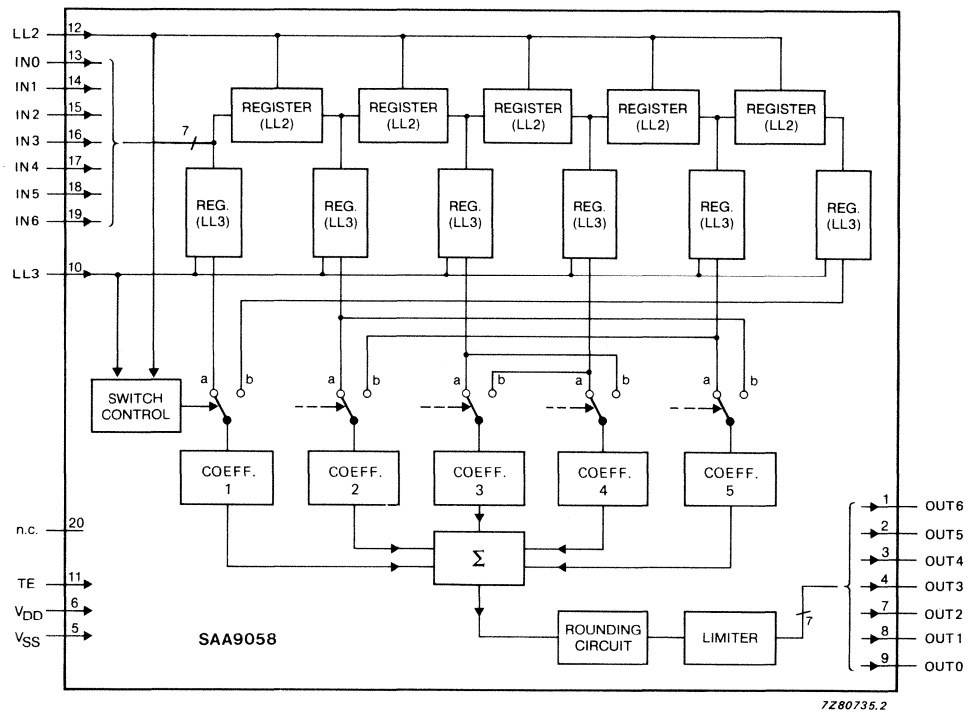


Fig. 1 Block diagram (see Fig. 3 for switch timing).

PACKAGE OUTLINE

20-lead DIL; plastic (SOT-146).

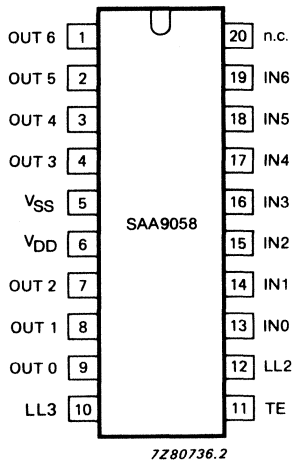


Fig. 2 Pinning diagram.

PINNING

1	OUT6	output data
2	OUT5	
3	OUT4	
4	OUT3	
5	V_{SS}	ground (0 V)
6	V_{DD}	positive supply voltage (+5 V)
7	OUT2	output data
8	OUT1	
9	OUT0	
10	LL3	output clock
11	TE	production test input; V_{SS} for all applications
12	LL2	input clock
13	IN0	input data
14	IN1	
15	IN2	
16	IN3	
17	IN4	
18	IN5	
19	IN6	
20	n.c.	not connected

OPERATION

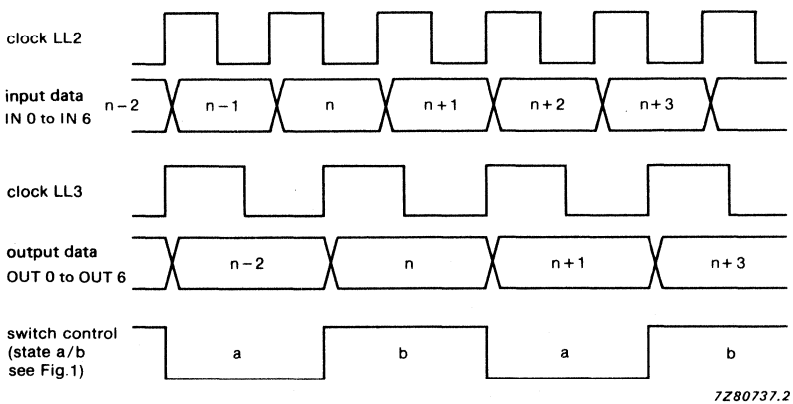


Fig. 3 Relationship of inputs to outputs.

Frequency response

The virtual frequency response in the 2 x LL2 (40,5 MHz) domain is interpreted as the characteristic of the interpolation filter directly before conversion to the LL3 (13,5 MHz) sample rate and the spectral components beyond LL3/2 are aliased into the baseband.

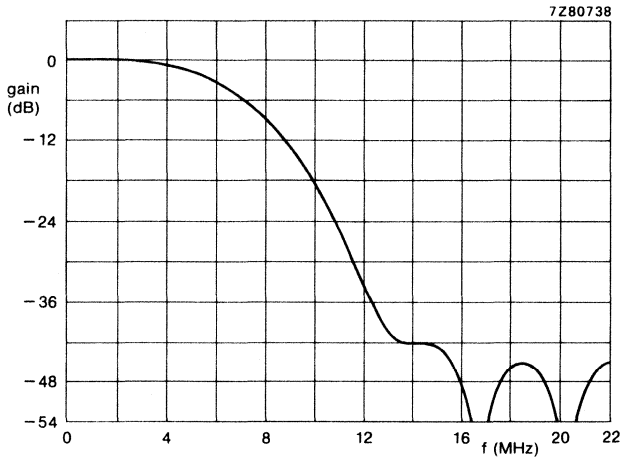


Fig. 4 Frequency response.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 7 V
Input voltage range	V_I	−0,5 to + 7 V
Output voltage range to $I_{O\,max}$ = 20 mA	V_O	−0,5 to + 7 V
Maximum power dissipation	P_{tot}	0,5 W
Operating ambient temperature range	T_{amb}	0 to + 70 °C
Storage temperature range	T_{stg}	−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

T_{amb} = 0 to +70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	5,0	5,5	V
Supply current at V_{DD} = 5,5 V, data outputs not connected, data inputs LOW and frequency nominal	I_{DD}	–	< 100*	65	mA
Inputs					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH (except LL2, LL3)	V_{IH}	2,0	–	V_{DD}	V
Input voltage HIGH (LL2, LL3)	V_{IH}	2,4	–	V_{DD}	V
Input leakage current	I_I	–	–	10	μA
Input capacitance (LL2)	C_I	–	–	10	pF
Input capacitance (LL3)	C_I	–	–	10	pF
Input capacitance (D0 to D6)	C_I	–	–	5	pF
Outputs					
Output voltage HIGH at I_{OH} = −0,5 mA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OH} = 2,0 mA	V_{OL}	0	–	0,6	V
Timing (Fig. 5)					
LL2 cycle time	t_{C2}	46	–	53	ns
LL2 duty factor t_{C2H}/t_{C2}	–	45	–	55	%
LL2 rise and fall time	t_r, t_f	–	–	6**	ns
LL3 cycle time	t_{C3}	69	–	80	ns
LL3 duty factor t_{C3H}/t_{C3}	–	45	–	55	%
LL3 rise and fall time	t_r, t_f	–	–	6**	ns
Skew time	t_{skew}	−2	–	+ 2	ns
Input data set-up time	t_{SU}	12	–	–	ns
Input data hold time	t_{HD}	3	–	–	ns
Output data load capacitance	C_L	7,5	–	15	pF
Output data hold time	t_{OH}	3	–	–	ns
Output data delay time	t_{OD}	–	–	33	ns

* For digital TV application.

** Difference between t_r, t_f of LL2 and t_r, t_f of LL3 shall be less than 2 ns. Rising and falling edges of clocks are assumed to be smooth due to low pass filtering.

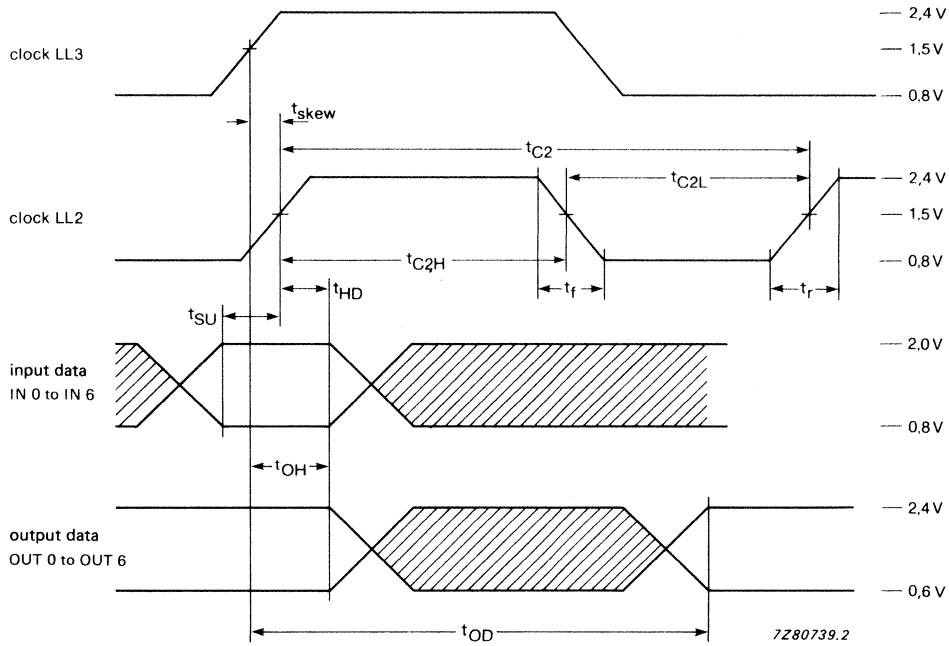


Fig. 5 Timing diagram.

DEVELOPMENT DATA

6-FUNCTION ANALOGUE MEMORY; MICROCOMPUTER CONTROLLED

The SAB3013 is a MOS N-channel integrated circuit which provides 6 analogue memories controlled by a microcomputer.

Features

- 6-function analogue memory; D/A converter with 6-bit resolution.
- The output of the analogue values is pulse-width modulated with adjustable repetition rate (max. 21,8 kHz).
- Microcomputer-adapted asynchronous serial interface for data input (CBUS).
- Parallel operation of up to four SAB3013 circuits is possible.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}	0 to	+70 °C
Clock frequency	f_{CLK}	<	1,4 MHz
Supply current; V_{DD} = 5 V; I_O = 0; T_{amb} = 25 °C	I_{DD}	typ.	15 mA

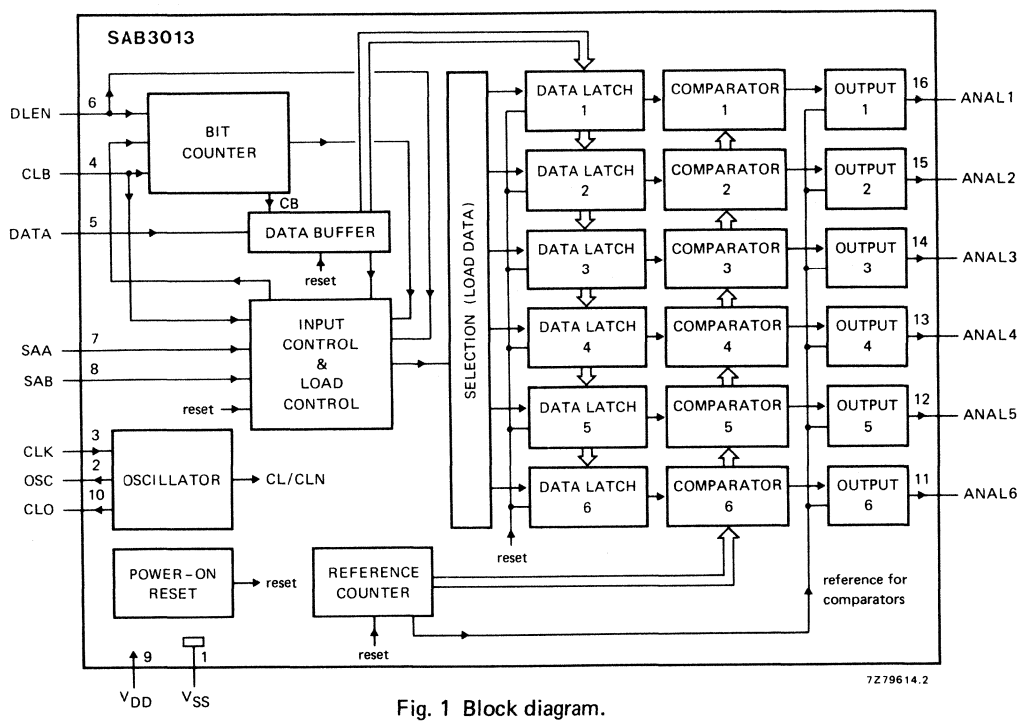


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

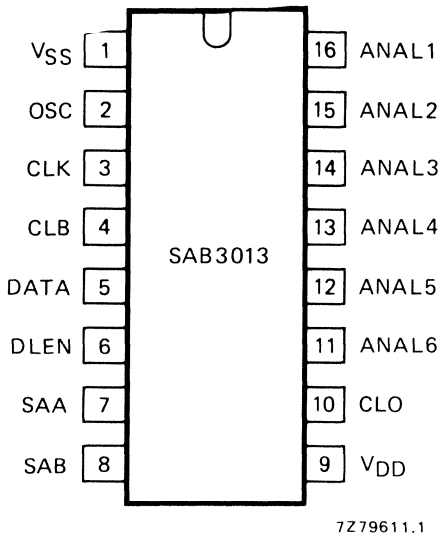


Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)	
9	V_{DD}	positive supply	
4	CLB	asynchronous clock pulse	CBUS
5	DATA	data input	CBUS
6	DLEN	data line enable input	CBUS
7	SAA	address inputs	
8	SAB	address inputs	
2	OSC	oscillator output	
3	CLK	oscillator input (Schmitt-trigger)	
16	ANAL1	analogue outputs	
15	ANAL2	analogue outputs	
14	ANAL3	analogue outputs	
13	ANAL4	analogue outputs	
12	ANAL5	analogue outputs	
11	ANAL6	analogue outputs	
10	CLO	buffered oscillator output	

GENERAL DESCRIPTION

The SAB3013 is designed to deliver analogue values in microcomputer-controlled television receivers and radio receivers. The circuit comprises an analogue memory and D/A converter for 6 analogue functions with a 6-bit resolution for each. The information for the analogue memory is transfered by the microcomputer via an asynchronous serial data bus.

The SAB3013 accomplishes a word format recognition, so it is able to operate one common data bus together with circuits having different word formats.

The data word of the microcomputer used for the SAB3013 consists of information for addressing the appropriate SAB3013 circuit (2-bits), for addressing the analogue memories concerned (3-bits) and processing of the wanted analogue value (6-bits). The address of the circuit is externally programmable via two inputs. It is possible to address up to four SAB3013 circuits via one common bus.

The built-in oscillator can be used for a frequency between 30 kHz and 1,4 MHz. The analogue values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ (max. 21,8 kHz at f_{CLK} = 1,4 MHz), and the analogue values are determined by the ratio of the HIGH-time and the cycle time. A d.c. voltage proportional to the analogue value is obtained by means of an external integration network (low-pass filter).

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance to the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 7,5		V
Input voltage range	V_I	−0,3 to + 15		V
Input current	$\pm I_I$	max.	100	μA
Output voltage (open drain outputs)	V_O	V_{SS} to 15		V
Output current (open drain/push-pull outputs)	$\pm I_O$	max.	10	mA
Power dissipation per output	P_O	max.	25	mW
Total power dissipation per package	P_{tot}	max.	250	mW
Operating ambient temperature range	T_{amb}	0 to + 70		°C
Storage temperature range	T_{stg}	−20 to + 125		°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltage	V_{DD}	4,5	5	5,5	V	
Supply current	I_{DD}	–	–	35	mA	V_{DD} = 5,5 V
Inputs DATA, CLB, DLEN, SAA, SAB						
Input voltage LOW	V_{IL}	0	–	12	V	
Input voltage HIGH	V_{IH}	2,0	–	12	V	
Input leakage current	I_{IR}	–	–	1	μA	V_I = –0,3 to + 12 V
Outputs ANAL1 to ANAL6 (open drain)						
Output voltage LOW	V_{OL}	–	–	0,7	V	I_O = 6 mA
Output leakage current	I_{OR}	–	–	20	μA	V_{OH} = 15 V *
Load capacitance	C_L	–	–	1000	pF	
Input CLK						
Input voltage LOW	V_{IL}	–0,3	–	0,8	V	
Input voltage HIGH	V_{IH}	3,5	–	12	V	
Input leakage current	I_{IR}	–	–	1	μA	V_I = –0,3 to 12 V
Pulse duration HIGH	t_{WH}	355	–	–	ns	
Pulse duration LOW	t_{WL}	355	–	–	ns	
Output CLO						
Output voltage LOW	V_{OL}	–	–	0,8	V	I_O 500 μA
Output voltage HIGH	V_{OH}	3,5	–	–	V	$-I_O$ = 100 μA
Inputs DATA, CLB						
Pulse duration HIGH	t_{WH}	450	–	–	ns	see Fig. 3
Pulse duration LOW	t_{WL}	450	–	–	ns	see Fig. 3
Input frequency CLB	f_{CLB}	0	–	1	MHz	
Internal oscillator CLK/OSC						
External resistor	R	27	–	1000	kΩ	
External capacitor	C	27	–	1000	pF	
Clock frequency	f_{CLK}	0,7	1,0	1,4	MHz	R = 27 kΩ; C = 27 pF
Frequency for external oscillator	f_{CLK}	0,03	–	1,4	MHz	

* For correct operation: V_{OHmin} = 3 V.

CHARACTERISTICS (continued)

V_{SS} = 0; T_{amb} = 0 to + 70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Timing (see Fig. 3)						
Data set-up time DATA → CLB	t_{SUDA}	800	–	–	ns	measured with a voltage swing of min. V_{IH}–V_{IL}
Data hold time DATA → CLB	t_{HDDA}	300	–	–	ns	
Enable set-up time DLEN → CLB	t_{SUEN}	400	–	–	ns	
Disable set-up time CLB → DLEN	t_{SUDI}	400	–	–	ns	
Set-up time DLEN → CLB (load pulse)	t_{SULD}	1000	–	–	ns	

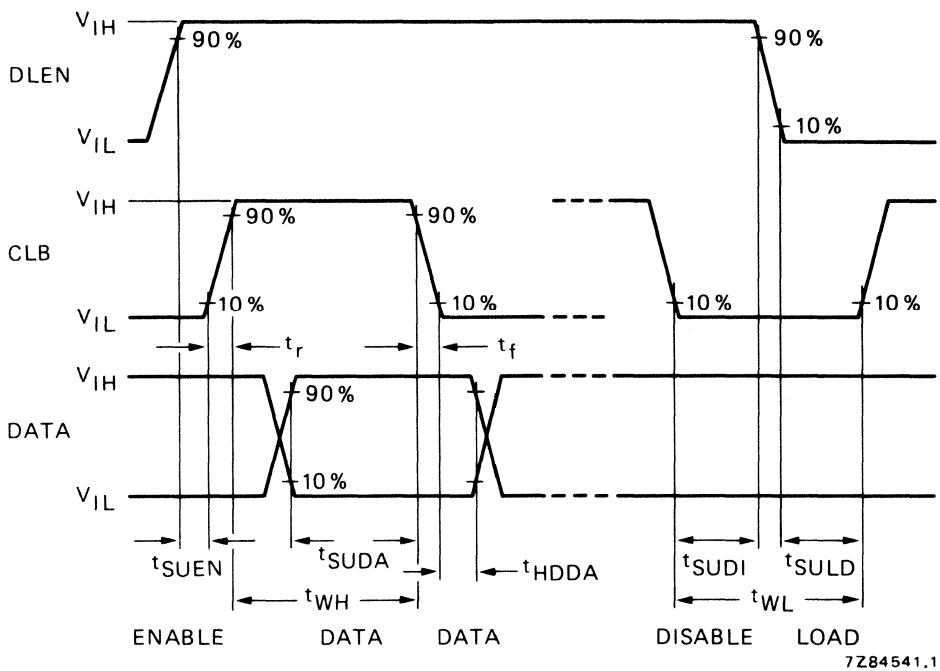


Fig. 3 CBUS timing.

OPERATION DESCRIPTION

The data input is achieved serially via the inputs DATA, DLEN and CLB. Clock pulses have to be applied at input CLB for data processing at input DATA. Data processing is only possible when DLEN = HIGH. The data from the data buffer is loaded directly into the output latch on receipt of a load pulse at input CLB (DLEN = LOW), provided the following conditions are met:

- 12 clock pulses must be received at input CLB (word format control) during transmission (DLEN = HIGH).
- The start-bit must be LOW.
- The system address bits must be A = SAA and B = SAB.
- The analogue address must be valid.

The data word for the SAB3013 consists of the following bits (see Fig. 4):

1 start-bit
2 system address bits (A and B)
3 address bits for selection of the required analogue memory
6 data bits for processing the analogue value

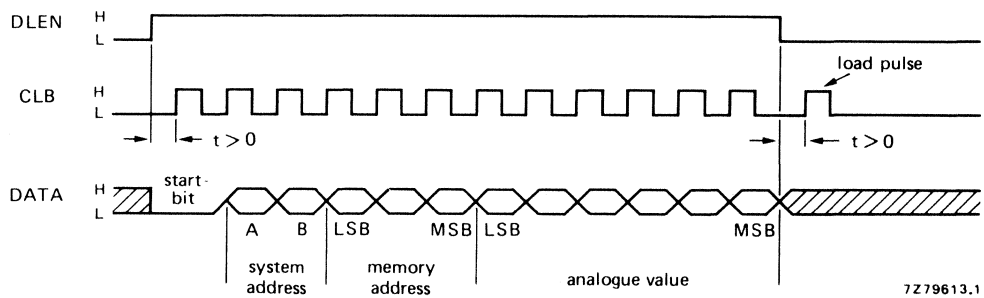


Fig. 4 Waveforms showing a CBUS transmission.

ADDRESS inputs (SAA, SAB)

The address of the SAB3013 is programmed at the inputs SAA and SAB. These inputs must be defined and not left open-circuit.

Reset

The circuit generates internally a reset-cycle with a duration of one clock cycle after switching on the supply. If a spike on the supply is likely to destroy data, a reset signal will be generated. All analogue memories are set to 50% (analogue value 32/64) after the reset cycle. The supply voltage rise dV_{DD}/dt must be max. 0,5 V/μs and min. 0,2 V/μs.

Oscillator inputs (CLK, OSC)

The oscillator frequency is determined by the external circuitry connected to the terminals CLK and OSC as shown in Fig. 5. Instead of this circuitry an externally generated oscillator signal can be connected to input CLK.

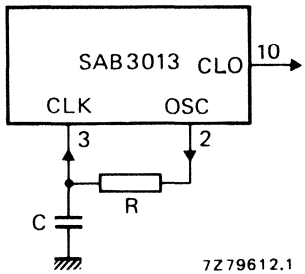


Fig. 5 Application advice for the oscillator.

At output CLO a buffered oscillator signal is available for control of other circuits.

For f_{CLK} = 0,7 to 1,4 MHz;
R = 27 kΩ; C = 27 pF.

Analogue outputs (ANAL1 to ANAL6)

The analogue values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ at the outputs ANAL1 to ANAL6. The analogue value is determined by the ratio of the HIGH-time and the cycle time (values between 1/64 and 64/64 can be obtained).

Table 1 Addressing of the analogue data registers

R_A LSB	R_B	R_C MSB	addressing
0	0	0	not valid
1	0	0	ANAL1
0	1	0	ANAL2
1	1	0	ANAL3
0	0	1	ANAL4
1	0	1	ANAL5
0	1	1	ANAL6
1	1	1	not valid

Table 2 Correlation of analogue value to analogue output signal

analogue value	binary input data LSB ... MSB	duty cycle 'low'	duty cycle 'high'
lowest value	0 0 0 0 0 0	63/64	1/64
	1 0 0 0 0 0	62/64	2/64
power-on reset value	1 1 1 1 1 0	32/64	32/64
highest value	0 1 1 1 1 1	1/64	63/64
	1 1 1 1 1 1	0	64/64

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3035 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 8 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 8 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 16)	V_{P1}	typ.	12 V
(pin 22)	V_{P2}	typ.	13 V
(pin 17)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 16)	I_{P1}	typ.	32 mA
(pin 22)	I_{P2}	typ.	0,1 mA
(pin 17)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	400 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

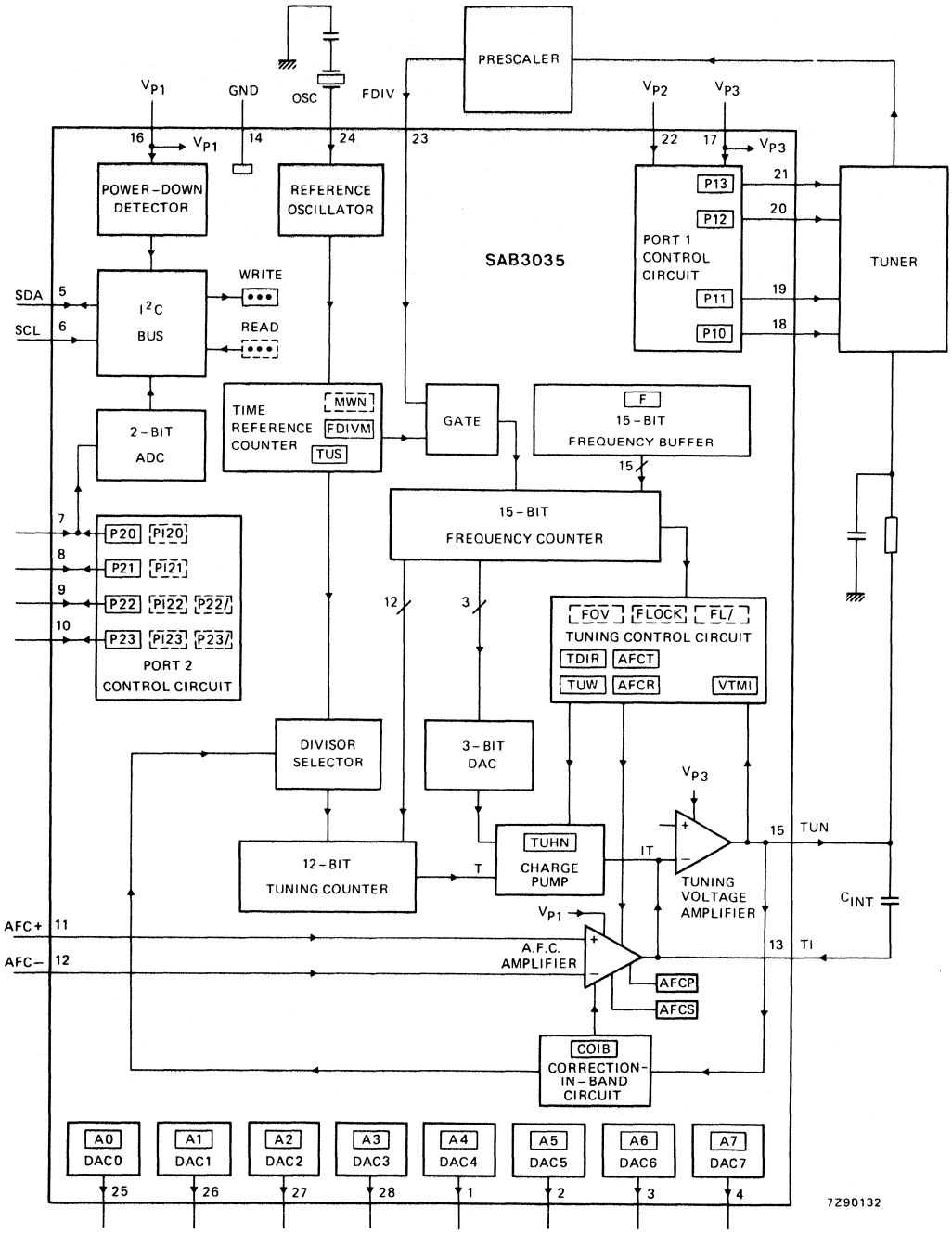


Fig. 1 Block diagram.

DEVELOPMENT DATA

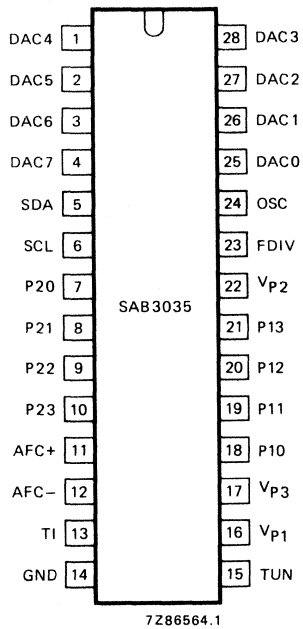
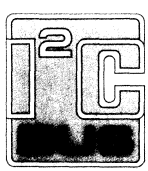


Fig. 2 Pinning diagram.

PINNING

1	DAC4	outputs of static DACs
2	DAC5	
3	DAC6	
4	DAC7	
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	P20	general purpose input/output ports
8	P21	
9	P22	
10	P23	
11	AFC+	a.f.c. inputs
12	AFC−	
13	TI	tuning voltage amplifier inverting input
14	GND	ground
15	TUN	tuning voltage amplifier output
16	V_{P1}	+12 V supply voltage
17	V_{P3}	+32 V supply for tuning voltage amplifier
18	P10	High-current band-selection output ports
19	P11	
20	P12	
21	P13	
22	V_{P2}	positive supply for high-current band-selection output circuits
23	FDIV	input from prescaler
24	OSC	crystal oscillator input
25	DAC0	outputs of static DACs
26	DAC1	
27	DAC2	
28	DAC3	



Purchase of Philips I²C components conveys a licence under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

The SAB3035 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Eight 6-bit digital-to-analogue converters DAC0 to DAC7 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

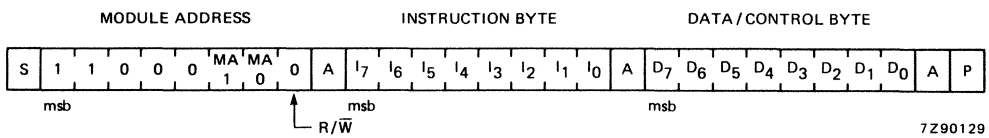


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

	INSTRUCTION BYTE								DATA / CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
freq.	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X2, X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

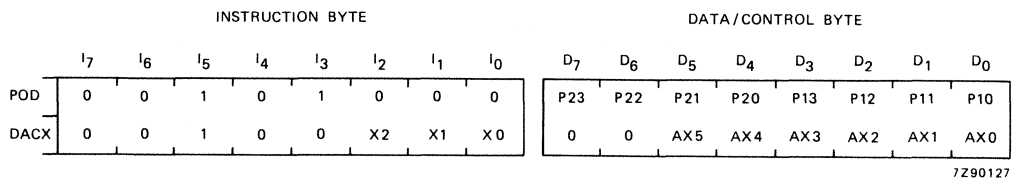


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

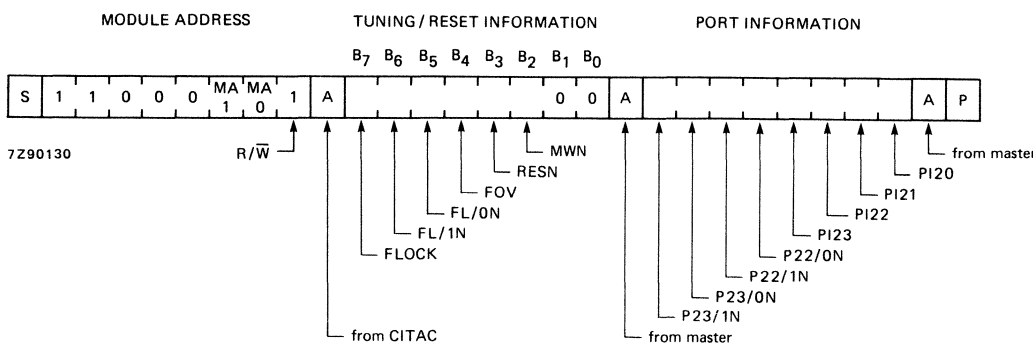


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

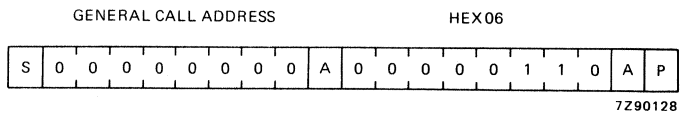


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 16)	V_{P1}	−0,3 to +18	V
(pin 22)	V_{P2}	−0,3 to +18	V
(pin 17)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 5)	V_{SDA}	−0,3 to +18	V
(pin 6)	V_{SCL}	−0,3 to +18	V
(pins 7 to 10)	V_{P2X}	−0,3 to +18	V
(pins 11 and 12)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 13)	V_{TI}	−0,3 to V_{P1}*	V
(pin 15)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 18 to 21)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 23)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 24)	V_{OSC}	−0,3 to +5	V
(pins 1 to 4 and 25 to 28)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

DEVELOPMENT DATA

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	20	32	50	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	−2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	400	–	mW
Operating ambient temperature	T_{amb}	−20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 5); SCL input (pin 6)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 5, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 7 to 10, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 11, 12)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 13, 15)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 18 to 21)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 23)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 7 (pins 25 to 28 and 1 to 4)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 7) for valid module address as a function of MA1, MA0					
MA1 0	MA0 0	V_{VA00}	–0,3	–	16	V
0	1	V_{VA01}	–0,3	–	0,8	V
1	0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1	1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

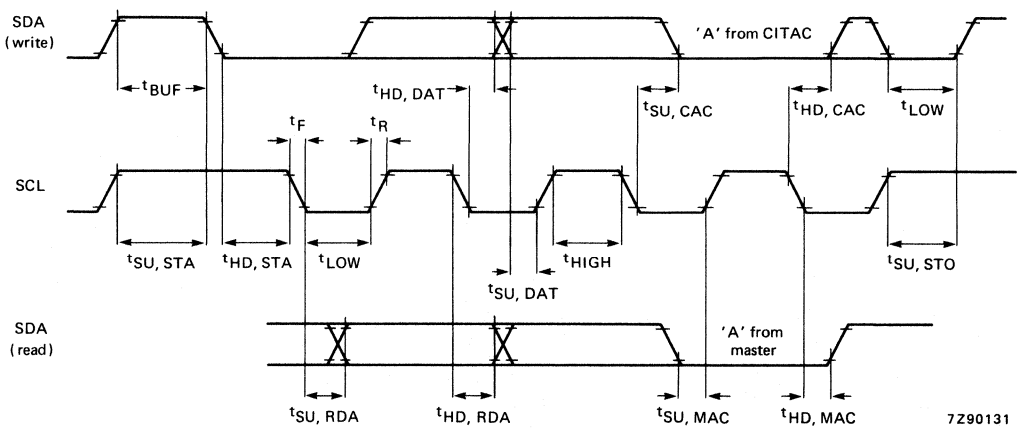


Fig. 8 I²C bus timing SAB3035.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3036 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 5)	V_{P1}	typ.	12 V
(pin 14)	V_{P2}	typ.	13 V
(pin 9)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 5)	I_{P1}	typ.	23 mA
(pin 14)	I_{P2}	typ.	0,1 mA
(pin 9)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	300 mW
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102H).

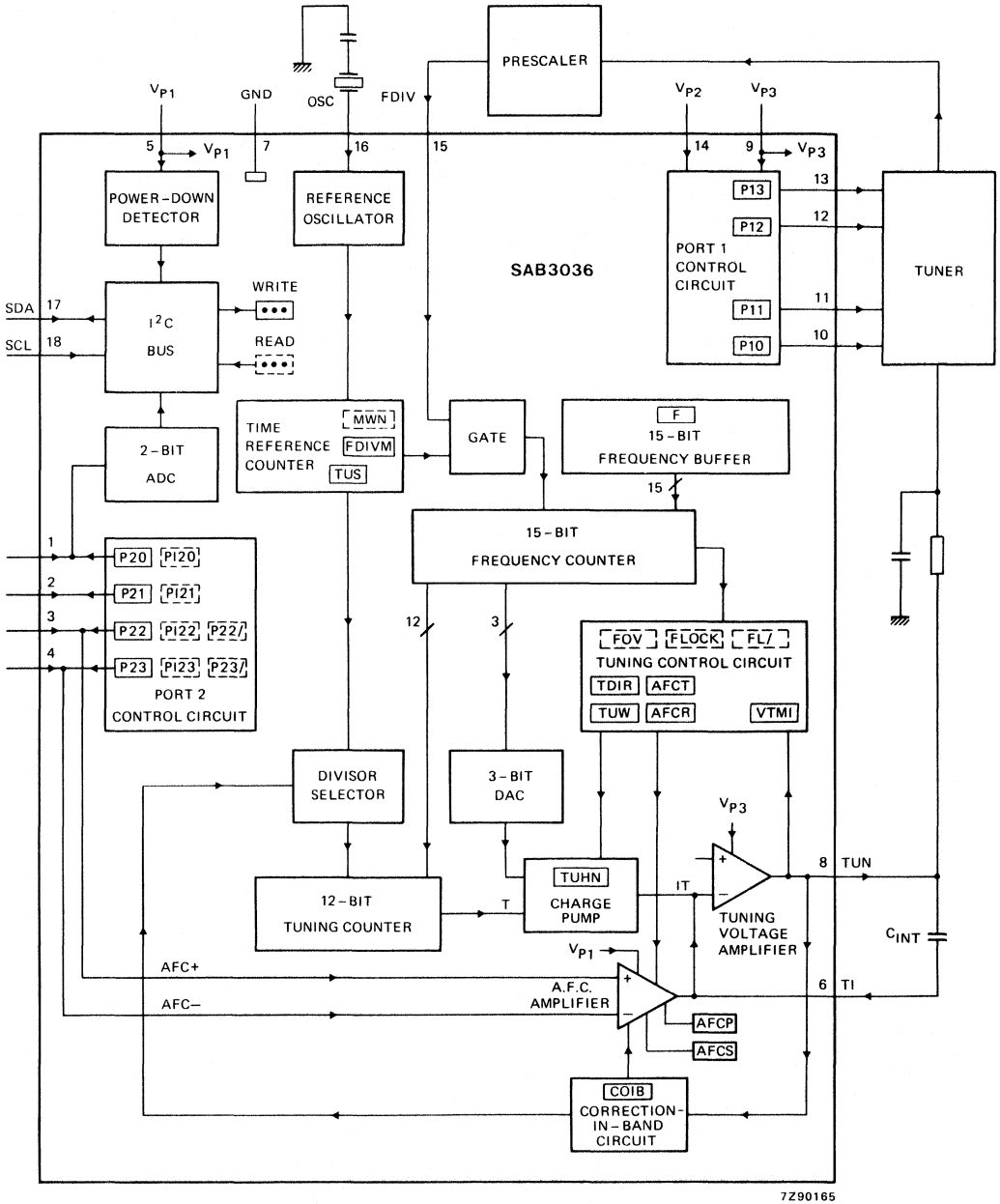


Fig. 1 Block diagram.

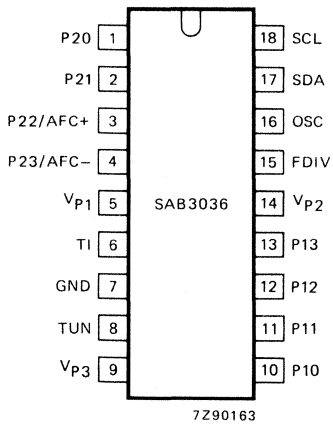


Fig. 2 Pinning diagram.

PINNING

1	P20	general purpose input/output ports
2	P21	
3	P22/AFC+	general purpose input/output ports and a.f.c. inputs
4	P23/AFC−	
5	V_{P1}	+ 12 V supply voltage
6	TI	tuning voltage amplifier inverting input
7	GND	ground
8	TUN	tuning voltage amplifier output
9	V_{P3}	+ 32 V supply for tuning voltage amplifier
10	P10	high-current band-selection output ports
11	P11	
12	P12	
13	P13	
14	V_{P2}	positive supply for high-current band-selection output circuits
15	FDIV	input from prescaler
16	OSC	crystal oscillator input
17	SDA	serial data line, I^2C bus
18	SCL	serial clock line, I^2C bus

DEVELOPMENT DATA

Purchase of Philips I^2C components conveys a licence under the Philips' I^2C patent to use the components in the I^2C system provided the system conforms to the I^2C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

The SAB3036 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals and are connected with the AFC+ and AFC− inputs respectively. The a.f.c. amplifier must be switched off when P22 and/or P23 are used. When a.f.c. is used, P22 and P23 must be programmed HIGH (high impedance state). With the aid of port P20, up to three independent module addresses can be programmed.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

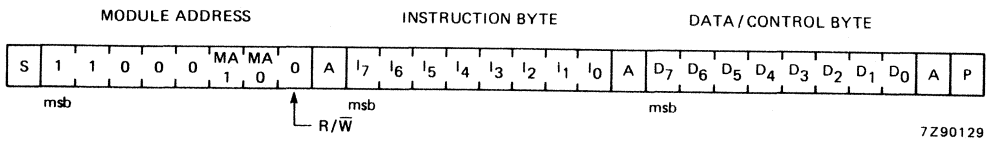


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

OPERATION (continued)

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at $\Delta f = 50$ kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

$\Delta f = 50$ kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at $C_{INT} = 1\ \mu F$ mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

DEVELOPMENT DATA

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

OPERATION (continued)

Table 5 Tuning window programming

TUW1	TUW0	|Δf| (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as |Δf| is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	|Δf| (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction byte POD (port output data) is shown in Fig. 5, together with the corresponding data/control byte. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

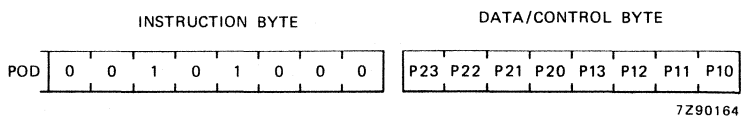


Fig. 5 Control programming.

OPERATION (continued)

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

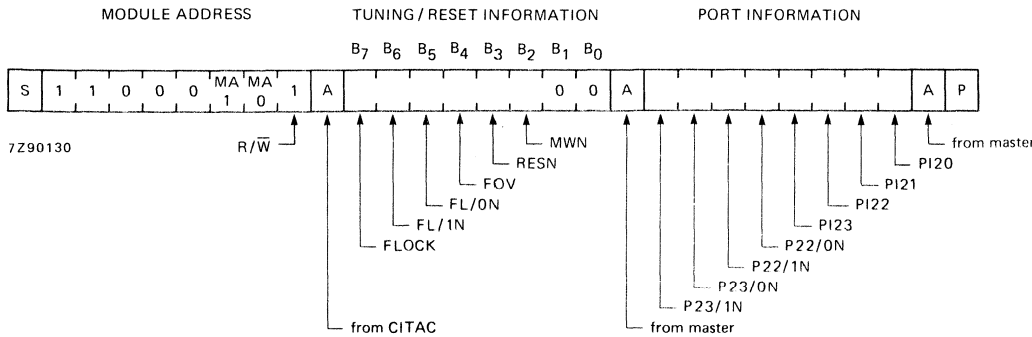


Fig. 6 Information byte format.

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

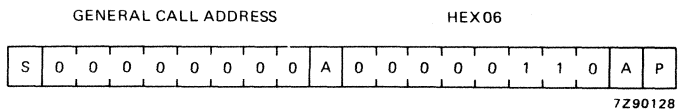


Fig. 7 Reset programming.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:		
(pin 5)	V_{P1}	−0,3 to + 18 V
(pin 14)	V_{P2}	−0,3 to + 18 V
(pin 9)	V_{P3}	−0,3 to + 36 V
Input/output voltage ranges:		
(pin 17)	V_{SDA}	−0,3 to + 18 V
(pin 18)	V_{SCL}	−0,3 to + 18 V
(pins 1 and 2)	$V_{P20, P21}$	−0,3 to + 18 V
(pins 3 and 4)	$V_{P22, P23, AFC}$	−0,3 to V_{P1}* V
(pin 6)	V_{TI}	−0,3 to V_{P1}* V
(pin 8)	V_{TUN}	−0,3 to V_{P3}* V
(pins 10 to 13)	V_{P1X}	−0,3 to V_{P2}** V
(pin 15)	V_{FDIV}	−0,3 to V_{P1}* V
(pin 16)	V_{OSC}	−0,3 to + 5 V
Total power dissipation	P_{tot}	max. 1000 mW
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature	T_{amb}	−20 to + 70 °C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.
** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	14	23	40	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	−2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	300	–	mW
Operating ambient temperature	T_{amb}	−20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 17); SCL input (pin 18)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 17, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 1 to 4, open collector)					
Input voltage HIGH (P20, P21)	V_{IH}	2	–	16	V
Input voltage HIGH (P22, P23) AFC switched off	V_{IH}	2	–	$V_{P1}-2$	V
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 3, 4)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current (P22 and P23 programmed HIGH)	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 6, 8)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 10 to 13)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 15)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	16	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 1) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

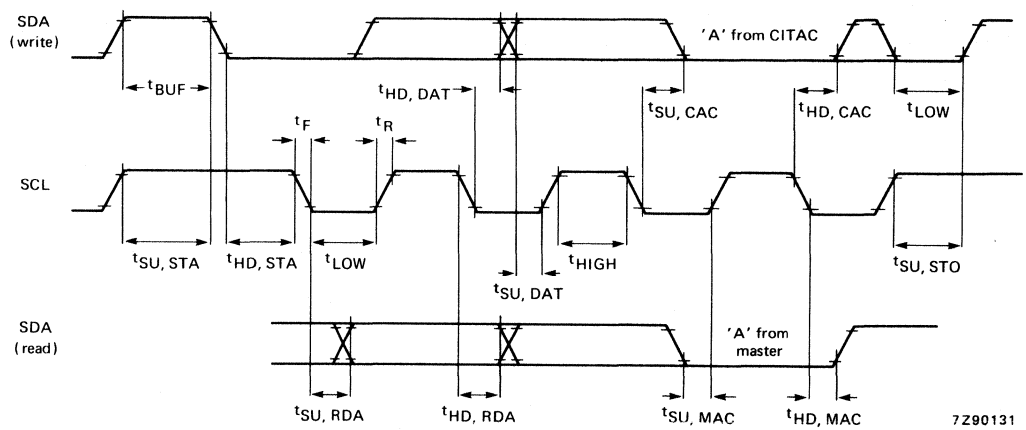


Fig. 8 I²C bus timing SAB3036.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3037 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 4 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 4 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 13)	V_{P1}	typ.	12 V
(pin 19)	V_{P2}	typ.	13 V
(pin 14)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 13)	I_{P1}	typ.	30 mA
(pin 19)	I_{P2}	typ.	0,1 mA
(pin 14)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	380 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

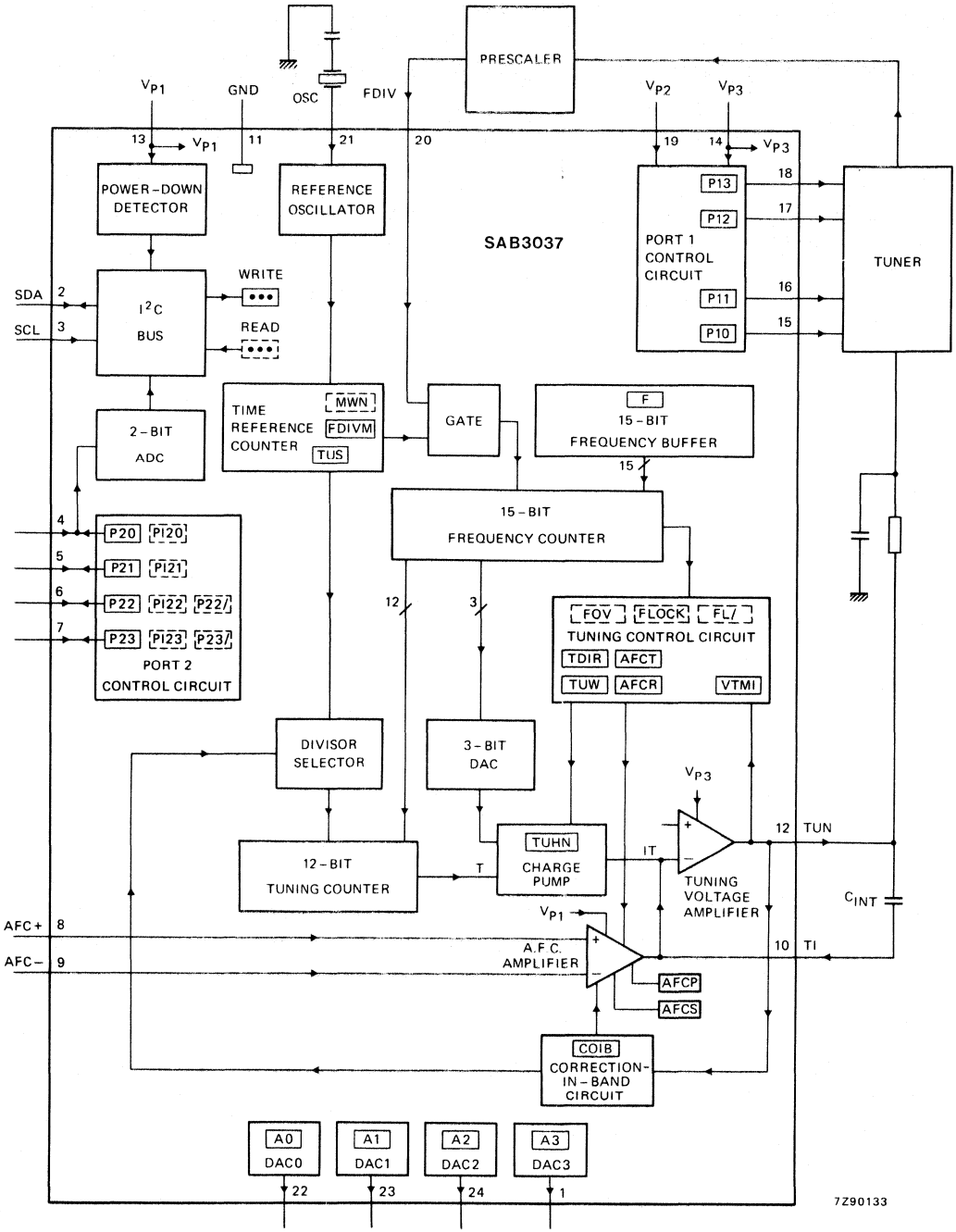


Fig. 1 Block diagram.

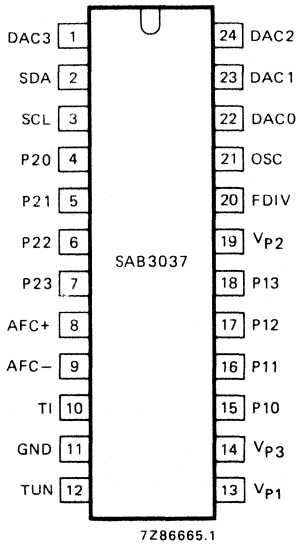
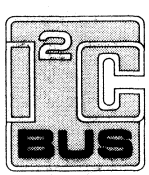


Fig. 2 Pinning diagram.

PINNING

1	DAC3	output of static DAC
2	SDA	serial data line (I²C bus)
3	SCL	serial clock line (I²C bus)
4	P20	general purpose input/output ports
5	P21	general purpose input/output ports
6	P22	general purpose input/output ports
7	P23	general purpose input/output ports
8	AFC+	a.f.c. inputs
9	AFC−	a.f.c. inputs
10	TI	tuning voltage amplifier inverting input
11	GND	ground
12	TUN	tuning voltage amplifier output
13	V_{P1}	+ 12 V supply voltage
14	V_{P3}	+ 32 V supply for tuning voltage amplifier
15	P10	high-current band-selection output ports
16	P11	high-current band-selection output ports
17	P12	high-current band-selection output ports
18	P13	high-current band-selection output ports
19	V_{P2}	positive supply for high-current band-selection output circuits
20	FDIV	input from prescaler
21	OSC	crystal oscillator input
22	DAC0	outputs of static DACs
23	DAC1	outputs of static DACs
24	DAC2	outputs of static DACs

DEVELOPMENT DATA



FUNCTIONAL DESCRIPTION

The SAB3037 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 $\mu A\ \mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250\ \mu A\ \mu s$ (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Four 6-bit digital-to-analogue converters DAC0 to DAC3 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

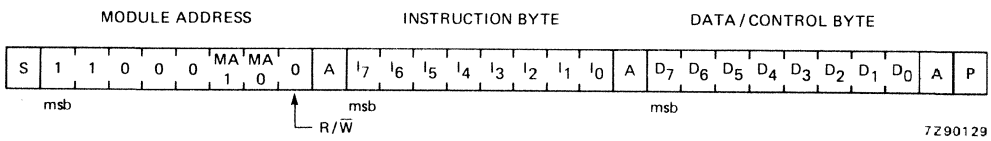


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

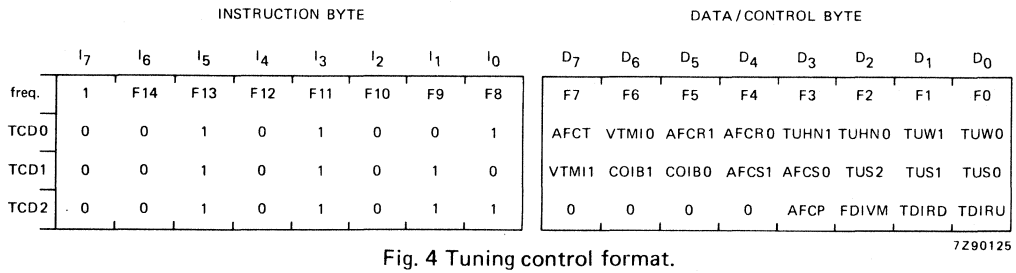


Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

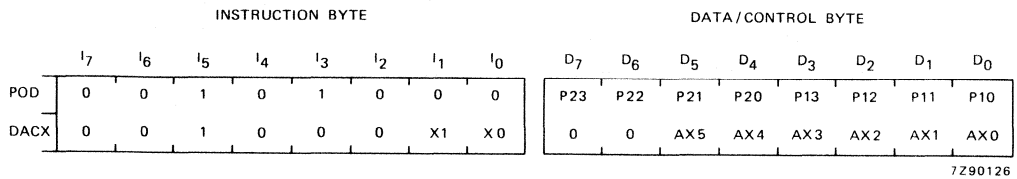


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

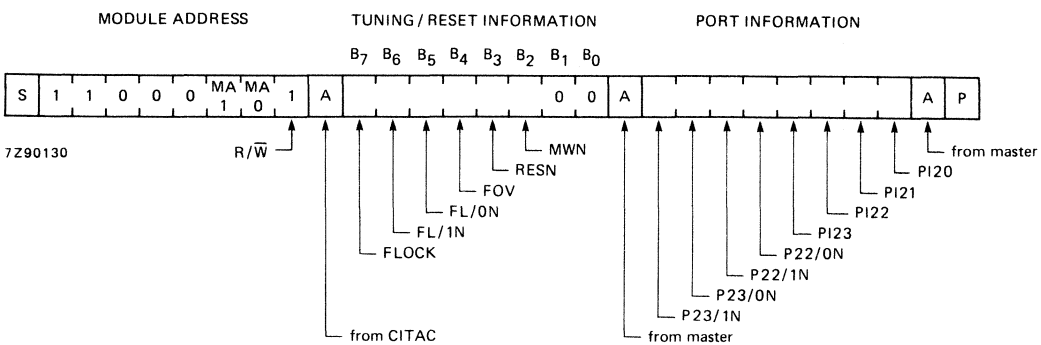


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

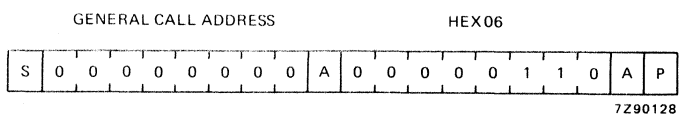


Fig. 7 Reset programming.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 13)	V_{P1}	−0,3 to +18	V
(pin 19)	V_{P2}	−0,3 to +18	V
(pin 14)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 2)	V_{SDA}	−0,3 to +18	V
(pin 3)	V_{SCL}	−0,3 to +18	V
(pins 4 to 7)	V_{P2X}	−0,3 to +18	V
(pins 8 and 9)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 10)	V_{TI}	−0,3 to V_{P1}*	V
(pin 12)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 15 to 18)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 20)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 21)	V_{OSC}	−0,3 to +5	V
(pins 1 and 22 to 24)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	18	30	45	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	−2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	380	–	mW
Operating ambient temperature	T_{amb}	−20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 2); SCL input (pin 3)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	−0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 2, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 4 to 7, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC− (pins 8, 9)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	−20	–	+20	%
Input offset voltage	V_{Ioff}	−75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 10, 12)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	−5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 15 to 18)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 20)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 21)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 3 (pins 22 to 24 and pin 1)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 4) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

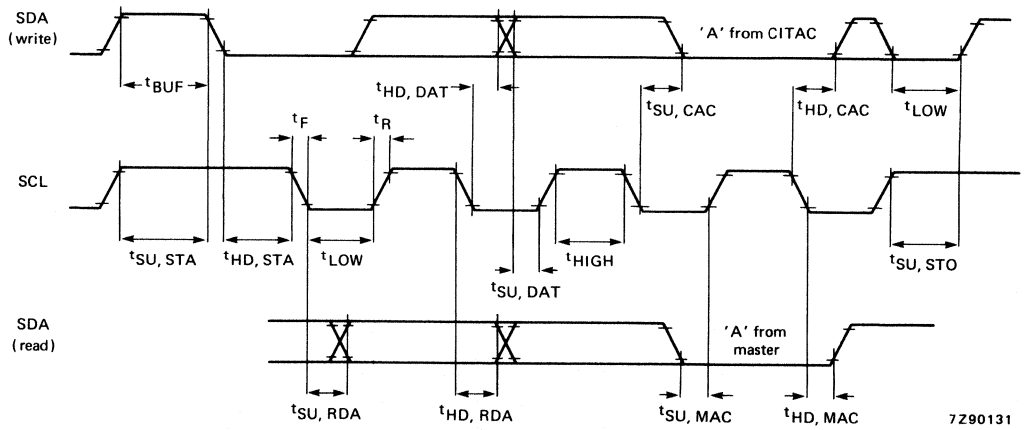


Fig. 8 I²C bus timing SAB3037.

SENSITIVE 1 GHz DIVIDE-BY-64/DIVIDE-BY-256 SWITCHABLE PRESCALER

GENERAL DESCRIPTION

The SAB6456/SAB6456T is a prescaler for UHF/VHF tuners. It can be switched to divide-by-64 or divide-by-256 by the mode-control (MC) pin. The circuit has an input frequency range of 70 MHz to 1 GHz, has high input sensitivity and good harmonic suppression.

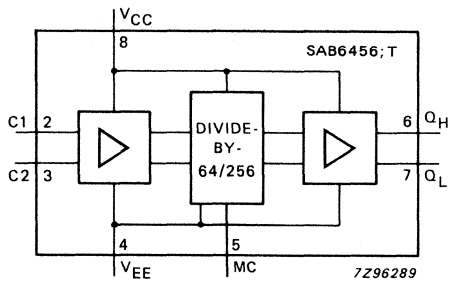


Fig. 1 Block diagram.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 8 to pin 4	V_{CC}	4,5	5,0	5,5	V
Supply current	pin 8	I_{CC}	–	21	–	mA
Input frequency range	pins 2 and 3	f_i	70	–	1000	MHz
Sensitivity to input voltage (r.m.s. value)		$V_{i(rms)}$	–	–	10	mV
Output voltage (peak-to-peak value)	pins 6 and 7	$V_{o(p-p)}$	–	1	–	V
Operating ambient temperature range		T_{amb}	0	–	80	°C

PACKAGE OUTLINES

SAB6456 : 8-lead DIL; plastic (SOT-97).
SAB6456T: 8-lead mini-pack (SO-8; SOT-96A).

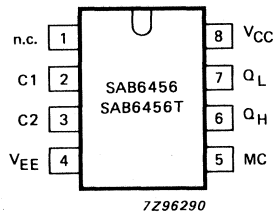


Fig. 2 Pinning diagram.

PINNING

1.	n.c.	not connected
2.	C1	differential inputs
3.	C2	
4.	V_{EE}	ground (0 V)
5.	MC	mode control
6.	Q_H	complementary outputs
7.	Q_L	
8.	V_{CC}	positive supply voltage

FUNCTIONAL DESCRIPTION

The circuit comprises an input amplifier, a divider stage with selectable division ratio and an output stage.

The input amplifier is driven by a sinusoidal signal from the local oscillator of a television tuner. The inputs (C1, C2) are differential and are biased internally to permit capacitive coupling. When driven asymmetrically the unused input should be connected to ground via a capacitor.

The mode-control (MC) input to the divider stage is intended for static control of the division ratio, selection is made as follows:

divide-by-64 : MC pin open-circuit

divide-by-256: MC pin connected to ground

The divider stage may oscillate during no-signal conditions but this oscillation is suppressed when input signals are received.

Two complementary signals (Q_H, Q_L) are provided by the output differential amplifier stage. The voltage-edges of the output signals are slowed internally to reduce harmonics in the television intermediate frequency band.

ELECTROSTATIC DISCHARGE PROTECTION

Inputs and outputs have electrostatic discharge protection according to specification MIL-883C, class B.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC-134)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 8 to pin 4	V_{CC}	–	–	7,0	V
Input voltage		V_i	–	–	V_{CC}	V
Storage temperature range		T_{stg}	−55	–	+150	°C
Junction temperature		T_j	–	–	+150	°C

THERMAL RESISTANCE

From junction to ambient

8-lead DIL; plastic (SOT-97A)	$R_{th\ j\text{-}a}$	120 K/W
8-lead mini-pack (SO-8; SOT-96A)		
on printed circuit board	$R_{th\ j\text{-}a}$	260 K/W
on ceramic substrate	$R_{th\ j\text{-}a}$	170 K/W

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; test IC mounted in a test socket or on a printed circuit board; measurements taken after thermal equilibrium is established

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC} −0,8	V
Supply current		I_{CC}	–	21	28	mA
Mode-control (MC)						
Input voltage LOW (divide-by-256)		V_{IL}	0	–	0,2	V
Input current LOW		$-I_L$	–	25	60	μA
Input voltage HIGH (divide-by-64)	pin 5 open-circuit	V_{IH}	1,4	–	3,0	V

A.C. CHARACTERISTICS

V_{CC} = 4,5 to 5,5 V; V_{EE} = 0 V; T_{amb} = 0 to +80 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity to input voltage (r.m.s. value)	50 Ω system					
	f_i = 70 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 150 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 300 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 500 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 900 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 1000 MHz	$V_{i(rms)}$	–	–	10	mV
Input overload voltage (r.m.s. value)	50 Ω system f_i = 70 MHz to 1000 MHz	V_i	300	–	–	mV
Input parallel resistance	f_i = 70 MHz	R_i	–	560	–	Ω
	f_i = 1000 MHz	R_i	–	30	–	Ω
Input capacitance	f_i = 70 MHz	C_i	–	5	–	pF
	f_i = 1000 MHz	C_i	–	1,5	–	pF
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC} –0,8	V
Output voltage swing (peak-to-peak value)	f_i = 70 MHz	$V_{o(p\text{-}p)}$	0,8	1,0	1,2	V
	f_i = 1000 MHz; R_L = 820 Ω; C_L = 60 pF	$V_{o(p\text{-}p)}$	0,17	–	–	V
Attenuation of third harmonic at output	f_i = 800 MHz; R_L = 820 Ω; C_L = 60 pF		–15	–23	–	dB
Output unbalance	see Fig. 3	ΔV_o	–	–	0,1	V
Output resistance		R_o	–	500	–	Ω

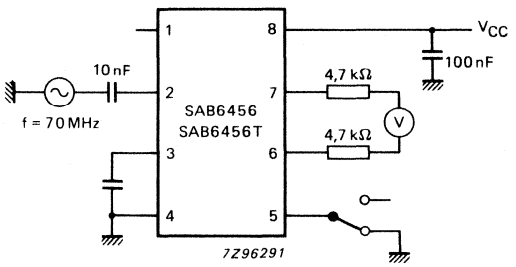


Fig. 3 Test circuit for output unbalance measurement.

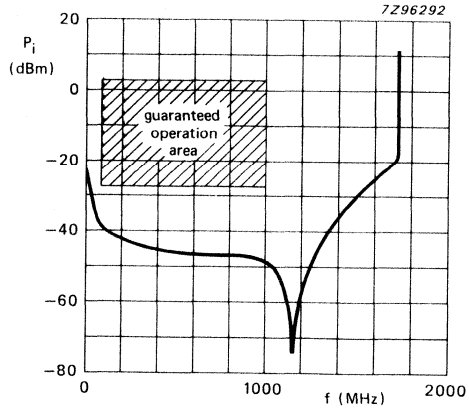


Fig. 4 Typical input sensitivity curve:
V_{CC} = 5 V; T_{amb} = 25 °C.

DEVELOPMENT DATA

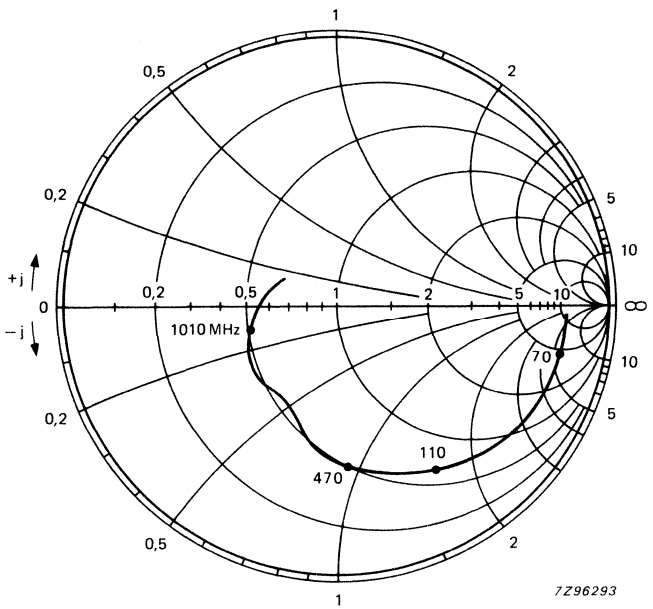


Fig. 5 Smith chart of typical input impedance:
$V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 50 Ω.

UNIVERSAL DAC (UDAC)

GENERAL DESCRIPTION

The SAD1009 is intended as a peripheral to a microcontroller-based servo system in video cassette recorders. The device relieves the microcontroller of some of the real time functions. These functions include; generation of programmable pulse width signals (duty factor etc.) and accurate measurement of time period signals (tacho signal etc.). The SAD1009 has nine programmable output ports. All functions of the UDAC are programmable. Commands and data from the microcontroller are loaded via a bidirectional bus using a 16-bit format. Data from the time period measurement is transferred to the microcontroller via the same bidirectional bus, also using a 16-bit format. The clock signal for this device is provided by the quartz oscillator of the microcontroller.

Features

- Generation of programmable pulse width signals
- Measurement of time period signals
- All functions are programmable

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4,75	5,0	5,25	V
Inputs						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current		$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
Outputs						
Output voltage						
LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = −1,0 mA	V_{OH}	V_{DD} −0,4	–	–	V
Output sink current		I_O	–	–	1,6	mA
Output source current		$-I_O$	–	–	1,0	mA

PACKAGE OUTLINES

SAD1009P: 24-lead DIL; plastic (SOT-101A).
SAD1009T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

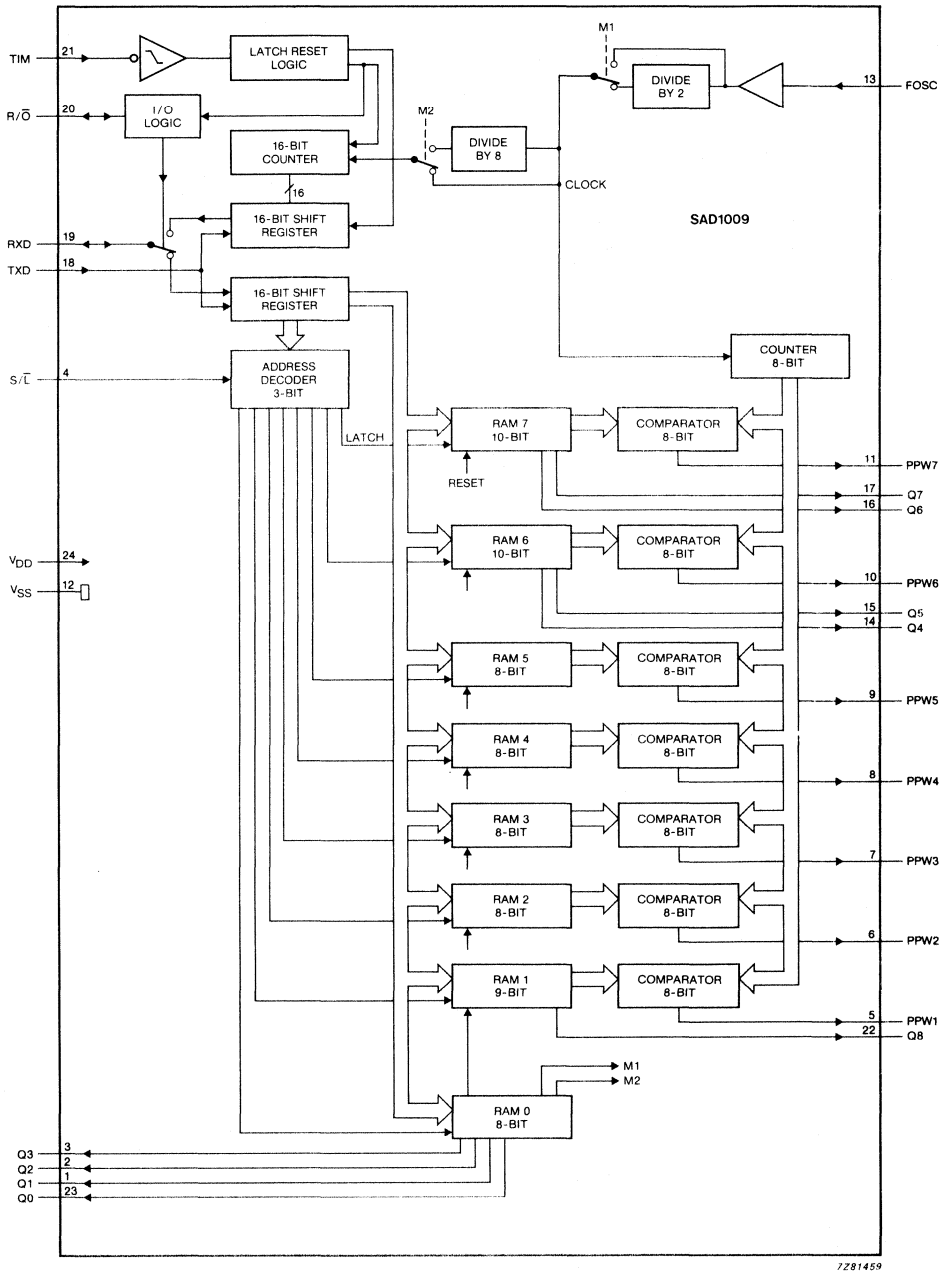


Fig. 1 Block diagram.

PINNING

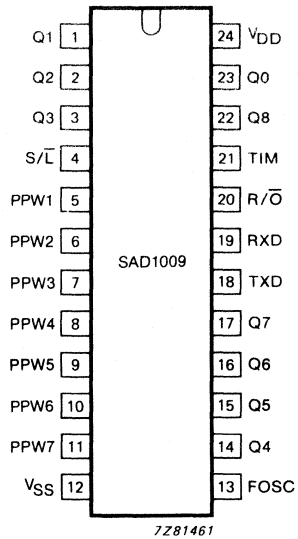


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

Power supply

V_{DD}	positive supply voltage (+5 V)
V_{SS}	ground (0 V)

Inputs

S/$\overline{L}$	shift/$\overline{\text{latch}}$ input
FOSC	oscillator input
TXD	serial clock

Special inputs

TIM	timer input

Outputs

Q0 to Q8	programmable output ports
PPW1 to PPW7	programmable pulse width outputs

Input/outputs

RXD	serial data
R/$\overline{O}$	handshake

FUNCTIONAL DESCRIPTION

Loading data

All commands and data are loaded into the SAD1009 via the bidirectional bus (TXD, RXD). The bidirectional bus is compatible with the serial interface of the '8051' microcontroller, using mode 0.

A 16-bit word is used to program a function of the UDAC. The first 3-bits received from the RAM constitute the address and the remaining 13-bits are data (LSB first, MSB last). None of the functions require all 13-bits of data, therefore, 16-bit words contain a number of immaterial bits (x). The programming format is shown in Table 1.

To shift a program word into the input buffer of the UDAC the S/$\overline{L}$ line (shift/latch not) must be HIGH. The contents of the input buffer are transferred to the appropriate RAM on the HIGH-to-LOW transition of the S/$\overline{L}$ signal. When S/$\overline{L}$ is LOW the input buffer is disabled and cannot accept new incoming information. Fig. 3 illustrates the program reception cycle.

Table 1 Programming format

bit	status	PPW1	PPW2	PPW3	PPW4	PPW5	PPW6	PPW7
1	L	H	L	H	L	H	L	H
2	L	L	H	H	L	L	H	H
3	L	L	L	L	H	H	H	H
4	$\overline{\text{RESET}}$	Q8	X	X	X	X	Q4	Q6
5	X	X	X	X	X	X	Q5	Q7
6	X	X	X	X	X	X	X	X
7	X	X	X	X	X	X	X	X
8	X	X	X	X	X	X	X	X
9	Q0	D8	D8	D8	D8	D8	D8	D8
10	Q1	D7	D7	D7	D7	D7	D7	D7
11	Q2	D6	D6	D6	D6	D6	D6	D6
12	Q3	D5	D5	D5	D5	D5	D5	D5
13	X	D4	D4	D4	D4	D4	D4	D4
14	X	D3	D3	D3	D3	D3	D3	D3
15	M1	D2	D2	D2	D2	D2	D2	D2
16	M2	D1	D1	D1	D1	D1	D1	D1

Where:

X : don't care
D1 to D8: data for programming pulse width, D1 = MSB and D8 = LSB

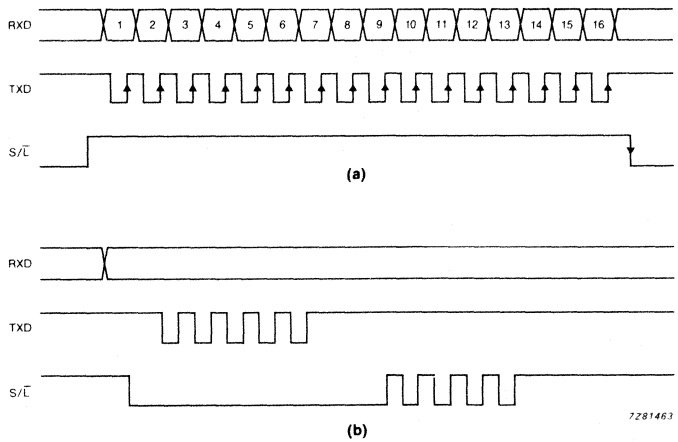


Fig. 3 Program reception cycle: a) normal reception cycle; b) no information is loaded into the input buffer, the RAMs contents remain unchanged.

Pulse width modulated outputs

The UDAC has seven pulse width modulated outputs (PPW1 to PPW7). The output PPW1 is slightly different to outputs PPW2 to PPW7, the difference is explained below. Each output produces a pulse width modulated signal with a duty factor programmable in steps of 1/256 and has a repetition frequency of approximately 23 kHz. These pseudo analogue signals are used to control the capstan and reel drives. Motor control can be performed in the following ways:

- convert the pulse width modulated signal into an analogue signal using filtering and analogue power amplification
- by feeding the pulse width modulated signal to the motor via a power switch and a switch mode filter

To conserve power use the second method for control of the capstain and reel motors. For the scanner control two outputs are available, so that by weighted addition a higher resolution can be achieved.

PPW1 is also an 8-bit programmable output, with a repetition frequency of 23 kHz. The difference is the low frequency contents of the signal are reduced by changing the distribution of the HIGH and LOW level portions. This redistribution means that a filter with two poles; each at 43 μs, is sufficient to reduce the peak-to-peak ripple to less than 1 LSB. This output is for use in applications where long filter delays are not tolerated.

Clock frequency

The clock signal of the UDAC is derived from the quartz oscillator of the microcontroller. The clock frequency should not exceed 6 MHz. The device also contains a programmable 'divide by two' circuit which allows these frequencies to be doubled, thus 6 MHz or 12 MHz microcontrollers can be used. The FOSC signal can be divided by two using bit M1 of RAM 0 (see Table 2).

Table 2 UDAC adjustment

bit M1	quartz frequency (MHz)
H	12
L	6

Programmable output ports

A total of nine output ports can be programmed to supply a HIGH or LOW level signal. Four of these outputs (Q4 to Q7) are intended to supply information about the breaking and direction of the capstan and reel motors, therefore these output ports must be programmed at the same time as the pulse widths of PPW6 and PPW7. Output port Q8 is programmed at the same time as PPW1. The other four output ports (Q0 to Q3) are programmed by RAM 0.

Measurement of the time period

To facilitate accurate measurement of the time period (falling edge to falling edge) of a signal applied to TIM, the UDAC contains a 16-bit counter and a buffer to store the contents of the previous counter measurement. The counter operates at a frequency of $f_{CLOCK}/2$ or $f_{CLOCK}/16$, the counter can be programmed using bit M2 of RAM 0. This timer can record periods of up to 21,8 ms and 175 ms respectively (see Table 3). When the time period is too long and the timer overflows, the microcontroller is loaded with a hex 'FFFF' when it reads the time period after the next pulse.

Table 3 Counter frequency

M2	division ratio	time period (max.)	frequency	resolution
L	2	21,8 ms	46 Hz	333 ns
H	6	175 ms	5,7 Hz	2,67 μs

Data from the timer can be transferred to the microcontroller via a bidirectional bus when the handshaking signal pin R/$\overline{O}$ is pulled LOW by the microcontroller. The LSB is transferred first and the MSB last. After the data has been transferred pin R/$\overline{O}$ remains in a LOW state (pulled down by the UDAC) until a new measurement of the time period is concluded. Note that each measurement of a time period can only be read once. After the next input pulse the 'data ready' state is signalled to the microcontroller by releasing the R/$\overline{O}$ pin, so that the microcontroller reads a HIGH level on this pin.

Note

During the 'data not ready' state the R/$\overline{O}$ is in a low impedance state and during the 'data ready' state the R/$\overline{O}$ is in a high impedance state (= HIGH). To speed up the transition from LOW-to-HIGH, the high impedance state is preceded by a short period of low impedance HIGH state.

Reset

The device can be reset by software by loading a LOW into the $\overline{\text{RESET}}$ bit of RAM 0. The effect of this reset is as follows:

- RAM 0; not influenced
- RAM 1; duty factor = 50%, Q8 = LOW
- RAM 2 to 5; duty factor = 50%
- RAM 6 to 7; duty factor = 0 and Q4 to Q7 = LOW

The reset is de-activated automatically on the next LOW-to-HIGH transition of S/$\overline{L}$. This allows new program information to be loaded and transferred to any RAM without having finished the reset. Due to RAM 0 not being influenced by the reset, the data required after the reset can be loaded along with the reset command.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	–	7	V
Input voltage range	note 1	V_I	−0,5	V_{DD} + 0,5	V
Input voltage at S/$\overline{L}$		$V_{4\text{-}12}$	−0,5	V_{DD} + 2,0	V
D.C. current into any input		$\pm I_I$	–	10	mA
D.C. current from any output		$\pm I_O$	–	10	mA
D.C. current into V_{DD}		$\pm I_I$	–	25	mA
D.C. current into V_{SS}		$\pm I_I$	–	25	mA
Total power dissipation	note 2	P_{tot}	–	200	mW
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−20	+70	°C

Notes to ratings

1. Input voltage should not exceed 7 V unless otherwise specified.
2. Diminishes by 5 mW/K from 60 °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 4,75 to 5,25 V; T_{amb} = −20 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4,75	5,0	5,25	V
Supply current range	$V_O = V_{DD}$, I_O = 0 mA on all outputs; $V_I = V_{SS}$ on all inputs	I_{DD}	–	100	–	μA
TXD, RXD, S/$\overline{L}$, R/$\overline{O}$						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current	note 1	$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
RXD, R/$\overline{O}$, Q0 to Q7						
Output voltage	note 2					
LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = −1,0 mA	V_{OH}	V_{DD}−0,4	–	–	V
Output sink current		I_O	–	–	1,6	mA
Output source current		$-I_O$	–	–	1,0	mA
FOSC						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current		$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF

D.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RXD	used as input					
Input leakage current		$\pm I_I$	–	–	10	μA
TIM						
Input voltage						
LOW		V_{IL}	–	–	$0,3xV_{DD}$	V
LOW	V_{DD} = 5 V at 20 °C	V_{IL}	–	1,8	–	V
HIGH		V_{IH}	$0,7xV_{DD}$	–	–	V
HIGH	V_{DD} = 5 V at 20 °C	V_{IH}	–	2,9	–	V
Hysteressis	used as input	V_{hys}	–	730	–	mV
R/$\overline{O}$	used as input					
Output resistance		R_O	500	–	1000	Ω
Input leakage current		$\pm I_I$	–	–	10	μA
R/$\overline{O}$	used as output; open drain output; note 3; see Fig. 7					
Output voltage						
LOW	I_{OL} = 0,4 mA	V_{OL}	–	–	0,8	V
HIGH	I_{OH} = –0,4 mA	V_{OH}	$V_{DD}-0,8$	–	–	V
PPW1 to PPW7						
Output voltage						
LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = –4 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output sink current		I_O	–	–	4	mA
Output source current		$-I_O$	–	–	4	mA

Notes to the d.c. characteristics

1. This value applies to TXD and S/$\overline{L}$, the input leakage current for RXD and R/$\overline{O}$ is shown above.
2. This value applies to RXD and Q0 to Q7, the output voltage for R/$\overline{O}$ is shown above.
3. After a LOW-to-HIGH transition of the R/$\overline{O}$ output, the port is held HIGH for approximately one clock cycle. This low impedance HIGH period is followed by the high impedance OFF-state.

DEVELOPMENT DATA

A.C. CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
RXD, R/$\overline{O}$, Q0 to Q7						
Output transition time	C_L = 50 pF					
LOW-to-HIGH		t_{TLH}	–	–	30	ns
HIGH-to-LOW		t_{THL}	–	–	30	ns
FOSC						
Maximum pulse frequency	M1 = L	f_{max}	–	–	12	MHz
	M1 = H	f_{max}	–	–	6	MHz
Minimum pulse width						
LOW		t_{WL}	20	–	–	ns
HIGH		t_{WH}	20	–	–	ns
TXD						
Pulse frequency		f_{max}	–	–	6	MHz
Pulse width						
LOW		t_{WL}	50	–	–	ns
HIGH		t_{WH}	50	–	–	ns
RXD	used as input; see Fig. 5					
Set-up time						
RXD to TXD		t_{SURXD}	50	–	–	ns
Hold time						
RXD to TXD		t_{HDRXD}	50	–	–	ns
RXD	used as output; see Fig. 6					
Propagation delay						
TXD to RXD		t_{PRXD}	–	–	50	ns
R/$\overline{O}$ to RXD		$t_{PR/O}$	–	–	50	ns
S/$\overline{L}$	see Fig. 7					
Pulse width LOW						
Set-up time						
TXD to S/$\overline{L}$		t_{SUTXD}	50	–	–	ns
Hold time						
TXD to S/$\overline{L}$		t_{HDTXD}	50	–	–	ns
Propagation delay						
S/$\overline{L}$ to Q0 - Q7		t_p	–	–	50	ns
TIM						
Pulse width						
LOW	M2 = LOW	t_{WL}	700	–	–	ns
LOW	M2 = HIGH	t_{WL}	5,4	–	–	μs
HIGH		t_{WH}	100	–	–	ns

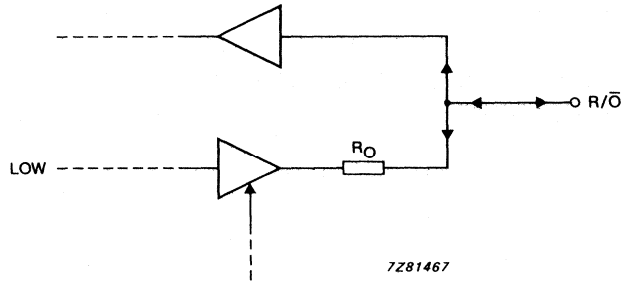


Fig. 4 Equivalent R/$\overline{O}$ output port.

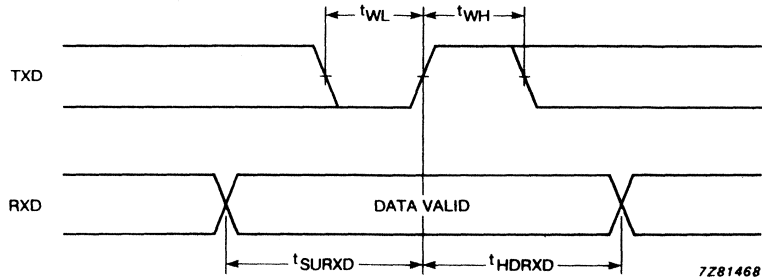


Fig. 5 RXD input waveform.

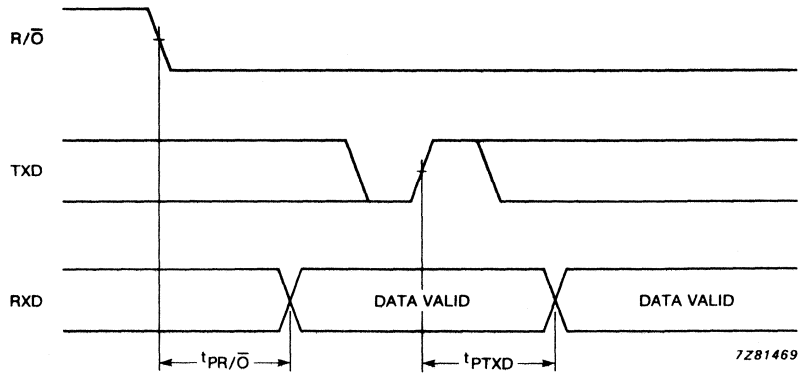


Fig. 6 RXD output waveform.

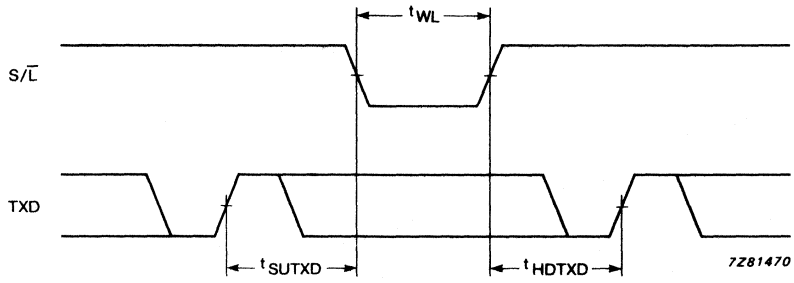


Fig. 7 S/$\overline{L}$ input waveform.

AUTOMATIC TRACKING OSCILATOR AND DIGITAL-TO-ANALOGUE CONVERTER (ATO/DAC)

GENERAL DESCRIPTION

The SAD1010 is intended as a peripheral to a microcontroller-based servo system in video cassette recorders. The device performs the functions which the microcontroller is unfit to carry out. These functions include; generation of a reference signal for PCM audio recording, generation of programmable pulse width signals (duty factor etc.), generation of the pilot signal and the measurement of time period signals (tacho signal etc.). The SAD1010 has nine programmable output ports, of which one output port provides a 62,5 kHz signal. All functions of the ATO/DAC are programmable. Commands and data from the microcontroller are loaded via a bidirectional bus, using a 16-bit format. The clock signal for this device may be provided by the quartz oscillator of the microcontroller.

Features

- Generation of reference signal for PCM audio recording
- Generation of programmable pulse width signals
- Generation of the pilot signal
- Measurement of time period signals
- All functions are programmable

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4,75	5,0	5,25	V
Inputs						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current		$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
Outputs						
Output voltage						
LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = −1,0 mA	V_{OH}	V_{DD}−0,4	–	–	V
Output sink current		I_O	–	–	1,6	mA
Output source current		$-I_O$	–	–	1,0	mA

PACKAGE OUTLINES

SAD1010P: 28-lead DIL; plastic (SOT-117).
SAD1010T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

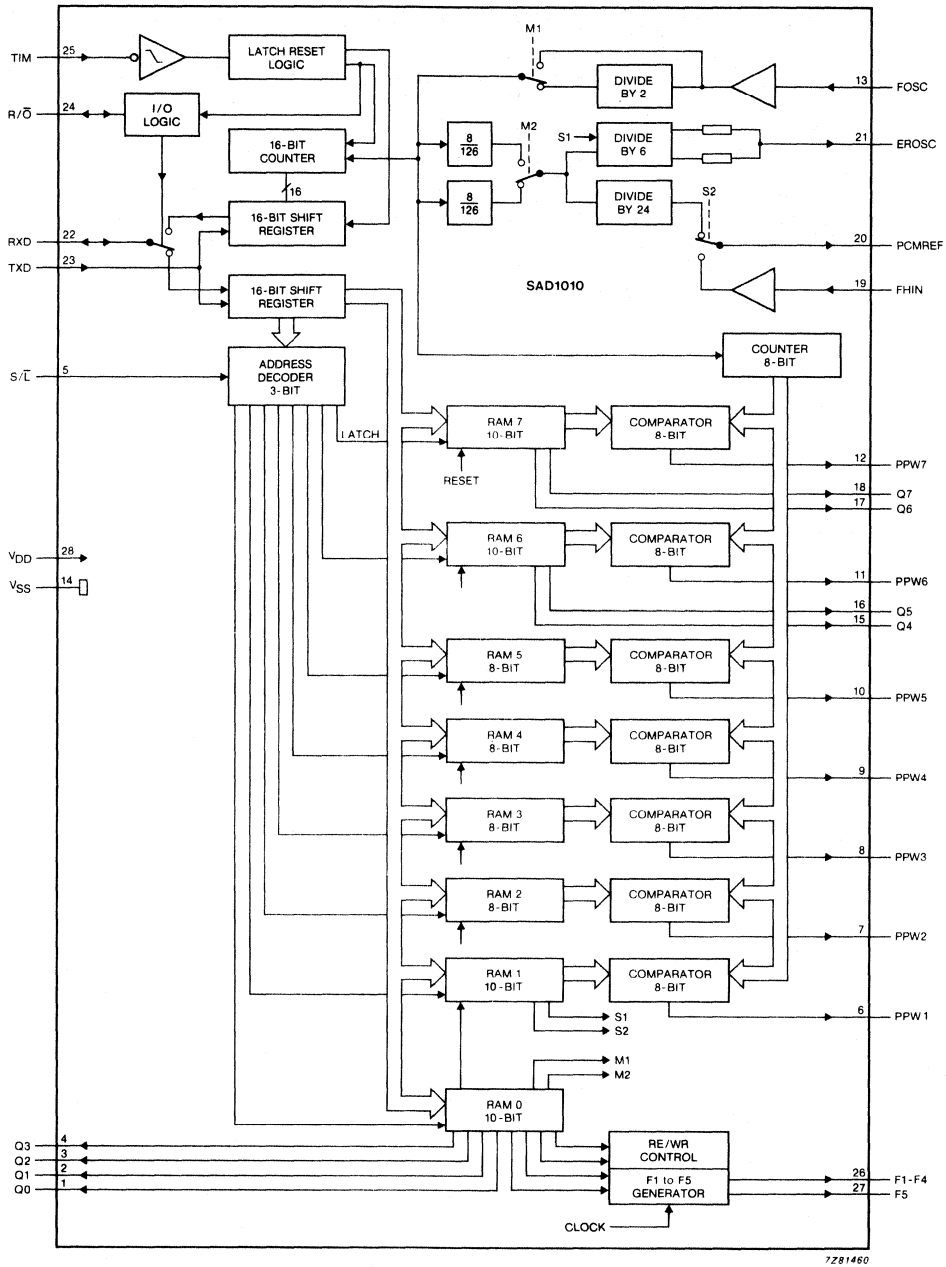


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

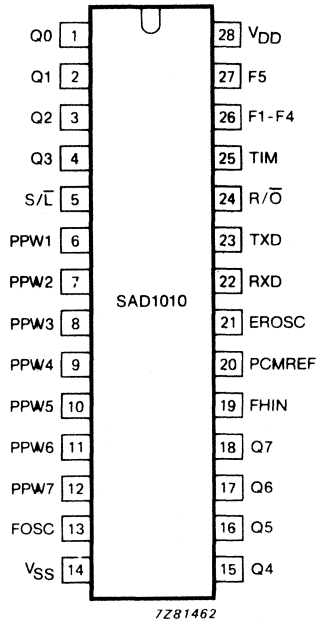


Fig. 2 Pinning diagram.

Power supply

V_{DD}	positive supply voltage (+5 V)
V_{SS}	ground (0 V)

Inputs

S/$\overline{L}$	shift/$\overline{\text{latch}}$ input
FOSC	oscillator input
TXD	serial clock

Special inputs

FHIN	frequency input (high voltage)
TIM	timer input

Outputs

Q0 to Q7	programmable output ports
PPW1 to PPW7	programmable pulse width outputs
PCMREF	PCM reference output

3-state output

F5	pilot signal output

Analogue outputs

EROSC	erase oscillator output
F1-4	pilot signal outputs

Input/outputs

RXD	serial data
R/$\overline{O}$	handshake

FUNCTIONAL DESCRIPTION

Loading data (see Table 1)

All commands and data are loaded into the SAD1010 via the bidirectional bus (TXD, RXD). The bidirectional bus is compatible with the serial interface of the '8051' microcontroller, using mode 0.

A 16-bit word is used to program a function of the ATO/DAC. The first 3-bits received from the RAM constitute the address and the remaining 13-bits are data (LSB first, MSB last). A majority of the functions do not require all 13-bits of data, therefore, a number of 16-bit words contain immaterial bits (X).

To shift a program word into the input buffer of the ATO/DAC the S/$\overline{L}$ line (shift/latch not) must be HIGH. The contents of the input buffer are transferred to the appropriate RAM on the HIGH-to-LOW transition of the S/$\overline{L}$ signal. When S/$\overline{L}$ is LOW the input buffer is disabled and cannot accept new incoming information. Fig. 3 illustrates the program reception cycle.

Table 1 Programming format

bit	status	PPW1	PPW2	PPW3	PPW4	PPW5	PPW6	PPW7
1	L	H	L	H	L	H	L	H
2	L	L	H	H	L	L	H	H
3	L	L	L	L	H	H	H	H
4	$\overline{\text{RESET}}$	S1	X	X	X	X	Q4	Q6
5	FSEL0	S2	X	X	X	X	Q5	Q7
6	FSEL1	X	X	X	X	X	X	X
7	WR	X	X	X	X	X	X	X
8	RE	X	X	X	X	X	X	X
9	Q0	D8	D8	D8	D8	D8	D8	D8
10	Q1	D7	D7	D7	D7	D7	D7	D7
11	Q2	D6	D6	D6	D6	D6	D6	D6
12	Q3	D5	D5	D5	D5	D5	D5	D5
13	X	D4	D4	D4	D4	D4	D4	D4
14	X	D3	D3	D3	D3	D3	D3	D3
15	M1	D2	D2	D2	D2	D2	D2	D2
16	M2	D1	D1	D1	D1	D1	D1	D1

Where:

X: don't care
D1 to D8: data for programming pulse width, D1 = MSB and D8 = LSB

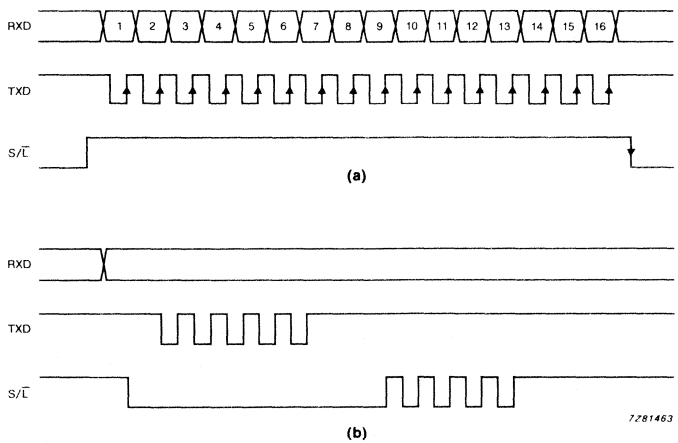


Fig. 3 Program reception cycle: a) normal reception cycle; b) no information is loaded into the input buffer, the RAMs contents remain unchanged.

DEVELOPMENT DATA

Pulse width modulated outputs

The ATO/DAC has seven pulse width modulated outputs. Each output produces a pulse width modulated signal with duty factor programmable in steps of 1/256 and has a repetition frequency of approximately 23 kHz. These pseudo analoque signals are used to control the actuator deflection, DTF analoque-to-digital conversion and the motors of the scanners, capstan and reel drives. Motor control can be performed in the following ways:

- convert the pulse width modulated output into an anlogue signal using filtering and analogue power amplification
- by feeding the pulse width modulated output to the motor via a power switch and a switch mode filter.

To conserve power use the second method for control of the capstain and reel motors. For the scanner control two outputs are available, so that by weighted addition a higher resolution can be achieved.

The PPW1 signal is used to compare the analogue tracking signal (read from tape) with the expected signal, which is stored as a digital value in the microcontroller. The PPW1 signal is converted into an analogue signal via a filter and is then fed to a comparator. To simplify the filtering, the low frequency contents of the signal are reduced by changing the distribution of the HIGH and LOW level portions. The average duty factor is not affected by this redistribution. The redistribution means that a filter with two poles, each at 43 μs, is sufficient to reduce the peak-to-peak ripple to less than 1 LSB.

Clock frequency

The clock signal of the ATO/DAC is derived from the quartz oscillator of the microcontroller. The quartz frequency must be of a value that allows the pilot frequencies to be derived by integer division. This means that the clock frequency must be 375 x horizontal scan frequency for 625 line mode or 378 x horizontal scan frequency for 525 line mode. The device also contains a 'divide by two' circuit which allows these frequencies to be doubled, thus 6 MHz or 12 MHz microcontrollers can be used.

2-bits of the RAM 0 data are used to adjust the ATO/DAC to the required quartz frequency (see Table 2).

Table 2 ATO/DAC adjustment

bits		line mode	quartz frequency MHz
M2	M1		
L	L	625	11,718750
L	H	625	5,859375
H	L	525	11,895104
H	H	525	5,947552

Pilot signal

The DFT tracking system requires 5 different pilot signals (F1 to F5). F1 to F4 are used for playback tracking and F5 is used for head adjustment during recording. The correct frequencies are obtained by dividing the clock signal (see Table 3).

Table 3 Pilot frequencies

signal	division ratio	frequency (kHz)	
		625 mode	525 mode
F1	58	101	103
F2	50	117	119
F3	36	163	165
F4	40	146	149
F5	26	225	229

The selection of F1 to F4 is controlled by RAM 0, bits FSEL0 and FSEL1. The read or write sequence of F5 is controlled by bits RE and WR (see Table 4).

Table 4 Selection of F1 to F5

RE	WR	FSEL1	FSEL0	F1 to F4	F5
L	L	L	L	F4	Z
L	L	L	H	F1	Z
L	L	H	L	F2	Z
L	L	H	H	F3	Z
L	H	X	X	d.c.	F5
H	L	X	X	d.c.	Z
H	H	X	X	d.c.	Z

Where:

X = don't care
Z = high impedance OFF-state
d.c = low impedance OFF-state

Signals F1 to F4 must be filtered to avoid disturbances of the video and audio signals. F1 to F4 provide a multi-level signal and all harmonics up to 1,1 MHz on this signal are reduced to a maximum of −20 dB so that a simple filter is sufficient.

PCM reference

The PCM audio circuit requires a line frequency signal for reference. The requirements of this signal vary according to the type of operation (record/playback):

- During record the reference signal must be locked to the incoming video signal. Due to the output voltage levels involved a special input port (FHIN) which can handle signals of up to 13 V is used.
- During playback the reference signal is derived from the same source as the drum reference signal i.e. the microcontroller quartz. Therefore the clock signal divided by 375 (CCIR) or 378 (NTSC) can be used as the playback reference.

Switching between record and playback reference is controlled by bit S2 of RAM 1:

- S2 = L, reference from microcontroller quartz (playback)
- S2 = H, reference from input port FHIN (record)

Programmable output ports

A total of eight output ports can be programmed to supply a HIGH or LOW level signal. Four of these outputs (Q4 to Q7) supply information about the braking and direction of the capstan and reel motors, therefore these output port must be programmed at the same time as the pulse widths of PPW6 and PPW7. The four output ports (Q0 to Q3) are programmed by RAM 0.

EROSC output

The quartz clock is divided to form a stable 62,5 kHz signal which can be fed to the erase oscillator and the actuator end stages. To reduce the third harmonic this signal has three levels. The signal is disabled when S1 of RAM 1 = LOW.

Note

As the 62,5 kHz (4 x horizontal scan frequency) signal is derived from the clock (375 x horizontal scan frequency signal for 625 line mode or 378 x horizontal scan frequency for 525 line mode) by non-integer division some jitter occurs. The peak-to-peak jitter is 170 ns.

DEVELOPMENT DATA

Measurement of the time period

To facilitate accurate measurement of the time period (falling edge to falling edge) of a signal applied to TIM, the ATO/DAC contains a 16-bit counter which operates at a frequency of $f_{CLOCK}/2$ and a buffer to store the contents of the previous counter measurement. This timer can record period of up to 22 ms (max.) e.g. a frequency of 45 Hz can be measured with a resolution of 340 ns. When the time period exceeds 22 ms the timer overflows. In this situation the microcontroller is loaded with a hex 'FFFF' when it reads the time period after the next pulse.

Data from the timer can be transferred to the microcontroller via a bidirectional bus when the handshaking signal pin $R/\overline{O}$ is pulled LOW by the microcontroller. The LSB is transferred first and the MSB last. After the data has been transferred pin $R/\overline{O}$ remains in a LOW state (pulled down by the ATO/DAC) until a new measurement of the time period is concluded. Note that each measurement of a time period can only be read once. After the next input pulse the 'data ready' state is signalled to the microcontroller by releasing the $R/\overline{O}$ pin, so that the microcontroller reads a HIGH level on this pin.

Note

During the 'data not ready' state the $R/\overline{O}$ is in a low impedance state and during the 'data ready' state the $R/\overline{O}$ is in a high impedance state. To speed up the transition from LOW-to-HIGH, the high impedance state is preceded by a short period of low impedance HIGH state.

Reset

The device can be reset by software by loading a LOW into the $\overline{RESET}$ bit of RAM 0. The effect of this reset is as follows:

- RAM 0; not influenced
- RAM 1; duty factor = 1/2, PCMREF = quartz reference and EROSC = OFF = LOW
- RAM 2 to 5; duty factor = 1/2
- RAM 6 to 7; duty factor = 0 and Q4 to Q7 = LOW

The reset is de-activated automatically on the next LOW-to-HIGH transition of $S/\overline{L}$. This allows new program information to be loaded and transferred to any RAM without having to end the reset first. Due to RAM 0 not being influenced by the reset, the data required after the reset can be loaded along with the reset command.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	–	7,0	V
Input voltage range	note 1	V_I	−0,5	V_{DD} + 0,5	V
Input voltage at S/$\overline{L}$		$V_{5\text{-}14}$	−0,5	V_{DD} + 2,0	V
Input voltage at FHIN		$V_{19\text{-}14}$	−0,5	V_{DD} + 8,0	V
D.C. input current		$\pm I_I$	–	10	mA
D.C. output current		$\pm I_O$	–	10	mA
Total power dissipation		P_{tot}	–	200	mW
Storage temperature range		T_{stg}	−55	+150	°C

Note to ratings

1. Input voltage should not exceed 7 V unless otherwise specified.

DEVELOPMENT DATA

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

V_{DD} = 4,75 to 5,25 V; T_{amb} = −20 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4,75	5,0	5,25	V
Supply current range	$V_O = V_{DD}$, I_O = 0 mA on all outputs and $V_I = V_{SS}$ on all inputs, except FOSC; 12 MHz; M1 = L	I_{DD}	–	2,6	–	mA
TXD, RXD, S/$\overline{L}$						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current		$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
RXD, PCMREF, Q0 to Q7, F5						
Output voltage						
LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = −1,0 mA	V_{OH}	V_{DD}−0,4	–	–	V
Output sink current		I_O	–	–	1,6	mA
Output source current		$-I_O$	–	–	1,0	mA
FOSC						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
Input leakage current		$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
FHIN						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input voltage		V_I	0	–	13	V
Input current	V_I = 13	I_I	–	–	0,2	mA
Input leakage current	$V_{SS} < V_I < V_{DD}$	$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
EROSC	see Fig. 4					
Output voltage level						
HIGH	I_O = 0 mA	V_{OH}	–	V_{DD}–0,2	–	V
MIDDLE	I_O = 0 mA	V_{OM}	–	½ V_{DD}	–	V
LOW	I_O = 0 mA	V_{OL}	–	0,2	–	V
Mid-level deviation	note 2	ΔV_{OM}	–	–	100	mV
Output resistance		R_O	3,5	5,0	6,5	kΩ
TIM						
Input voltage						
LOW		V_{IL}	–	–	1,2	V
LOW	V_{DD} = 5 V at 20 °C	V_{IL}	–	1,8	–	V
HIGH		V_{IH}	3,4	–	–	V
HIGH	V_{DD} = 5 V at 20 °C	V_{IH}	–	2,9	–	V

DEVELOPMENT DATA

D.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Hysteressis		V_{hys}	–	730	–	mV
R/$\overline{O}$	used as output, open drain output, note 3, see Fig. 5					
Output voltage						
LOW	I_{OL} = 0,4 mA	V_{OL}	–	–	0,8	V
HIGH	I_{OH} = 0,4 mA	V_{OH}	V_{DD}–0,8	–	–	V
Output resistance		R_O	500	–	1000	Ω
PPW1 to PPW7						
Output voltage						
LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = –4 mA	V_{OH}	V_{DD}–0,4	–	–	V
Output sink current		I_O	–	–	4	mA
Output source current		$-I_O$	–	–	4	mA
F1 to F4	see Fig. 6, all output voltage levels measured at I_O = 0 mA					
Output voltage						
level 1		V_{O1}	–	0,2	–	V
level 2 to 5 and 7				see note 4		
level 6		V_{O6}	–	V_{DD}–0,2	–	V
Output resistance		R_O	2,5	3,7	4,8	kΩ
F5	see Fig. 7					
High impedance leakage current						
LOW	V_O = ½ V_{DD}	I_{OZL}	–	–	1	μA
HIGH	V_O = ½ V_{DD}	$-I_{OZH}$	–	–	1	μA

DEVELOPMENT DATA

A.C. CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
RXD, PCMREF, Q0 to Q7, F5						
Output transition time	C_L = 50 pF					
LOW-to-HIGH		t_{TLH}	–	–	30	ns
HIGH-to-LOW		t_{THL}	–	–	30	ns
FOSC						
Maximum pulse frequency	M1 = L	f_{max}	–	–	12	MHz
	M1 = H	f_{max}	–	–	6	MHz
Pulse width						
LOW		t_{WL}	20	–	–	ns
HIGH		t_{WH}	20	–	–	ns
TXD						
Maximum pulse frequency		f_{max}	6	–	–	MHz
Pulse width						
LOW		t_{WL}	50	–	–	ns
HIGH		t_{WH}	50	–	–	ns
RXD	used as input, see Fig. 8					
Set-up time						
RXD to TXD		t_{SURXD}	50	–	–	ns
Hold time						
RXD to TXD		t_{HDRXD}	50	–	–	ns
RXD	used as output, see Fig. 9					
Propagation delay						
TXD to RXD		t_{PRXD}	–	–	50	ns
R/$\overline{O}$ to RXD		$r_{PR/O}$	–	–	50	ns
S/$\overline{L}$	see Fig. 10					
Pulse width LOW		t_{WL}	50	–	–	ns
Minimum set-up time						
TXD to S/$\overline{L}$		t_{SUTXD}	50	–	–	ns
Minimum hold time						
TXD to S/$\overline{L}$		t_{HDTXD}	50	–	–	ns
Propagation delay						
S/$\overline{L}$ to Q0 to Q7		t_P	–	–	50	ns
PCMREF						
Division ratio						
FOSC to PCMREF	M1 = L, M2 = L		750	–	–	Hz/Hz
	M1 = H, M2 = L		375	–	–	Hz/Hz
	M1 = L, M2 = H		756	–	–	Hz/Hz
	M1 = H, M2 = H		378	–	–	Hz/Hz
Duty factor	note 1, S2 = L		–	50	–	%

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
TIM						
Pulse width						
LOW		t_{WL}	700	–	–	ns
HIGH		t_{WH}	100	–	–	ns

Notes to the characteristics

1. When S2 = H, then PCMREF follows FHIN.
2. The condition for the output voltage 'MIDDLE level' deviation is:

$$\left| V_{OM} - \frac{V_{OH} + V_{OL}}{2} \right|$$

3. After a LOW-to-HIGH transition of the R/$\overline{O}$ output, the port is held HIGH for approximately one clock cycle. This low impedance HIGH period is followed by the high impedance state.
4. Output voltage levels:

   Level 2 : $(0{,}134 \pm 0{,}008) \,.\, (V_{O6} - V_{O1}) + V_{O1}$

   Level 3 : $(0{,}366 \pm 0{,}011) \,.\, (V_{O6} - V_{O1}) + V_{O1}$

   Level 4 : $(0{,}634 \pm 0{,}011) \,.\, (V_{O6} - V_{O1}) + V_{O1}$

   Level 5 : $(0{,}866 \pm 0{,}008) \,.\, (V_{O6} - V_{O1}) + V_{O1}$

   Level 7 : $(0{,}500 \pm 0{,}013) \,.\, (V_{O6} - V_{O1}) + V_{O1}$

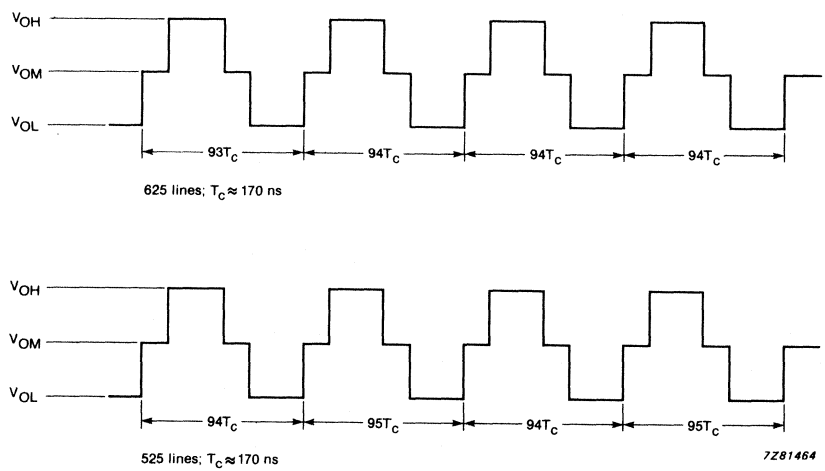


Fig. 4 EROSC output waveform.

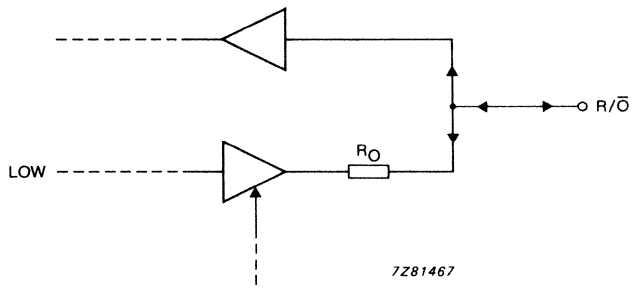


Fig. 5 R/$\overline{O}$ port equivalent output.

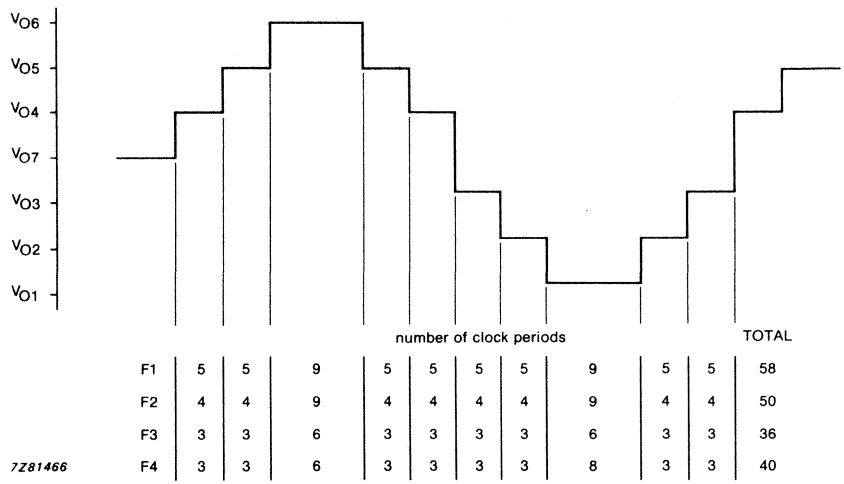


Fig. 6 F1 to F4 output waveform.

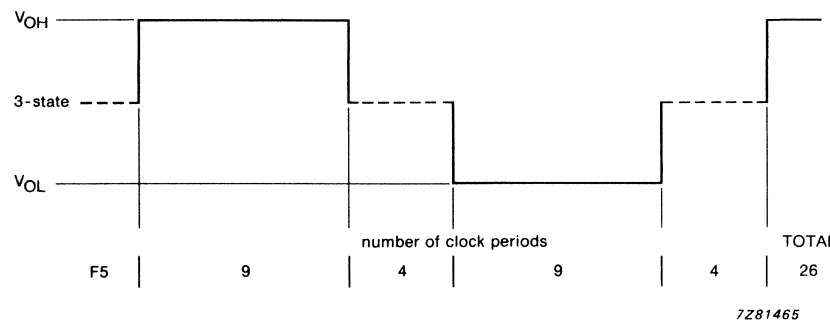


Fig. 7 F5 output waveform.

DEVELOPMENT DATA

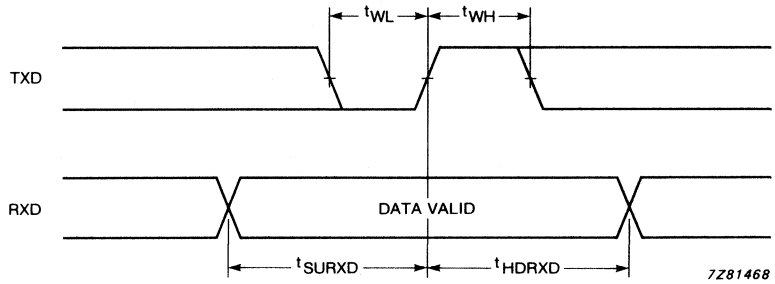


Fig. 8 RXD input waveform.

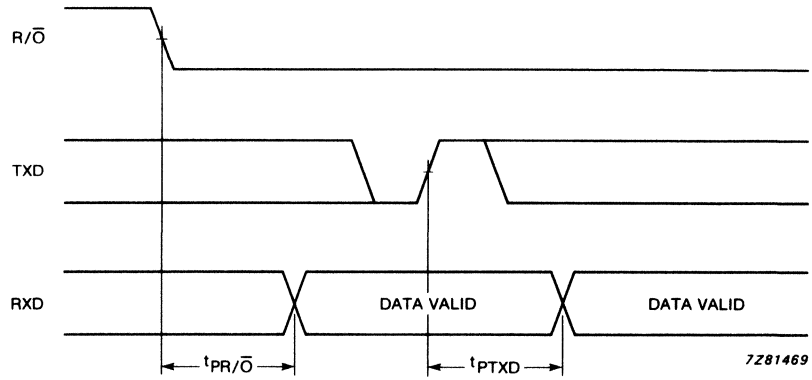


Fig. 9 RXD output waveform.

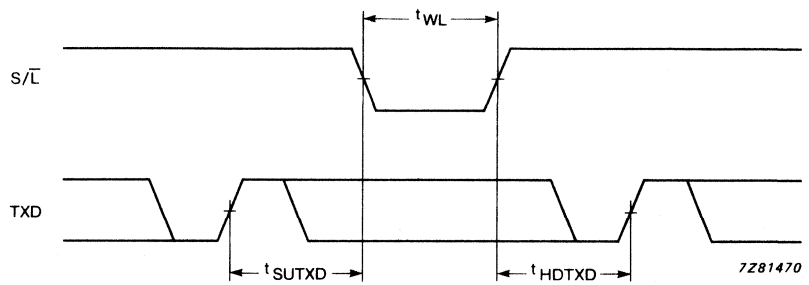


Fig. 10 S/$\overline{L}$ input waveform.

REMOTE CONTROL SYSTEM FOR INFRARED OPERATION

The SAF1032P (receiver/decoder) and the SAF1039P (transmitter) form the basic parts of a sophisticated remote control system (pcm: pulse code modulation) for infrared operation. The ICs can be used, for example, in TV, audio, industrial equipment, etc.
Features:

SAF1032P receiver/decoder:
- 16 programme selection codes
- automatic preset to stand-by at power 'ON', including automatic analogue base settings to 50% and automatic preset of programme selection '1' code
- 3 analogue function controls, each with 63 steps
- single supply voltage
- protection against corrupt codes.

SAF1039P transmitter:
- 32 different control commands
- static keyboard matrix
- current drains from battery only during key closure time
- two transmission modes selectable.

The devices are implemented in LOCMOS (Local Oxidation Complementary MOS) technology to achieve an extremely low power consumption.
Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

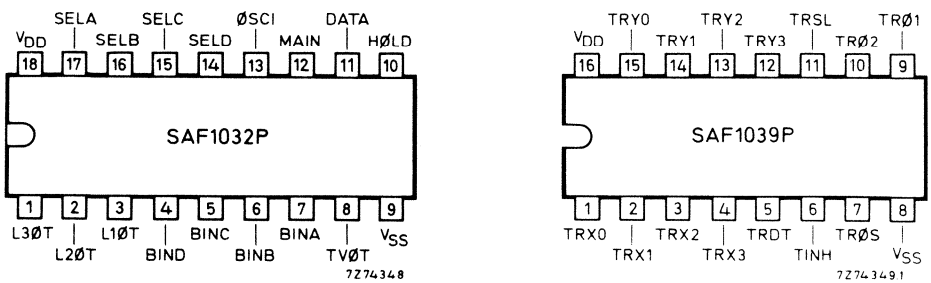


Fig. 1 Pin designations.

PACKAGE OUTLINES

SAF1032P: 18-lead DIL; plastic (SOT-102H).
SAF1039P: 16-lead DIL; plastic (SOT-38Z).

PINNING

To facilitate easy function recognition, each integrated circuit pin has been allocated a code as shown below.

SAF1032P

1	L3ØT	linear output	10	HØLD	control input
2	L2ØT	linear output	11	DATA	data input
3	L1ØT	linear output	12	MAIN	reset input
4	BIND	binary 8 output	13	ØSCI	clock input
5	BINC	binary 4 output	14	SELD	binary 8 output
6	BINB	binary 2 output	15	SELC	binary 4 output
7	BINA	binary 1 output	16	SELB	binary 2 output
8	TVØT	on/off input/output	17	SELA	binary 1 output
9	V_{SS}		18	V_{DD}	

SAF1039P

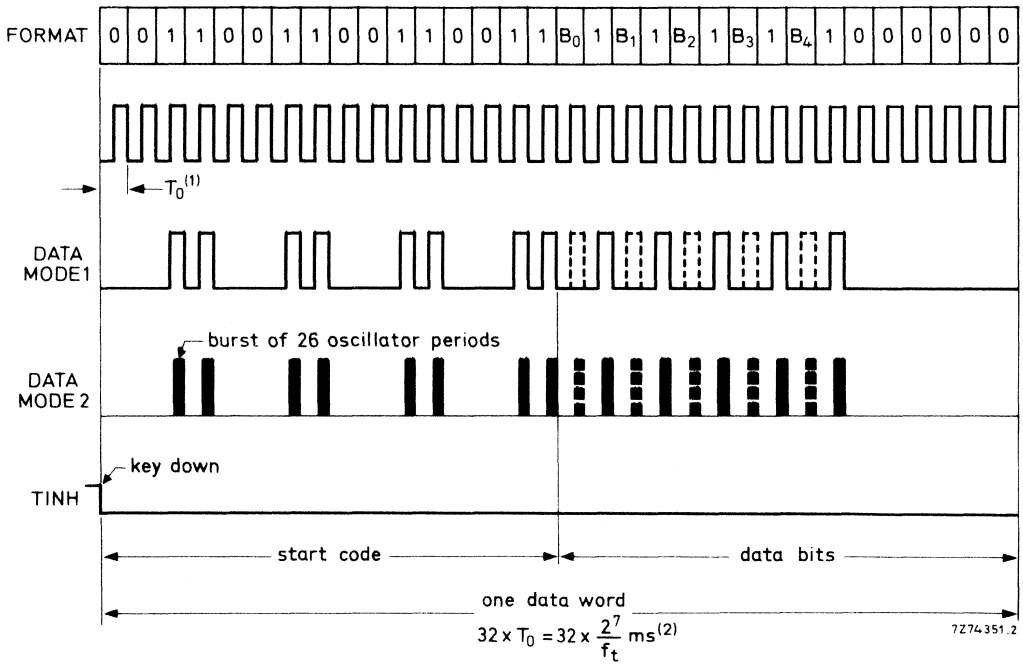
1	TRX0	keyboard input	9	TRØ1	oscillator control input
2	TRX1	keyboard input	10	TRØ2	oscillator control input
3	TRX2	keyboard input	11	TRSL	keyboard select line
4	TRX3	keyboard input	12	TRY3	keyboard input
5	TRDT	data output	13	TRY2	keyboard input
6	TINH	inhibit output/mode select input	14	TRY1	keyboard input
7	TRØS	oscillator output	15	TRY0	keyboard input
8	V_{SS}		16	V_{DD}	

BASIC OPERATING PRINCIPLES

The data to be transmitted are arranged as serial information with a fixed pattern (see Fig. 2), in which the data bit-locations B_0 to B_4 represent the generated key-command code. To cope with IR (infrared) interferences of other sources a selective data transmission is present. Each transmitted bit has a burst of 26 oscillator periods.

Before any operation will be executed in the receiver/decoder chip, the transmitted data must be accepted twice in sequence. This means the start code must be recognized each time a data word is applied and comparison must be true between the data bits of two successively received data words. If both requirements are met, one group of binary output buffers will be loaded with a code defined by the stored data bits, and an internal operation can also take place. See operating code table.

The contents of the 3 analogue function registers are available on the three outputs in a pulse code versus time modulation format after D (digital) to A (analogue) conversion. The proper analogue levels can be obtained by using simple integrated networks. For local control a second transmitter chip (SAF1039P) is used (see Fig. 7).



(1) T_0 = 1 clock period = 128 oscillator periods. (2) f_t in kHz.

Fig. 2 Pattern for data to be transmitted.

TIMING CONSIDERATIONS

The transmitter and receiver operate at different oscillator frequencies. Due to the design neither frequency is very critical, but correlation between them must exist. Calculation of these timing requirements shows the following.

With a tolerance of ±10% on the oscillator frequency (f_t) of the transmitter, the receiver oscillator frequency ($f_r = 3 \times f_t$) must be kept constant with a tolerance of ±20%.
On the other hand, the data pulse generated by the pulse stretcher circuit (at the receiver side) may vary ±25% in duration.

GENERAL DESCRIPTION OF THE SAF1039P TRANSMITTER

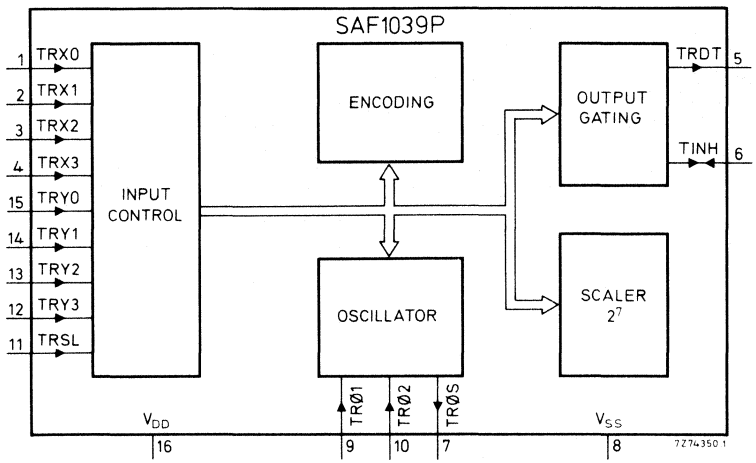


Fig. 3 Block diagram of SAF1039P transmitter.

Any keyboard activity on the inputs TRX0 to TRX3, TRY0 to TRY3 and TRSL will be detected. For a legal key depression, one key down at a time (one TRX and TRY input activated), the oscillator starts running and a data word, as shown on the previous page, is generated and supplied to the output TRDT. If none, or more than 2 inputs are activated at the same time, the input detection logic of the chip will generate an overall reset and the oscillator stops running (no legal key operation).

This means that for each key-bounce the logic will be reset, and by releasing a key the transmitted data are stopped at once.

The minimum key contact time required is the duration of two data words. The on-chip oscillator is frequency controlled with the external components R1 and C1 (see circuit Fig. 6); the addition of resistor R2 means that the oscillator frequency is practically independent of supply voltage variations. A complete data word is arranged as shown in Fig. 2, and has a length of 32 x T_0 ms, where $T_0 = 2^7/f_t$.

Operation mode

	DATA	FUNCTION OF TINH
1	unmodulated: LOCAL operation	output, external pull-up resistor to V_{DD}
2	modulated: REMOTE control	input, connected to V_{SS}

GENERAL DESCRIPTION OF THE SAF1032P RECEIVER/DECODER

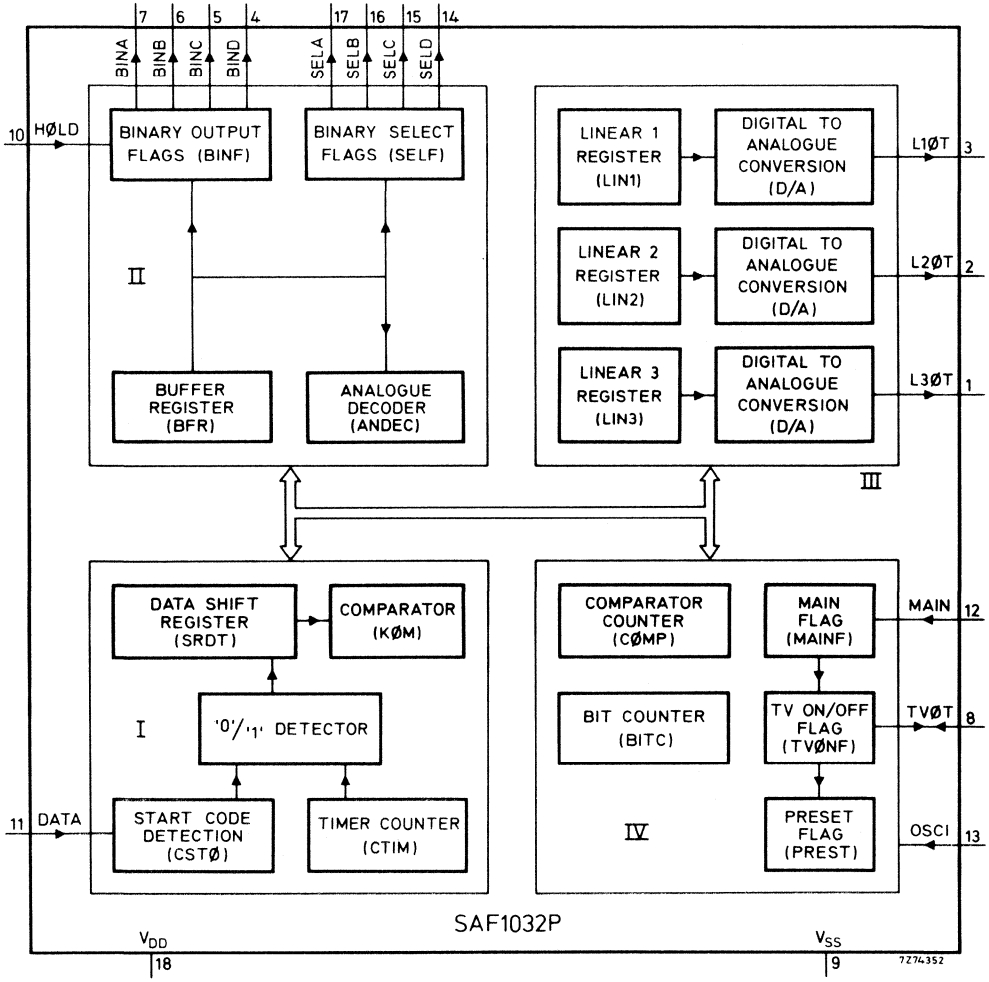


Fig. 4 Block diagram of SAF1032P receiver/decoder.

The logic circuitry of the receiver/decoder chip is divided into four main parts as shown in the block diagram above.

Part I

This part decodes the applied DATA information into logic '1' and '0'.
It also recognizes the start code and compares the stored data-bits with the new data-bits accepted.

Part II

This part stores the programme selection code in the output group (BINF) and memorizes it for condition HØLD = LOW.

It puts the functional code to output group (SELF) during data accept time, and decodes the internally used analogue commands (ANDEC).

Part III

This part controls the analogue function registers (each 6-bits long), and connects the contents of the three registers to the analogue outputs by means of D/A conversion. During sound mute, output L1ØT will be forced to HIGH level.

Part IV

This part keeps track for correct power 'ON' operation, and puts chip in 'stand-by' condition at supply voltage interruptions.

The logic design is dynamic and synchronous with the clock frequency (ØSCI), while the required control timing signals are derived from the bit counter (BITC).

Operation

Serial information applied to the DATA input will be translated into logic '1' and '0' by means of a time ratio detector.

After recognizing the start code (CSTØ) of the data word, the data bits will be loaded into the data shift register (SRDT). At the first trailing edge of the following data word a comparison (KØM) takes place between the contents of SRDT and the buffer register (BFR). If SRDT equals BFR, the required operation will be executed under control of the comparator counter (CØMP).

As shown in the operating code table on the next page, the 4-bit wide binary output buffer (BINF) will be loaded for BFR0 = '0', while for BFR0 = '1' the binary output buffer (SELF), also 4-bit wide will be activated during the data accept time.

At the same time operations involving the internal commands are executed. The contents of the analogue function registers (each 6-bits long) are controlled over 63 steps, with minimum and maximum detection, while the D/A conversion results in a pulsed output signal with a conversion period of 384 clock periods (see Fig. 5).

First power 'ON' will always put the chip in the 'stand-by' position. This results in an internal clearing of all logic circuitry and a 50% presetting of the contents of the analogue registers (analogue base value). The programme selection '1' code will also be prepared and all the outputs will be non-active (see operating output code table).

From 'stand-by' the chip can be made operational via a programme selection command, generated LOCAL or via REMOTE, or directly by forcing the TV ON/OFF output (TVØT) to zero for at least 2 clock periods of the oscillator frequency.

For POWER ON RESET a negative-going pulse should be applied to input MAIN, when V_{DD} is stabilized; pulse width LOW $\geqslant$ 100 μs.

Fig. 5 Analogue output pulses.

OPERATING CODE TABLE

key-matrix position			buffer BFR					BINF (BIN.)				SELF (SEL.)				function
TRX.	TRY.	TRSL	0	1	2	3	4	A	B	C	D	A	B	C	D	
0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	programme select + ON
0	1	0	0	0	0	1	0	1	0	0	0	1	1	1	1	
0	2	0	0	0	1	0	0	0	1	0	0	1	1	1	1	
0	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	
1	0	0	0	1	1	1	0	0	0	1	0	1	1	1	1	
1	1	0	0	1	0	1	0	1	0	1	0	1	1	1	1	
1	2	0	0	1	1	0	0	0	1	1	0	1	1	1	1	
1	3	0	0	1	0	0	0	1	1	1	0	1	1	1	1	
2	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1	programme select + ON
2	1	0	0	0	0	1	1	1	0	0	1	1	1	1	1	
2	2	0	0	0	1	0	1	0	1	0	1	1	1	1	1	
2	3	0	0	0	0	0	1	1	1	0	1	1	1	1	1	
3	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1	
3	1	0	0	1	0	1	1	1	0	1	1	1	1	1	1	
3	2	0	0	1	1	0	1	0	1	1	1	1	1	1	1	
3	3	0	0	1	0	0	1	1	1	1	1	1	1	1	1	
0	0	1	1	0	1	1	0	X	X	X	X	0	1	1	1	analogue base
0	1	1	1	0	0	1	0	X	X	X	X	0	0	1	1	reg. (LIN3) + 1
0	2	1	1	0	1	0	0	X	X	X	X	0	1	0	1	reg. (LIN2) + 1
0	3	1	1	0	0	0	0	X	X	X	X	0	0	0	1	reg. (LIN1) + 1
1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	OFF
1	1	1	1	1	0	1	0	X	X	X	X	1	0	1	1	reg. (LIN3) − 1
1	2	1	1	1	1	0	0	X	X	X	X	1	1	0	1	reg. (LIN2) − 1
1	3	1	1	1	0	0	0	X	X	X	X	1	0	0	1	reg. (LIN1) − 1
2	0	1	1	0	1	1	1	X	X	X	X	0	1	1	0	mute (set/reset)
2	1	1	1	0	0	1	1	X	X	X	X	0	0	1	0	spare functions
2	2	1	1	0	1	0	1	X	X	X	X	0	1	0	0	
2	3	1	1	0	0	0	1	X	X	X	X	0	0	0	0	
3	0	1	1	1	1	1	1	X	X	X	X	1	1	1	0	
3	1	1	1	1	0	1	1	X	X	X	X	1	0	1	0	
3	2	1	1	1	1	0	1	X	X	X	X	1	1	0	0	
3	3	1	1	1	0	0	1	X	X	X	X	1	0	0	0	

Note

Reset mute also on programme select codes, (LIN1) ± 1, and analogue base.

OPERATING OUTPUT CODE

	(BIN.)				(SEL.)				(LØT)			TVØT
	A	B	C	D	A	B	C	D	1	2	3	
'stand-by' OFF via remote	0	0	0	0	0	0	0	0	1	0	0	1
ON – 'not hold' condition non-operating	1	1	1	1	1	1	1	1	X	X	X	0
ON – 'hold' condition non-operating	X	X	X	X	1	1	1	1	X	X	X	0

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}-V_{SS}		−0,5 to 11	V
Input voltage	V_I	max.	11	V
Current into any terminal	$\pm I_I$	max.	10	mA
Power dissipation (per output)	P_o	max.	50	mW
Power dissipation (per package)	P_{tot}	max.	200	mW
Operating ambient temperature	T_{amb}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1039P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	7	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	10	μA	10	25
		–	1	50	μA	7	65
operating; TRØ1 at V_{SS}; outputs unloaded; one keyboard switch closed	I_{DD}	–	–	1,7	mA	10	all
		–	0,8	–	mA	10	25
Inputs (note 1)							
TRØ2; TINH (note 2)							
input voltage HIGH	V_{IH}	$0,8V_{DD}$	–	V_{DD}	V	7 to 10	all
input voltage LOW	V_{IL}	0	–	$0,2V_{DD}$	V	7 to 10	all
input current	I_I	–	10^{-5}	1	μA	10	25
Outputs							
TRDT; TRØS; TRØ1							
output current HIGH at $V_{OH} = V_{DD} - 0,5$ V	$-I_{OH}$	0,4	–	–	mA	7	all
output current LOW at V_{OL} = 0,4 V	I_{OL}	0,4	–	–	mA	7	all
TRDT output leakage current when disabled $V_O = V_{SS}$ to V_{DD}	I_{OL}	–	–	1	μA	10	25
TINH							
output current LOW V_{OL} = 0,4 V	I_{OL}	0,4	–	–	mA	7	all
Oscillator							
maximum oscillator frequency	f_{osc}	120	–	–	kHz		
frequency variation with supply voltage, temperature and spread of IC properties at f_{nom} = 36 kHz (note 3)	Δf	–	–	$0,15f_{nom}$		7 to 10	all
oscillator current drain at f_{nom} = 36 kHz	I_{osc}	–	1,3	2,5	mA	10	25

Notes follow characteristics.

CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1032P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	8	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	50	μA	10	25
		–	1	300	μA	10	85
operating; I_O = 0; at ØSCI frequency of 100 kHz	I_{DD}	–	–	1	mA	10	all
Inputs							
DATA; ØSCI; HØLD; TVØT (see note 4)							
input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V	8 to 10	all
input voltage LOW	V_{IL}	0	–	$0{,}2V_{DD}$	V	8 to 10	all
MAIN; tripping levels							
input voltage increasing	V_{ti}	$0{,}4V_{DD}$	–	$0{,}9V_{DD}$	V	5 to 10	all
input voltage decreasing	V_{td}	$0{,}1V_{DD}$	–	$0{,}6V_{DD}$	V	5 to 10	all
input current; all inputs except TVØT	I_I	–	10^{-5}	1	μA	10	25
input signal rise and fall times (10% and 90% V_{DD}) all inputs except MAIN	t_r, t_f	–	–	5	μs	8 to 10	all
Outputs							
programme selection: BINA/B/C/D							
auxiliary: SELA/B/C/D							
analogue: L3ØT; L2ØT; L1ØT TVØT (note 4)							
all open drain n-channel output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA	8	all
output leakage current at $V_O = V_{SS}$ to V_{DD}	I_{OL}	–	–	10	μA	10	all

For note 4 see next page.

Notes to characteristics

1. The keyboard inputs (TRX.; TRY.; TRSL) are not voltage driven (see application information diagram Fig. 6).

   If one key is depressed, the circuit generates the corresponding code. The number of keys depressed at a time, and this being recognized by the circuit as an illegal operation, depends on the supply voltage (V_{DD}) and the leakage current (between device and printed-circuit board) externally applied to the keyboard inputs.

   If no leakage is assumed, the circuit recognizes an operation as illegal for any number of keys > 1 depressed at the same time with $V_{DD} = 7$ V. At a leakage due to a 1 MΩ resistor connected to each keyboard input and returned to either V_{DD} or V_{SS}, the circuit recognizes at least 2 keys depressed at a time with $V_{DD} = 7$ V.

   The highest permissible values of the contact series resistance of the keyboard switches is 500 Ω.

2. Inhibit output transistor disabled.

3. Δf is the width of the distribution curve at 2 σ points (σ = standard deviation).

4. Terminal TVØT is input for manual 'ON'. When applying a LOW level TVØT becomes an output carrying a LOW level.

APPLICATION INFORMATION

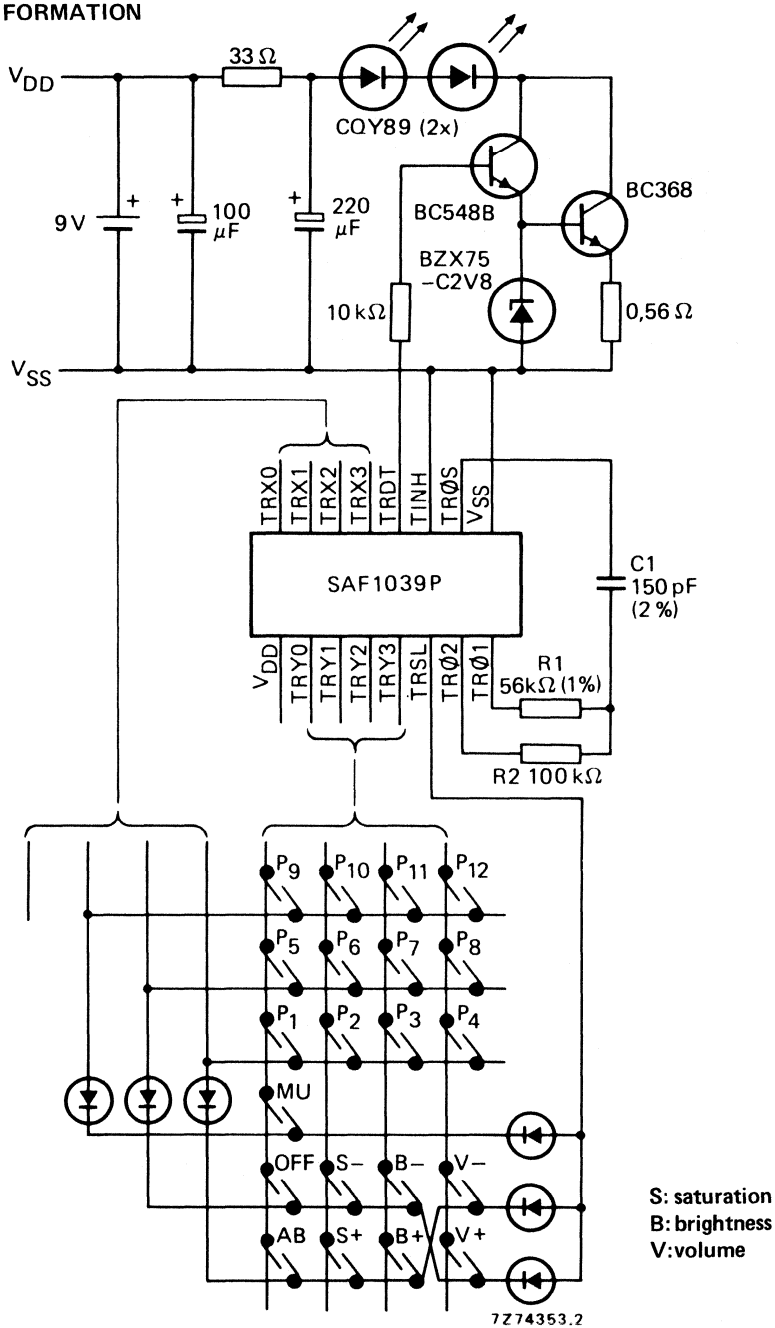


Fig. 6 Interconnection diagram of transmitter circuit SAF1039P in a remote control system, for a television receiver with 12 programmes.

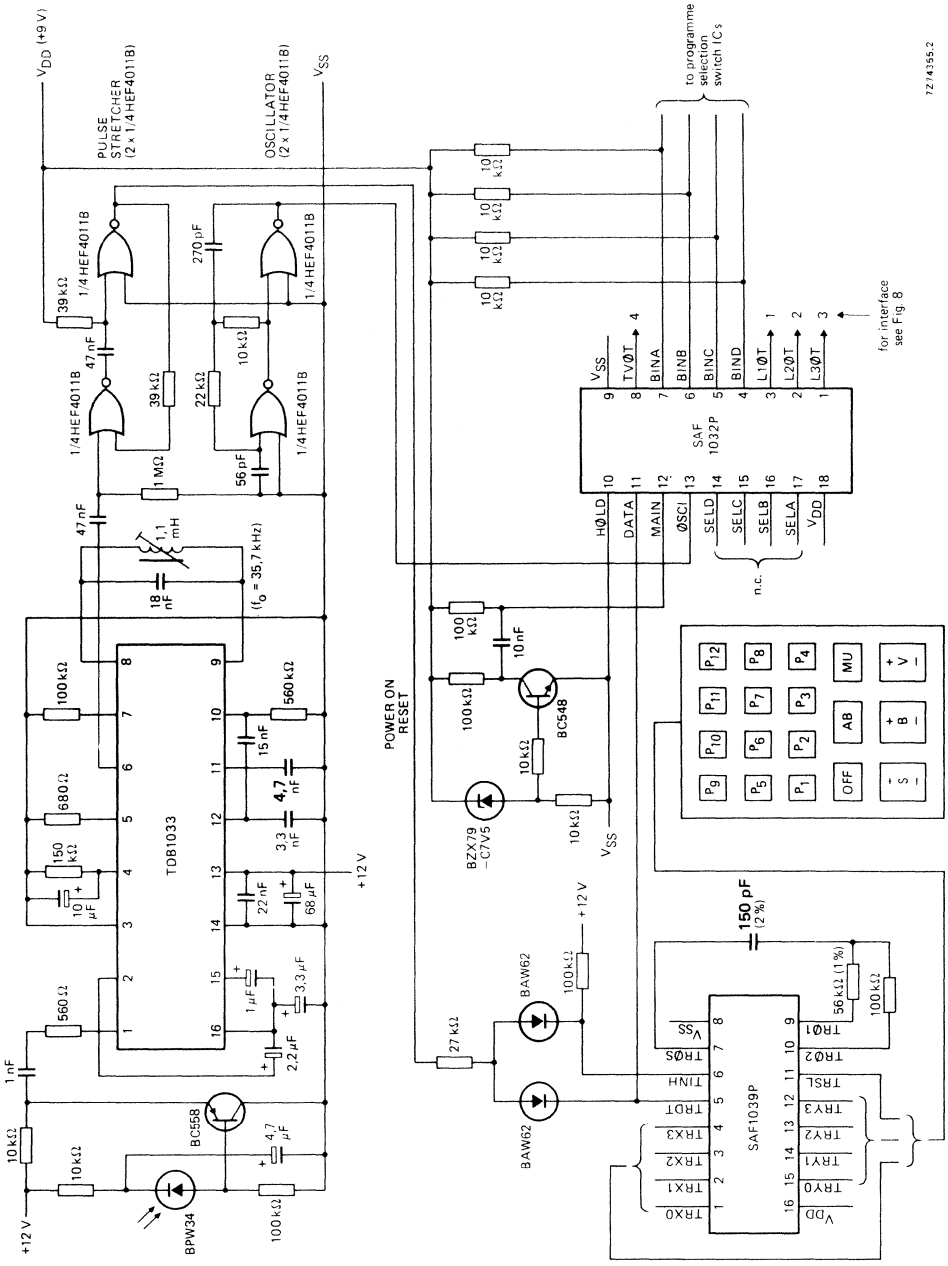


Fig. 7 Interconnection diagram showing the SAF1032P and SAF1039P used in a TV control system.

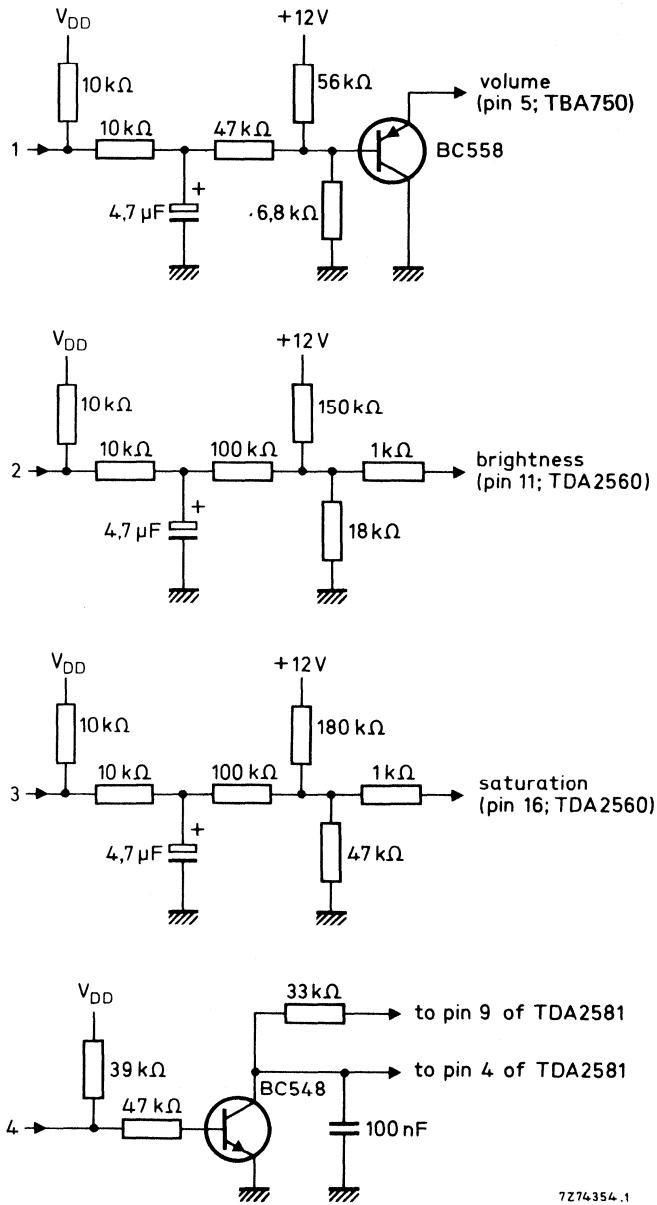


Fig. 8 Additional circuits from outputs L1ØT (1), L2ØT (2), L3ØT (3) and TVØT (4) of the SAF1032P in circuit of Fig. 7.

DATA LINE DECODER

GENERAL DESCRIPTION

The SAF1135 is a data line decoder, designed in CMOS technology, which operates in conjunction with the data line processor (SAA5235) to form a data line receiver system.

This system receives and decodes binary data that is transmitted in line 16 of every first field of a standard television signal. The decoded information is accessed via the built-in I^2C bus interface. This information can be used to program a video tape recorder to start and stop the recording of a television program at the correct time, regardless of a delay or extension in the transmission time of the required television program.

Valid Video Programming System (VPS) data is transmitted in line 16 only. There is no VPS information in line 329.

The data transmission is biphase modulated and the bit transfer rate is 2,5 Mbit/s.

Features

- Field selection
- Line 16 decoding
- Start code check
- Biphase check
- Storage of data line information
- Generation of data reset pulse
- I^2C bus transmitter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 14)	I_{DD}	–	1	–	mA
Bit transfer rate at input DLD (pin 8)	BR_{DLD}	–	2,5	–	Mbits/s
Clock frequency at input DLCL (pin 11)	f_{DLCL}	–	5	–	MHz
Storage temperature range	T_{stg}	−65	–	+150	°C
Operating ambient temperature range	T_{amb}	0	–	70	°C

PACKAGE OUTLINES

14-lead DIL; plastic (SOT-27).

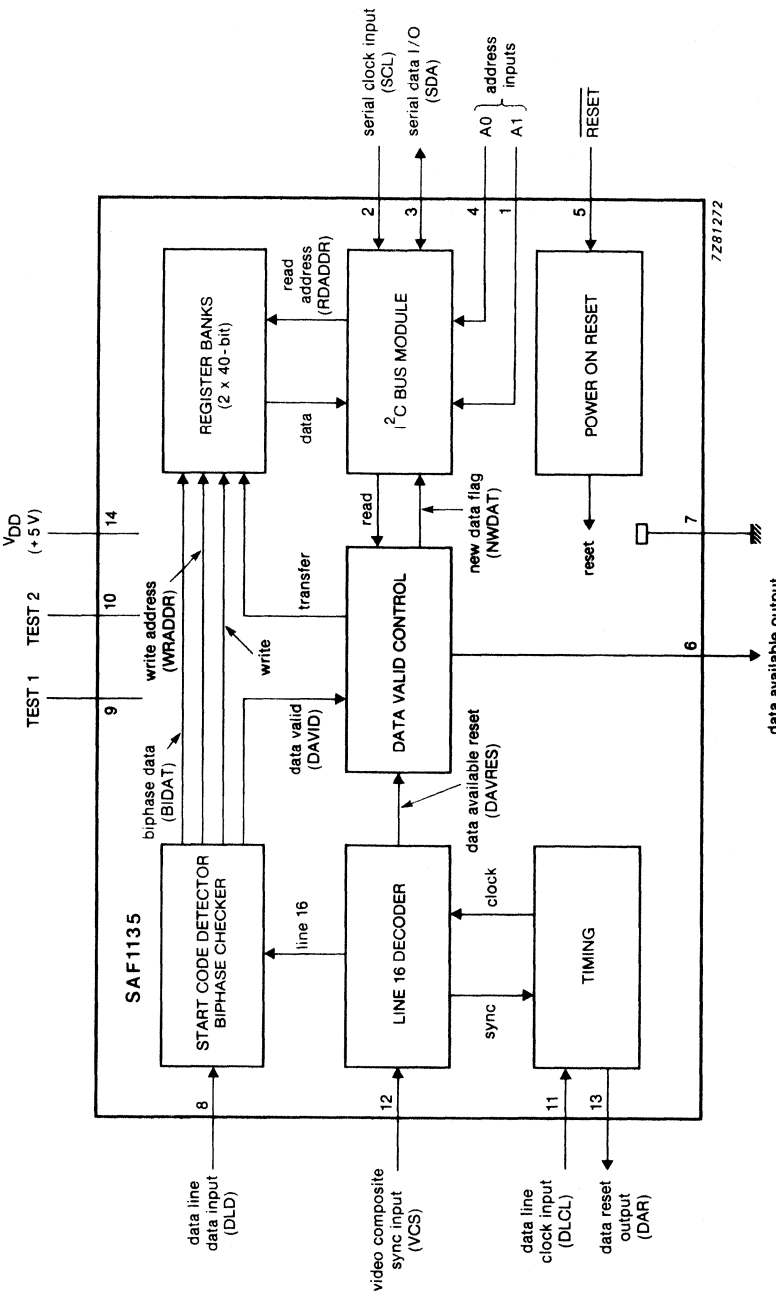


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The SAF1135 is designed to receive and decode Video Tape Recorder (VTR) control information which is transmitted in line 16 of every first field of a standard television signal. The following description refers to the block diagram Fig. 1 unless otherwise stated.

Data line 16

The total information of data line 16 consists of fifteen 8-bit words. The contents of the information is shown in Fig. 2, a timing diagram of the data line in Fig. 3 and a survey of VTR control labels in Fig. 4.

From the total fifteen 8-bit words, the SAF1135 extracts words 5, 11, 12, 13 and 14. The contents of these words can be requested via the built-in I^2C bus interface (see Fig. 9). The circuit is fully transparent, thus each bit is transferred without modification. Only the sequence of the words is changed; words 11 to 14 being transmitted first followed by word 5.

By evaluation of the Video Composite Sync (VCS) signal at pin 12 the SAF1135 identifies the beginning of line 16 in the first field. The line 16 decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection, see Fig. 5) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in register bank R (Receive). If no biphase error has occurred, the contents of register bank R are transferred to register bank T (Transmit) by the data valid control signal (DAVID). If the system has been addressed, this transfer is delayed until the next start or stop condition of the I^2C bus has been received.

The last correct data line information remains available until it is read via the I^2C bus. After it is read once the stored information is no longer considered to be valid, the internal new data flag (NWDAT) is reset and if the circuit is addressed, the only VPS data sent back is "FFF...F". The same conditions apply after power-up. Then no data can be read out.

New data is available after reception of another error-free line 16.

Power-on Reset

Reset pulses applied externally to pin 5 ($\overline{\text{RESET}}$; active LOW) are latched internally by the power-on reset circuit.

$\overline{\text{RESET}}$ = LOW influences:

- I^2C bus logic to no acknowledge
- NWDAT flag and internal timing to reset
- Data available output ($\overline{\text{DAV}}$; active LOW) at pin 6 forced to LOW
- Data reset output (DAR) at pin 13 forced to HIGH
- Serial data (SDA) input/output at pin 3 released

When $\overline{\text{RESET}}$ changes to HIGH the reset period is terminated with the next negative-going transition of the data line clock (DLCL) input at pin 11. Then, the data available ($\overline{\text{DAV}}$) output at pin 6 will go HIGH.

When an external reset is not used pin 5 is connected to V_{DD}. If an external reset is required, the rise time (t_r) of $\overline{\text{RESET}}$ voltage must be greater than 50 μs. An external 10 kΩ resistor connected between pin 5 and V_{DD} and an external 2,7 nF capacitor connected to V_{SS} will result in $t_r \geqslant 50\ \mu s$.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Word	Content
1	Run in
2	Start code
3	Program source identification (binary coded)
4	Program source identification (ASCII sequential)
5	Sound and VTR control information
6	Program/Test picture identification
7	Internal information exchange
8	Address assignment of signal distribution
9	
10	Messages/Commands
11	VTR Control Information
12	
13	
14	
15	Reserve

Fig. 2 Total information of data line 16.

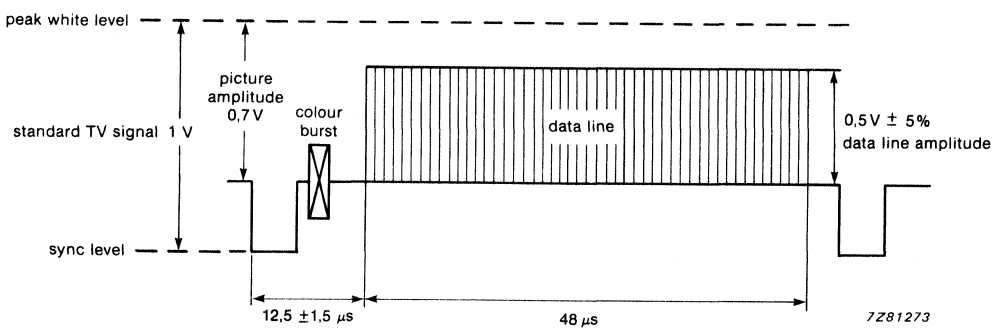


Fig. 3 Timing diagram of data line 16; modulation depth 71,4%.

VTR Control Information

Word-no.	5								11								12								13								14							
Bit-no.	1	2	3	4	5	6	7	8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Label binary	Bit 1	Bit 2	Status						Address range	Day							Month				Hour				Minute								Nation				Program Source			
	0	0	2-Channel																																				
	0	1	Mono																																				
	1	0	Stereo																																				
	1	1	2-Channel																																				
										Special System Code																														
System Status Code									1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	NC	.	.	NC	PC	.	.	.	PC
	Bit 3	Bit 4																																					
Pause Code	1	0	not for children						1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	NC	.	.	NC	PC	.	.	.	PC
Interrupt Code	0	1	free						1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	NC	.	.	NC	PC	.	.	.	PC

Where:

X = 0 or 1 (bit)
NC is the Nation Code
PC is the Program Source Code

Fig. 4 VTR control information of data line 16.

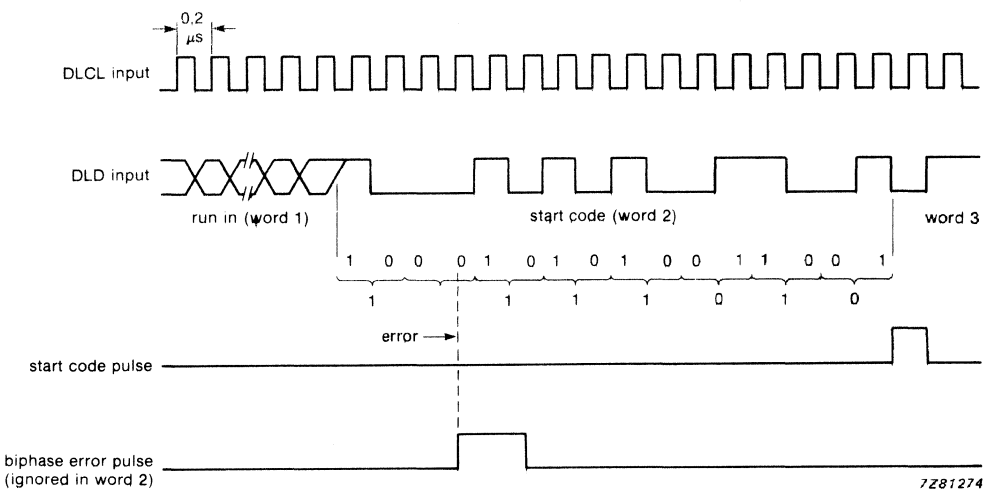


Fig. 5 Timing diagram of start code detection.

FUNCTIONAL DESCRIPTION (continued)

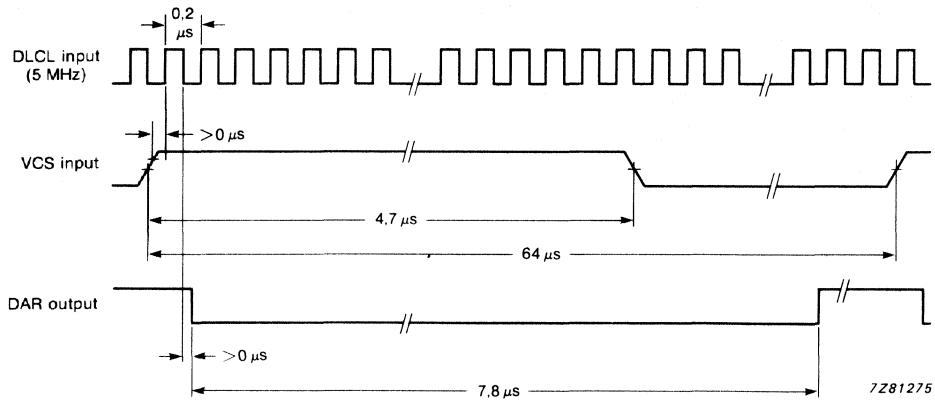


Fig. 6 Timing diagram of the data reset pulse generation.

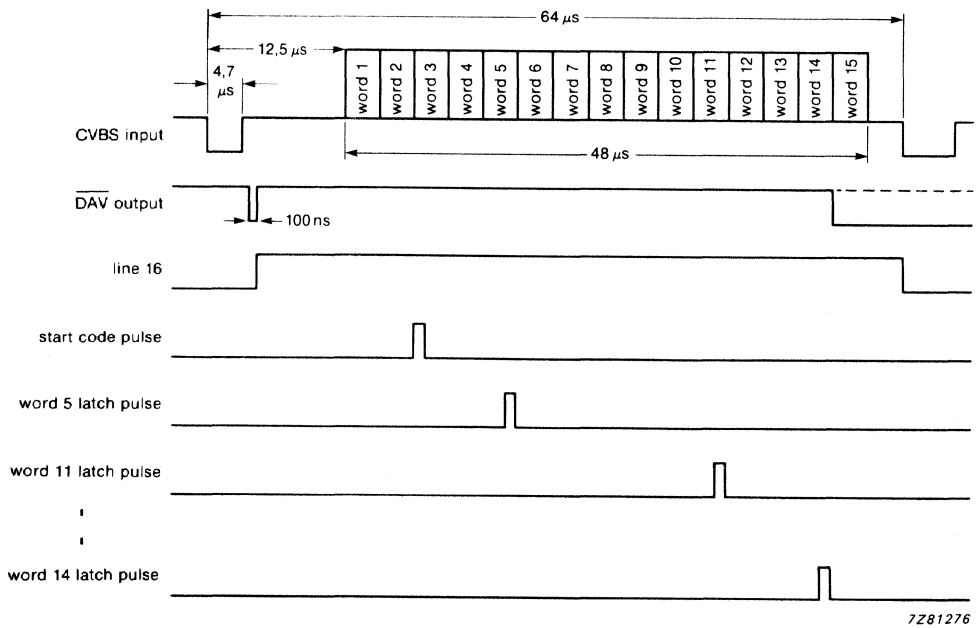


Fig. 7 Timing diagram of the data available output and word latch pulses.

Data line data and clock inputs (DLD; DLCL)

The data line data and clock signals from the SAA5235 are input at pins 8 and 11 respectively. The data transmission is biphase modulated, the bit transfer rate is 2,5 Mbit/s and the clock frequency is 5 MHz.

Input DLD incorporates an internal active clamping circuit. DLCL is internally a.c. coupled.

Video composite sync input (VCS)

The VCS input pulse at pin 12 is used for:

- Generation of the data reset pulse (DAR)
- Identification of the first field
- Selection of line 16

The timing of the data reset pulse generation is shown in Fig. 6.

I^2C bus address inputs (A0; A1)

The two I^2C address inputs at pins 4 and 1 respectively, provide the four different addresses 20H, 22H, 24H and 26H.

Data reset output (DAR)

The DAR output at pin 13 is a line frequency pulse with a 0,88 duty factor derived from the VCS pulse. The DAR pulse is fed to the SAA5235 to reset the data slicer circuit and the clock phase detector circuit.

Data available output ($\overline{DAV}$)

The $\overline{DAV}$ active LOW output at pin 6 is set to LOW after reception of one error-free data line 16. $\overline{DAV}$ returns to HIGH after at the beginning of the next first field.

If no valid data is available $\overline{DAV}$ remains HIGH. However, a short duration (100 ns) pulse inserted at the beginning of line 16 ensures that a HIGH-to-LOW transition occurs, which can be used for triggering.

The timing of $\overline{DAV}$ output and word latch pulses is shown in Fig. 7.

I^2C bus

The internally latched data from words 5 and 11 to 14 can be clocked out via the I^2C interface by a bus master. The lines are the serial clock input (SCL) at pin 2 and the serial data input/output (SDA) at pin 3.

The SAF1135 can operate only as a slave transmitter on the bus.
Data format is shown in Fig. 8.

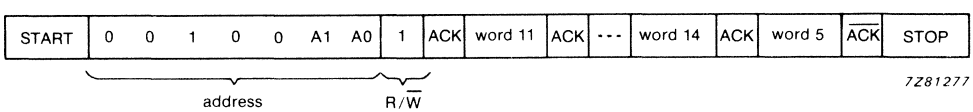


Fig. 8 I^2C bus data format.

- The MSB of each word is transmitted first.
- There is no restriction on the number of words to be transmitted, but if more than five words are requested, word 5 will be repeated.
- Noise pulses less than 200 ns duration are ignored on the bus lines.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 14)	V_{DD}		−0,5 to +7,0	V
Supply current (pin 14)	I_{DD}	max.	20	mA
Supply current (pin 7)	I_{SS}	max.	20	mA
Input voltage (pins 8 and 11)	V_I		−0,5 to +12	V
Input voltage on all other pins	V_I		−0,5 to V_{DD} +0,5*	V
Input current	$\pm I_I$	max.	10	mA
Output current	$\pm I_O$	max.	10	mA
Power dissipation per package**	P_{tot}	max.	400	mW
Power dissipation per output	P	max.	100	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

* V_{DD} +0,5 not to exceed 7,0 V.

** Above +60 °C: derate linearly with 8 mW/K.

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 14)						
Supply voltage	–	V_{DD}	4,5	5	5,5	V
Supply current	Quiescent at 25 °C All inputs at V_{DD} or V_{SS} $\overline{RESET}$ at V_{SS} TEST 1 and TEST 2 at V_{DD} I_O = 0 mA	I_{DD}	–	–	10	μA
	During normal operation (without LED at $\overline{DAV}$, V_{DD} = 5 V)	I_{DD}	–	1	–	mA
Inputs						
A0, A1, TEST 1, TEST 2, SCL						
Input voltage LOW		V_{IL}	–	–	$0,2V_{DD}$	V
Input voltage HIGH		V_{IH}	$0,7V_{DD}$	–	–	V
Leakage current		I_{LI}	–	–	1	μA
DLCL						
Input voltage	Clock internally a.c. coupled	V_I	–	–	12	V
Leakage current	V_I = 0 to 10 V	I_{LI}	–	–	10	μA
$\overline{RESET}$	During normal operation pin 5 connected to V_{DD}					
Input voltage LOW		V_{IL}	–	–	$0,3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0,9V_{DD}$	–	–	V
Input current HIGH		I_{IH}	–	–	15	μA
Leakage current		I_{LI}	–	–	10	μA
VCS						
Input voltage LOW		V_{IL}	–	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	–	V
Leakage current		I_{LI}	–	–	1	μA

D.C. CHARACTERISTICS (continued)

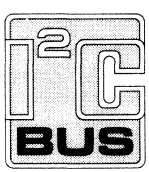
parameter	conditions	symbol	min.	typ.	max.	unit
Inputs/Outputs						
DLD	Internal active clamping circuit, open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	2,0	–	12	V
Leakage current		I_{LI}	–	–	1	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
SDA	open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	3,15	–	–	V
Leakage current	V_{DD} = 6 V; V_I = 0 or V_{DD}	I_{LI}	–	–	6	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Outputs						
DAR						
Output voltage LOW	I_{OL} = 1 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V
$\overline{DAV}$						
Output voltage LOW	I_{OL} = 10 mA	V_{OL}	–	–	1,0	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs						
Input capacitance		C_I	–	–	10	pF
A0, A1, TEST 1, TEST 2, SCL						
Rise time	$V_{IL(max)}$ to $V_{IH(min)}$	t_r	50	–	–	µs
DLCL						
Clock frequency	sinusoidal input signal	f_{DLCL}	–	5	–	MHz
Input voltage	peak-to-peak value	$V_{I(p-p)}$	1	–	–	V
DLD						
Coupling capacitor		C_{EXT}	—	1	4,7	nF
Set-up time	relative to rising edge of DLCL	t_{SU}	40	–	–	ns
Hold-up time	relative to rising edge of DLCL	t_{HD}	40	–	–	ns
Outputs						
DAR, $\overline{DAV}$						
Rise and fall times	C_L = 50 pF	t_r, t_f	–	–	50	ns
DAR-time LOW		$t_{DAR,L}$	–	7,8	–	µs
SDA						
Fall time	C_L = 400 pF	t_f	–	–	300	ns
I²C bus - Input/Output						
	For both SDA and SCL valid					
Input current HIGH	0,9 V_{DD}, including I_{LI} of possible output stage	I_{IH}	–	–	10	µA
Input capacitance		C_I	–	–	10	pF
Rise time		t_r	–	–	1	µs
Fall time		t_f	–	–	0,3	µs
Clock frequency		f_{CL}	–	–	100	kHz
Pulse duration LOW		t_{LOW}	4,7	–	–	µs
Pulse duration HIGH		t_{HIGH}	4,0	–	–	µs



Purchase of Philips I²C components conveys a license under the Philips I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

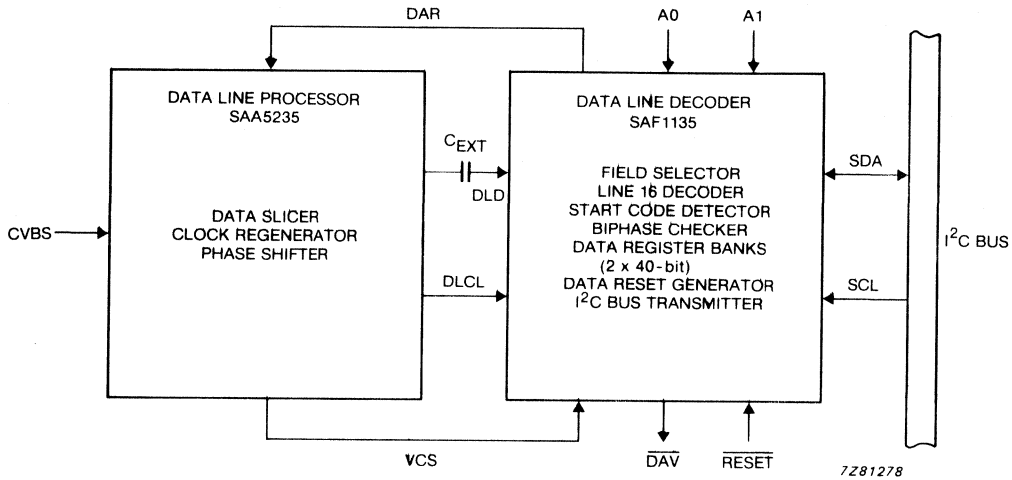


Fig. 9 Data line receiver.

SOUND I.F. AMPLIFIER/DEMODULATOR FOR TV

The TBA120U is an i.f. amplifier with a symmetrical FM demodulator and an a.f. amplifier with adjustable output voltage. The a.f. amplifier is also provided with an output for volume control and an input for VCR operation.

The input and output of the TBA120U are especially designed for LC-circuits, but the input can also be used with a ceramic filter.

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	12 V
Supply current	I_P	typ.	13,5 mA
I.F. voltage gain at f = 5,5 MHz	$G_{v\ if}$	typ.	68 dB
Input voltage starting limiting	V_i	typ.	30 μV
AM suppression at $\Delta f = \pm 50$ kHz	α	typ.	60 dB
A.F. output voltage adjustment range (pin 8)	$\Delta V_{o\ af}$	typ.	85 dB
A.F. output voltage at $\Delta f = \pm 50$ kHz (r.m.s. value)			
at pin 8	$V_{o\ af(rms)}$	typ.	1,2 V
at pin 12	$V_{o\ af(rms)}$	typ.	1,0 V

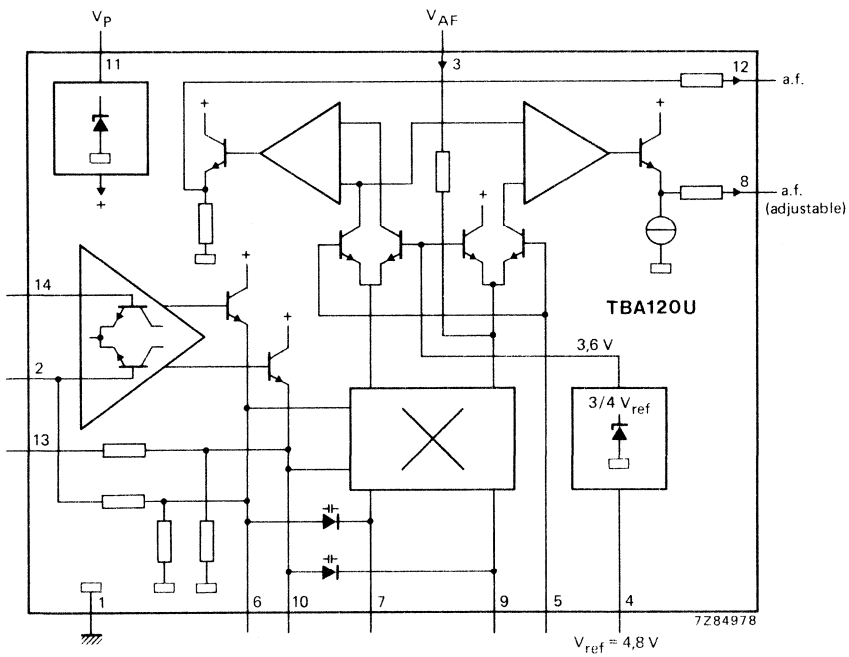


Fig. 1 Block diagram.

PACKAGE OUTLINE

14-lead DIL; plastic (SOT-27)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-1}$	max.	18	V*
Adjustment voltage (pin 5)	V_{5-1}	max.	6	V
Total power dissipation	P_{tot}	max.	400	mW
By-pass resistance	R_{13-14}	max.	1	kΩ
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; f = 5,5 MHz

I.F. voltage gain	$G_{v\ if\ 6-14}$	typ.	68	dB
Input voltage starting limiting at Δf = ± 50 kHz; f_m = 1 kHz	V_i	typ. <	30 60	μV μV
I.F. output voltage at limiting (peak-to-peak value)	$V_{o\ if\ (p-p)}$	typ.	250	mV
AM suppression at Δf = ± 50 kHz; V_i = 500 μV; f_m = 1 kHz; m = 30%	α	> typ.	50 60	dB dB
I.F. residual voltage without de-emphasis				
at pin 12	$V_{if\ 12}$	typ.	30	mV
at pin 8	$V_{if\ 8}$	typ.	20	mV
A.F. voltage gain	$G_{v\ af\ 8-3}$	typ.	7,5	
A.F. adjustment at R_{4-5} = 5 kΩ; R_{5-1} = 13 kΩ	$\Delta V_{o\ af}$	 typ.	20 to 36 28	dB dB
A.F. output voltage control range	$\Delta V_{o\ af}$	> typ.	70 85	dB dB
Adjustment resistor**	R_{4-5}		1 to 10	kΩ
D.C. voltage portion at the a.f. outputs				
pin 12	V_{12-1}	typ.	5,6	V
pin 8	V_{8-1}	typ.	4,0	V
Output resistance of the a.f. outputs				
pin 12	$R_{o\ 12-1}$	typ.	1,1	kΩ
pin 8	$R_{o\ 8-1}$	typ.	1,1	kΩ
Input resistance of the a.f. input	$R_{i\ 3-1}$	typ.	2	kΩ
Stabilized reference voltage	$V_{4-1} = V_{ref}$	 typ.	4,2 to 5,3 4,8	V V
Source resistance of reference voltage source	R_{4-1}	typ.	12	Ω

* Supply voltage operating range is 10 to 18 V.

** Pin 5 must be connected to pin 4, when volume control adjustment is not applicable.

Hum suppression			
at pin 12	V_{12}/V_{11}	typ.	30 dB
at pin 8	V_8/V_{11}	typ.	35 dB
Supply current (pin 11)	$I_P = I_{11}$		9,5 to 17,5 mA
		typ.	13,5 mA
I.F. input impedance	$\|Z_i\|$	typ.	40 kΩ/4,5 pF
		>	15 kΩ/< 6 pF
A.F. output voltage at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 45$; r.m.s. value			
at pin 12	$V_{o\,af\,(rms)}$	typ.	1,0 V
at pin 8	$V_{o\,af\,(rms)}$	typ.	1,2 V
Distortion at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 20$	d_{tot}	typ.	1 %

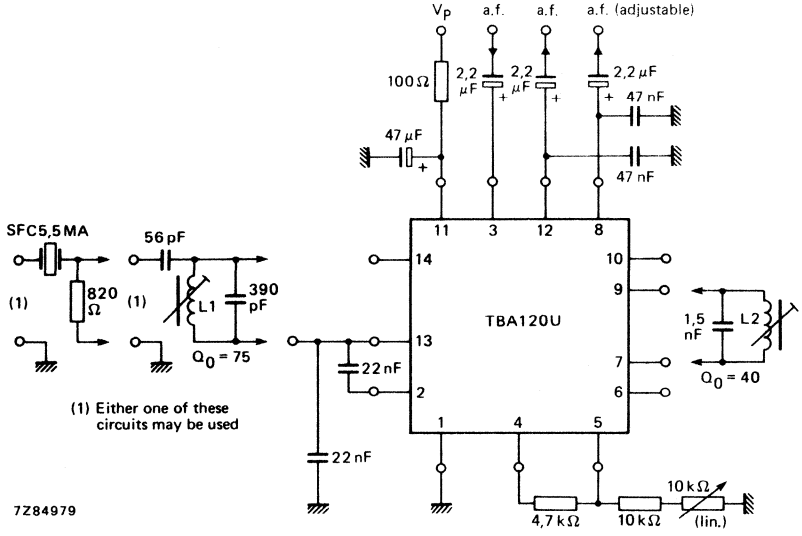


Fig. 2 Application example using TBA120U.

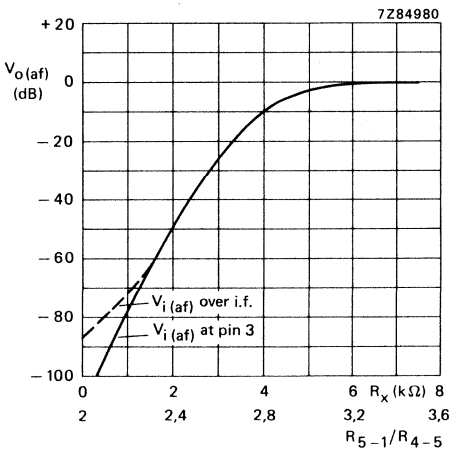


Fig. 3 The a.f. output voltage at pin 8 as a function of the resistance values as shown in Fig. 4.

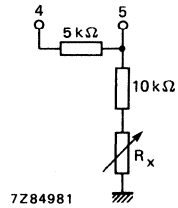
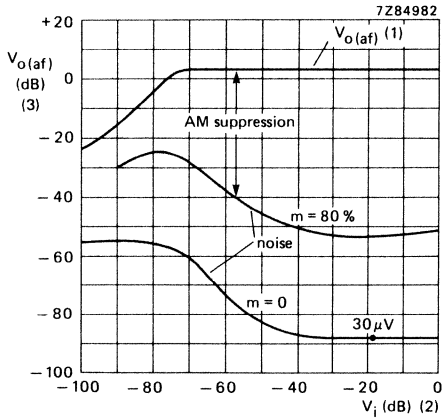


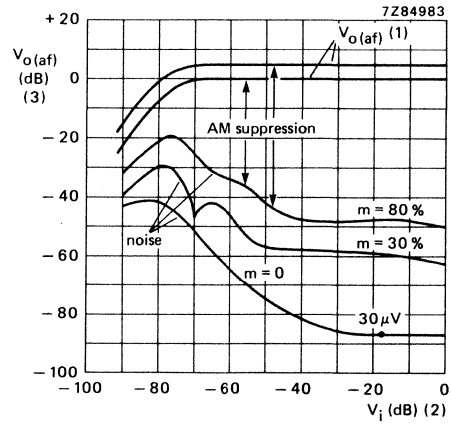
Fig. 4 Resistor conditions for curves in Fig. 3.



(1) $V_{o\,af}$ with de-emphasis at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $d_{tot} = 1{,}5\%$; 0 dB ≙ 770 mV.

(2) V_i: 0 dB ≙ 200 mV at 60 Ω.

Fig. 5 The a.f. output voltage at pin 8 as a function of the input voltage with SFC 5,5 MA at the input (see Fig. 2).



(1) $V_{o\,af}$ with de-emphasis at $f_m = 1$ kHz; 0 dB ≙ 770 mV;
curve a: $\Delta f = \pm 50$ kHz; $d_{tot} = 3\%$;
curve b: $\Delta f = \pm 25$ kHz; $d_{tot} = 1\%$.

(2) V_i: 0 dB ≙ 200 mV at pin 14.

Fig. 6 The a.f. output voltage at pin 8 as a function of the input voltage with broadband input (60 Ω).

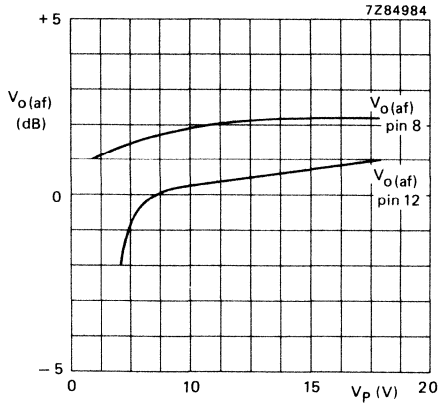


Fig. 7 The a.f. output voltages at pins 8 and 1 as a function of the supply voltage; 0 dB ≙ 770 mV.

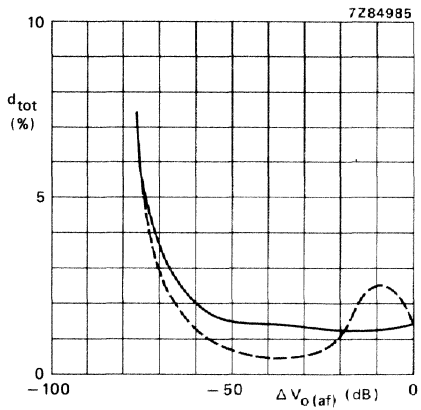


Fig. 8 Total distortion as a function of the a.f. output voltage change.
——— 0 dB ≙ 900 mV over i.f. (pin 8)
– – – – 0 dB ≙ 1,15 V (pin 8)

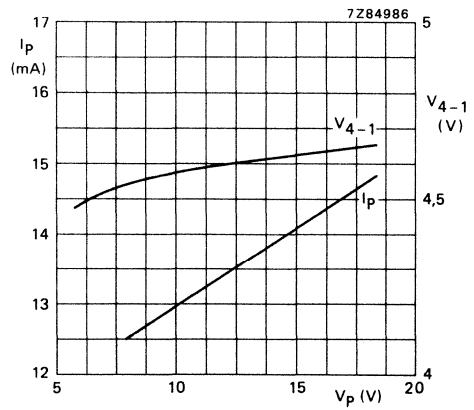


Fig. 9 Supply current and the reference voltage at pin 4 as a function of supply voltage.

HORIZONTAL COMBINATION

The TBA920 is a monolithic integrated circuit intended for television receivers with transistor, thyristor, or tube-equipped output stages.
It combines the following functions:
- noise gated sync separator
- line oscillator
- phase comparison between sync pulse and oscillator
- loop gain and time constant switching (also for video recorder applications)
- phase comparison between line-flyback pulse and oscillator
- output stage for drive a variety of line output stages

QUICK REFERENCE DATA

Supply voltage	V_{1-16}	nom.	12 V
Ambient temperature	T_{amb}		25 °C
Input signals			
Video input voltage (positive-going sync) top sync to white value	$V_{8-16(p-p)}$	typ.	3 V 1 to 7 V
Noise gate input current (peak value)	I_{9M}	>	30 μA
Input resistance of noise gate	R_{9-16}	typ.	200 Ω
Flyback signal input voltage (peak value)	V_{5-16M}	typ.	±1 V
Flyback signal input current (peak value)	I_{5M}	typ.	1 mA
Output signals			
Line driver output voltage (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	10 V
Line driver output current (average value)	$I_{2(AV)}$	max.	20 mA
Line driver output current (peak value)	I_{2M}	max.	200 mA
Composite sync output voltage (peak value)	V_{7-16M}	typ.	10 V

PACKAGE OUTLINE

16-lead dual in-line; plastic (SOT-38).

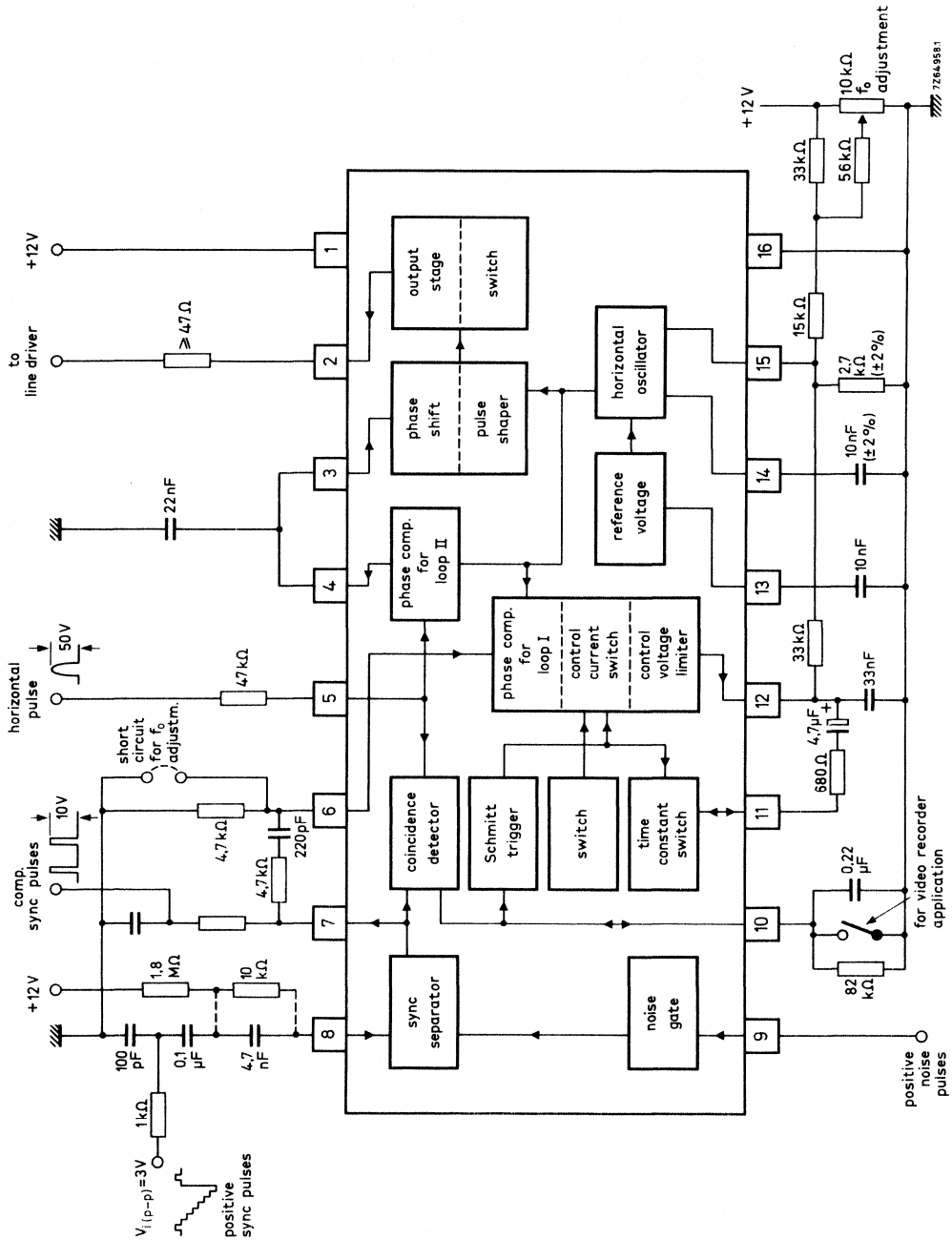


Fig. 1 Block diagram and application information.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (Vp)	V_{1-16}	max.	13,2	V
Phase shift voltage	V_{3-16}		0 to 13,2	V
Video input voltage	$-V_{8-16}$	max.	12	V
Coincidence detector voltage	V_{10-16}		−0,5 to +5	V
Line driver output current (average value)	$I_{2(AV)}$	max.	20	mA
(peak value)	I_{2M}	max.	200	mA
Horizontal pulse current (peak value)	I_{5M}	max.	10	mA
Composite sync current (peak value)	I_{7M}	max.	10	mA
Pos. sync pulse current (peak value)	I_{8M}	max.	10	mA
Noise gate current (peak value)	I_{9M}	max.	10	mA
Total power dissipation	P_{tot}	max.	600	mW*
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to + 70	°C

CHARACTERISTICS

At V_{1-16} = 12 V; T_{amb} = 25 °C. Measured in circuit of Fig. 1 (CCIR standard).

Current consumption at I_2 = 0	I_1	typ.	36	mA

Required input signals

Video signal

Input voltage (positive going sync) peak-to-peak value	$V_{i(p-p)}$	typ.	3	V
			1 to 7	V
Input current during sync pulse (peak value)	I_{8M}	typ.	100	μA

Noise gating (pin 9)

Input voltage (peak value)	V_{9-16M}	>	0,7	V
Input current (peak value)	I_{9M}	>	30	μA
		<	10	mA
Input resistance	R_{9-16}	typ.	200	Ω

Flyback pulse (pin 5)

Input voltage (peak value)	V_{5-16M}	typ.	±1	V
Input current (peak value)	I_{5M}	>	50	μA
		typ.	1	mA
Input resistance	R_{5-16}	typ.	400	Ω
Pulse duration at 15 625 Hz	t_5	>	10	μs

* 800 mW permissible while tubes are heating up.

CHARACTERISTICS (continued)

Delivered output signals

Composite sync pulses (positive; pin 7)			
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	typ.	10 V
Output resistance			
at leading edge of pulse (emitter follower)	$R_{7\text{-}16}$	$\approx$	50 Ω
at trailing edge	$R_{7\text{-}16}$	typ.	2,2 kΩ
Additional external load resistance	$R_{7\text{-}16(ext)}$	$>$	2 kΩ
Driver pulse (pin 2)			
Output voltage (peak-to-peak value)	$V_{2\text{-}16(p\text{-}p)}$	typ.	10 V
Average output current	$I_{2(AV)}$	$<$	20 mA
Peak output current	I_{2M}	$<$	200 mA
Output resistance (low ohmic)	$R_{2\text{-}16}$	typ.	2,5 or 15 Ω *
Output pulse duration when synchronized	t_2		12 to 32 μs **
Permissible delay between leading edge of output pulse and flyback pulse at t_5 = 12 μs	$t_{o\ tot}$		0 to 15 μs
Supply voltage at which output pulses are obtained	$V_{1\text{-}16}$	$>$	4 V

* Depends on switch position and polarity output current. $R_{2\text{-}16}$ = 2,5 Ω is valid for $V_{2\text{-}16}$ = +10,5 V and a load between pins 2 and 16 (e.g. an external resistor).

** The output pulse duration is adjusted by shifting the leading edge ($V_{3\text{-}16}$ from 6 V to 8 V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920S.
For a line output stage with a BU108 high-voltage transistor the resulting duration is about 22 μs, and in such a way that the line output transistor is switched on again about 8 μs after the middle of the line-flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.

Oscillator

Frequency; free running ($R_{15\text{-}16}$ = 3,3 kΩ)	f_o		15 625 Hz	*
Spread of frequency at $R_{15\text{-}16}$ = 3,3 kΩ; $C_{14\text{-}16}$ = 10 nF	$\frac{\Delta f_o}{f_o}$	<	1,5 %	**
Frequency change when decreasing the supply down to minimum 4 V	$\left\lvert\frac{\Delta f_o}{f_o}\right\rvert$	<	10 %	
Frequency control sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$	typ.	16,5 Hz/μA	
Adjustment range of frequency (in Fig. 2)	$\frac{\Delta f_o}{f_o}$	typ.	±5 %	
Influence of supply voltage on frequency at V_P = 12 V	$\frac{\delta f_o}{f_o} / \frac{\delta V_P}{V_{Pnom}}$	<	5 %	

Control loop 1 (between sync pulse and oscillator)

Control voltage range	$V_{12\text{-}16}$		0,8 to 5,5 V	
Control current (peak values)				
at $V_{10\text{-}16} > 4{,}5$ V; $V_{6\text{-}16} > 1{,}5$ V	I_{12M}	typ.	±2 mA	
at $V_{10\text{-}16} < 2$ V; $V_{6\text{-}16} > 1{,}5$ V	I_{12M}	typ.	±6 mA	
Loopgain of APC system				
a. Time coincidence between sync pulse and flyback pulse or $V_{10\text{-}16} > 4{,}5$ V	$\frac{\Delta f}{\Delta t}$	typ.	1 kHz/μs	
b. No time coincidence or $V_{10\text{-}16} < 2$ V	$\frac{\Delta f}{\Delta t}$	typ.	3 kHz/μs	
Catching and holding range	Δf	typ.	±1 kHz	▲

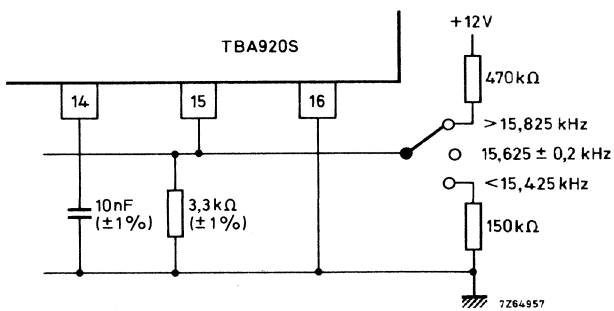


Fig. 2 Possibilities for oscillator frequency adjustment.

* The oscillator frequency can be changed for other TV standards by an appropriate value of $C_{14\text{-}16}$.

** Exclusive external components tolerances.

▲ Adjustable with $R_{12\text{-}15}$.

CHARACTERISTICS (continued)

Pull-in time for $\Delta f/f_o = \pm 3\% (\Delta f = 470$ Hz)	t	$\approx$	20	ms	(note 1)
Switch-over from large control sensitivity to small control sensitivity after catching	t	$\approx$	20	ms	(note 1)
Control loop II (between flyback pulse and oscillator)					
Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse	$t_{d\ tot}$		0 to 15	μs	
Static control error	$\frac{\Delta t}{\Delta t_d}$	$<$	0,5	%	(note 2)
Output current during flyback pulse (peak value)	I_{4M}	typ.	$\pm$0,7	mA	
Overall phase relation					
Phase relation between leading edge of sync pulse and middle of flyback pulse	t	typ.	4,9	μs	(note 3)
Tolerance of phase relation	$\lvert\Delta t\rvert$	$<$	0,4	μs	(note 4)
Voltage for $T_2 = 12$ to 32 μs	$V_{3\text{-}16}$		6 to 8	V	
Adjustment sensitivity	$\frac{\Delta T_2}{\Delta V_{3\text{-}16}}$	typ.	10	μs/V	
Input current	I_3	$<$	2	μA	
External switch-over of parameters (loop filter and loop gain) of control loop I (e.g. for video recorder application) see note 5.					
Required switch-over voltage					
at $R_{11\text{-}16} = 150\ \Omega$	$V_{10\text{-}16}$	$>$	4,5	V	
at $R_{11\text{-}16} = 2$ kΩ	$V_{10\text{-}16}$	$<$	2	V	
Required switch-over current					
at $R_{11\text{-}16} = 150\ \Omega$; $V_{10\text{-}16} = 4,5$ V	I_{10}	typ.	80	μA	(note 5)
at $R_{11\text{-}16} = 2$ kΩ; $V_{10\text{-}16} = 2$ V	I_{10}	typ.	120	μA	

1. See Fig. 1.
2. The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
3. This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picuture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black-and-white sets), then the phase relation is achieved at $C_{5\text{-}16} = 560$ pF.
4. The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a d.c. voltage to pin 3.
5. With sync pulses at pin 7 and 8; without RC network at pin 10.

4 W AUDIO POWER AMPLIFIER WITH D.C. VOLUME CONTROL

The TDA1013A is a monolithic integrated audio amplifier circuit with d.c. volume control in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit very suitable for applications in mains-fed apparatus such as television receivers and record players.

The d.c. volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control can be obtained by means of a variable d.c. voltage between 3,5 and 8 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop gain. This offers an optimum in number of external components, performance and stability.

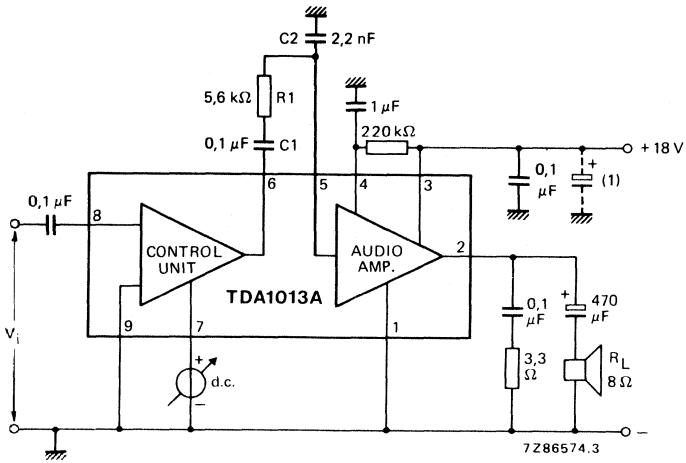
The SIL package (SOT-110B) offers a simple and low-cost heatsink connection.

QUICK REFERENCE DATA

Supply voltage range	V_P	15 to 35	V
Repetitive peak output current	I_{ORM}	max. 1,5	A
Total sensitivity (d.c. control at max. gain) for P_o = 2,5 W	V_i	typ. 55	mV
Audio amplifier			
Output power at d_{tot} = 10% V_P = 18 V; R_L = 8 Ω	P_o	typ. 4,5	W
Total harmonic distortion at P_o = 2,5 W; R_L = 8 Ω	d_{tot}	typ. 0,5	%
Sensitivity for P_o = 2,5 W	V_i	typ. 125	mV
D.C. volume control unit			
Gain control range	ϕ	> 80	dB
Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB)	V_i	> 1,2	V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ. 55	mV
Input impedance (pin 8)	$\lvert Z_i \rvert$	typ. 250	kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).



(1) Belongs to power supply.

Fig. 1 Basic application diagram also used as test circuit with R1 = 5,1 kΩ and C1 = 22 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Storage temperature	T_{stg}		−55 to + 150 °C
Crystal temperature	T_j		−25 to + 150 °C
Total power dissipation	see derating curve Fig. 2		

HEATSINK DESIGN

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C (max.); T_j = 150 °C (max); for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,5 W.
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2,5} = 36\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 − (9 + 1) = 26 K/W.

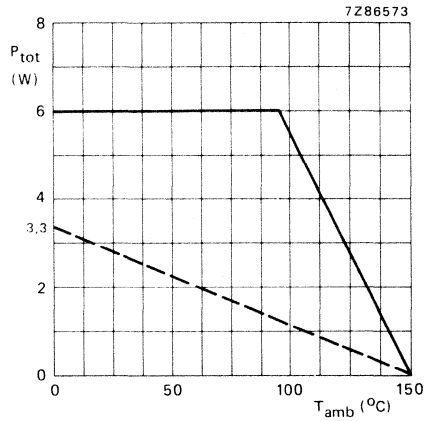


Fig. 2 Power derating curve.
——— infinite heatsink;
– – – without heatsink.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

Supply voltage	V_P	typ.	18	V
			15 to 35	V
Total quiescent current	I_{tot}	typ.	35	mA
Noise output voltage (see also note)	V_n	<	1,4	mV
Total sensitivity (d.c. control at maximum gain) for P_o = 2,5 W	V_i		38 to 69	mV
		typ.	55	mV
Frequency response (–3 dB)	f		35 Hz to 20	kHz
Audio amplifier				
Repetitive peak output current	I_{ORM}	<	1,5	A
Output power at d_{tot} = 10%	P_o	>	4	W
		typ.	4,5	W
Total harmonic distortion at P_o = 2,5 W	d_{tot}	typ.	0,5	%
		<	1	%
Voltage gain	G_v	typ.	30	dB
Sensitivity for P_o = 2,5 W	V_i	typ.	125	mV
Input impedance (pin 5)	$\|Z_i\|$	>	100	kΩ
		typ.	250	kΩ

Note

Measured in a bandwidth according to IEC 179-curve 'A'; R_S = 5 kΩ and d.c. control at minimum gain.

CHARACTERISTICS (continued)

D.C. volume control unit

Gain control range (see also Fig. 3)	ϕ	>	80 dB
Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB)	V_i	>	1,2 V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ.	55 mV
Input impedance (pin 8)	$\|Z_i\|$	>	100 kΩ
		typ.	250 kΩ
Output impedance (pin 6)	$\|Z_o\|$		100 to 400 Ω
		typ.	200 Ω

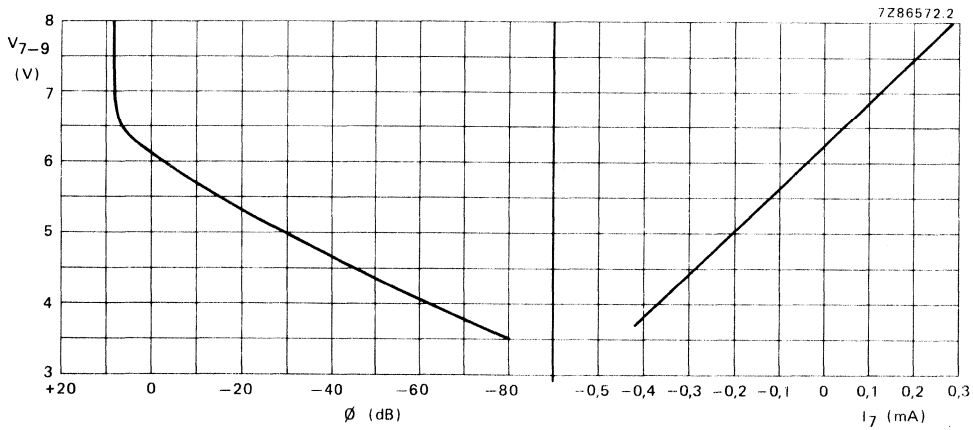


Fig. 3 Typical values gain control; V_i at pin 7.

1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 18	V
Peak output current	I_{OM}	max. 2,5	A
Output power at d_{tot} = 10%			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ. 0,3	%
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	> 100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ. 20	kΩ
Total quiescent current	I_{tot}	typ. 14	mA
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

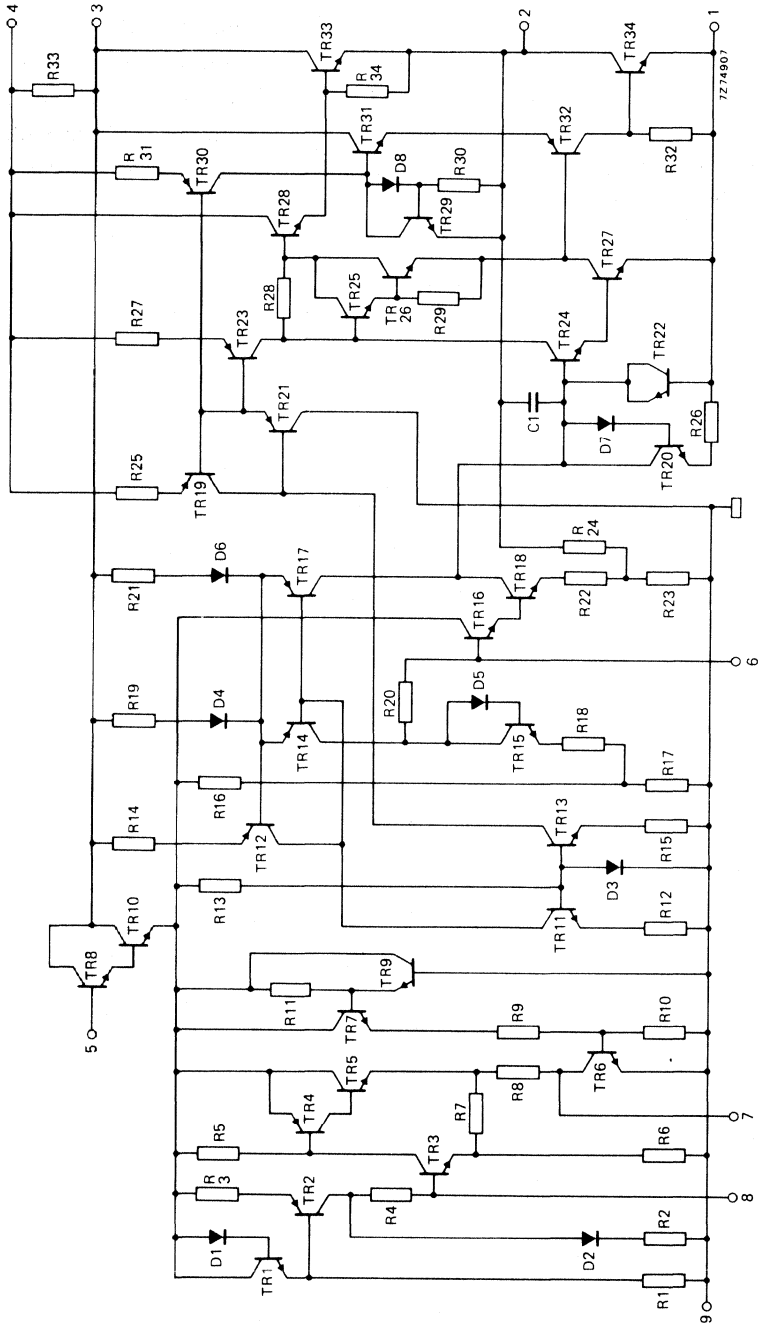


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Peak output current	I_{OM}	max.	2,5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

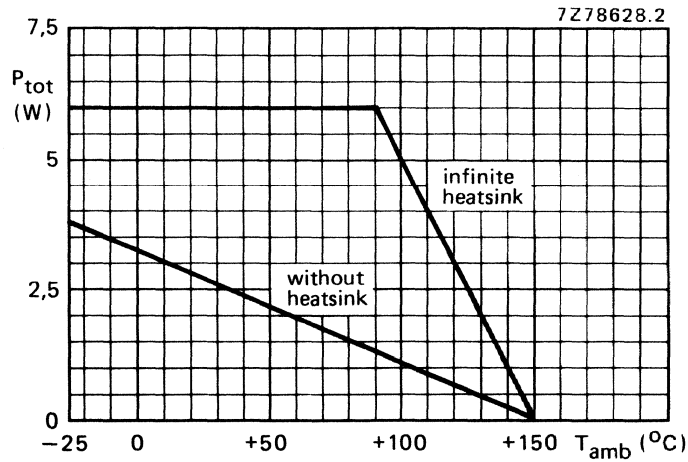


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 45 °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 45}{1,8} = 58\ K/W.$$

Where $R_{th\ j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

D.C. CHARACTERISTICS

Supply voltage range	V_P	3,6 to 18	V
Repetitive peak output current	I_{ORM}	< 2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. 14 < 25	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
without bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 3,0	W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ. 23	dB
power amplifier	G_{v2}	typ. 29	dB
total amplifier	$G_{v\,tot}$	typ. 52 49 to 55	dB dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. 0,3 < 1,0	% %
Frequency response; −3 dB (note 3)	B	60 Hz to 15	kHz
Input impedance:			
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	> 100 typ. 200	kΩ kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ. 20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ. 1	kΩ
Output voltage preamplifier (r.m.s. value)			
d_{tot} < 1% (note 2)	$V_{o(rms)}$	typ. 0,8	V
Noise output voltage (r.m.s. value; note 5)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. 0,5	mV
Noise output voltage at f = 500 kHz (r.m.s. value)			
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ. 8	μV
Ripple rejection (note 6)			
f = 100 Hz	RR	typ. 38	dB

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_O = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

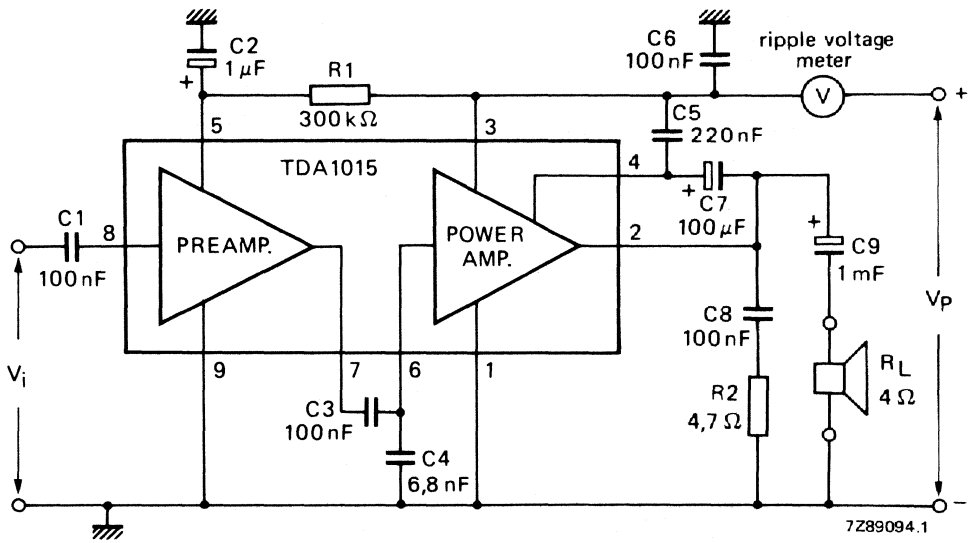


Fig. 3 Test circuit.

APPLICATION INFORMATION

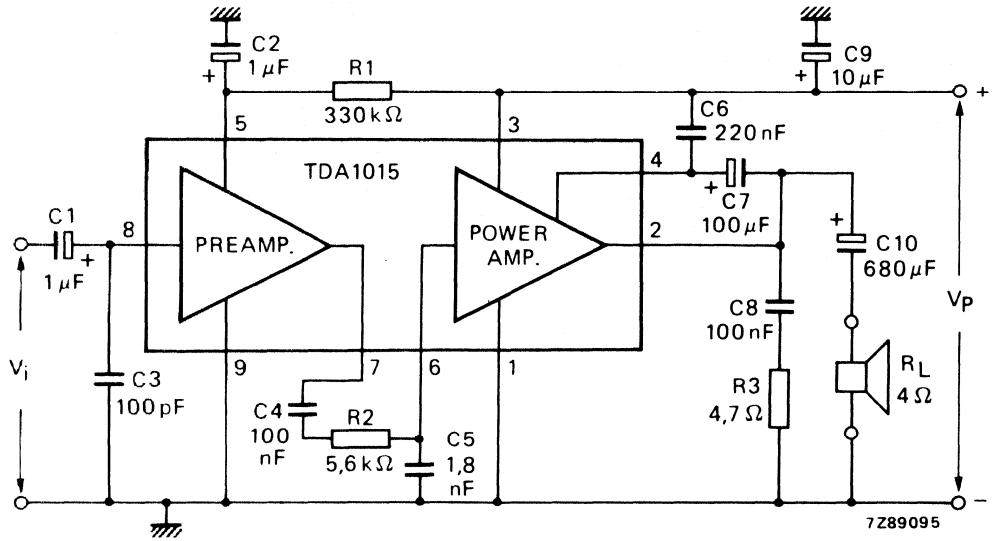


Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

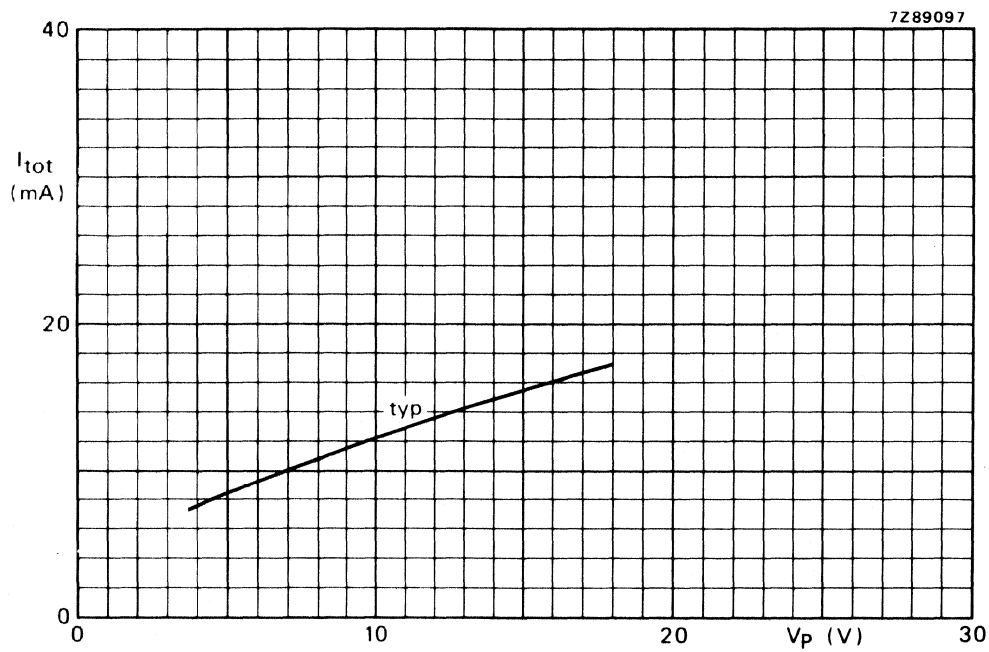


Fig. 5 Total quiescent current as a function of supply voltage.

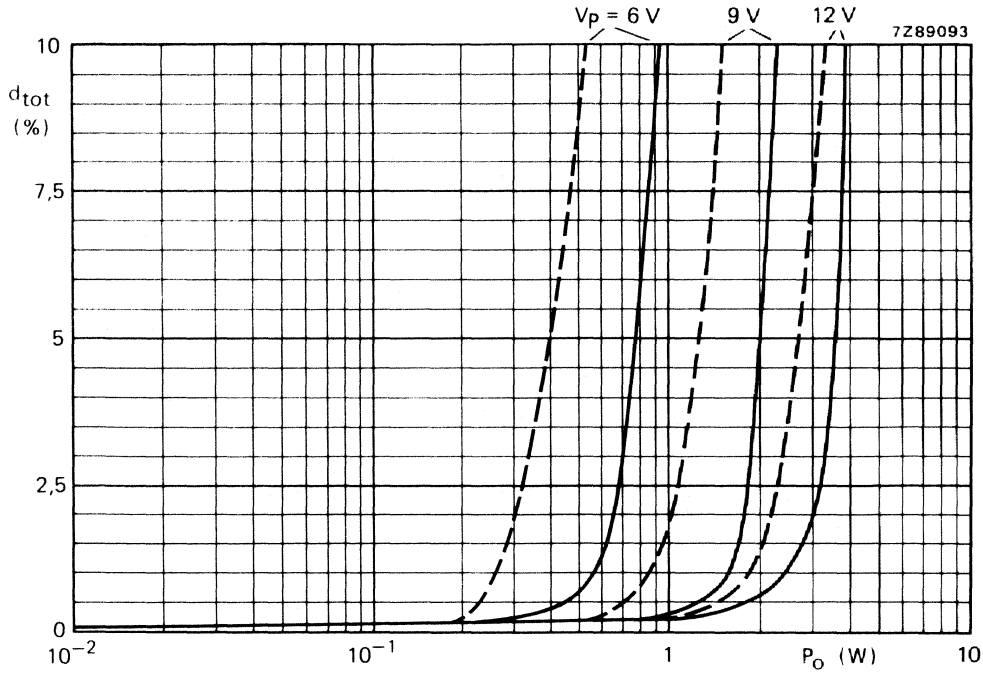


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

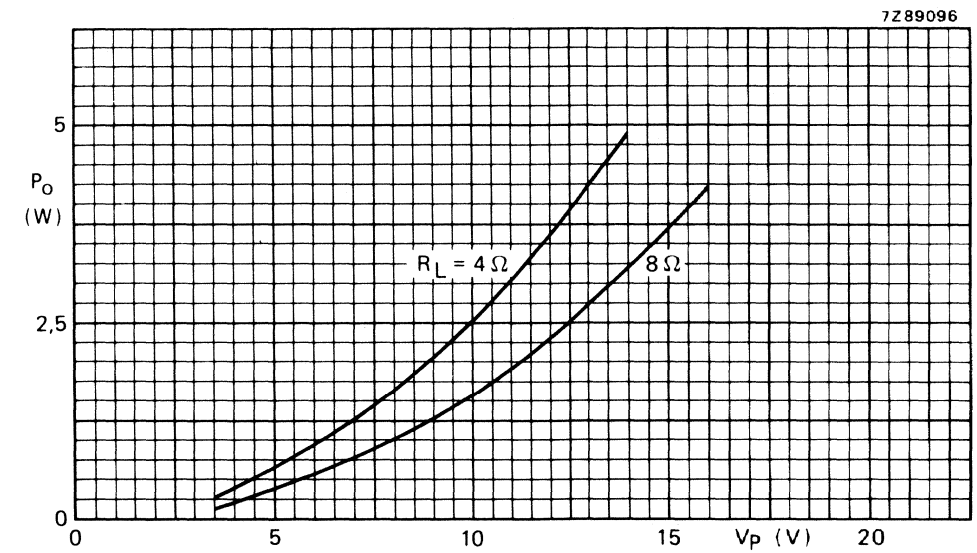


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

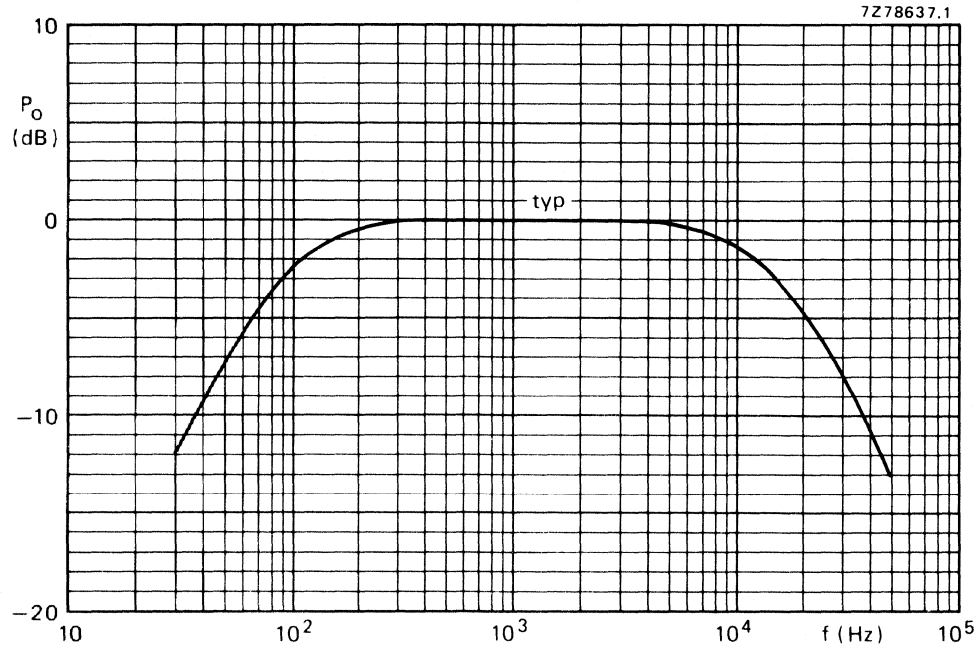


Fig. 8 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

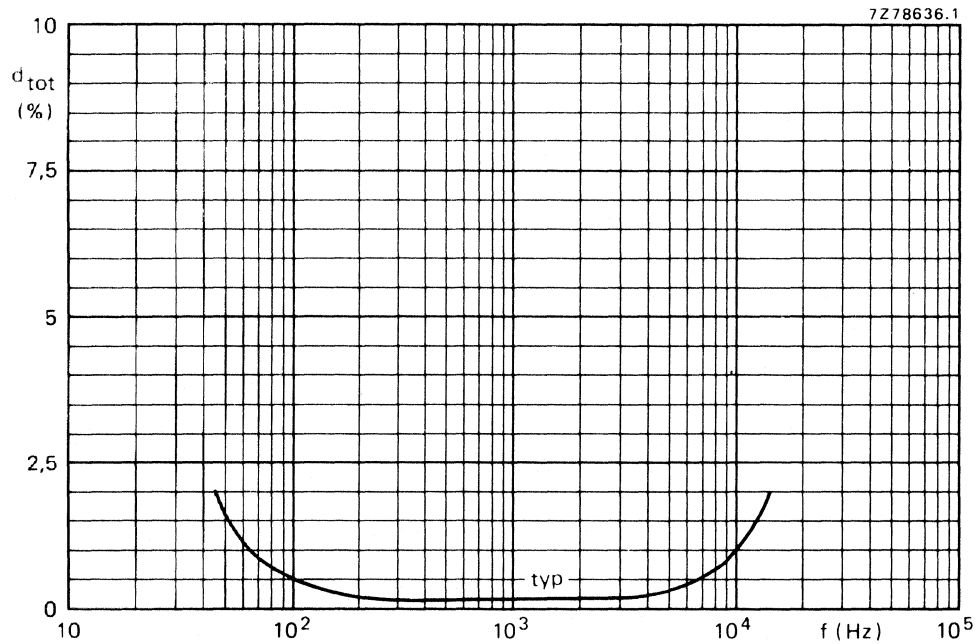


Fig. 9 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

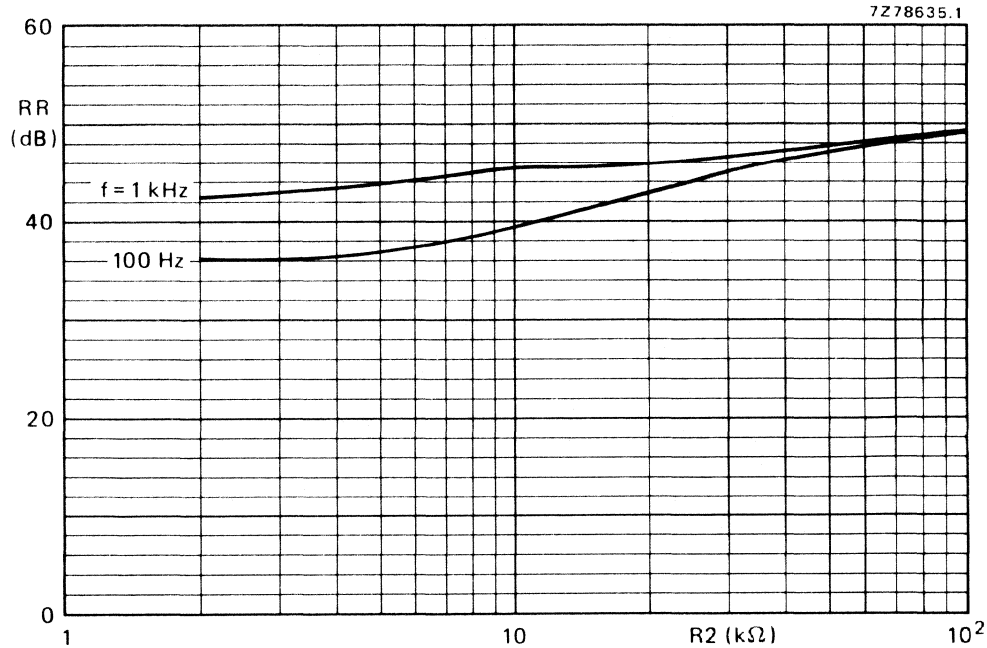


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

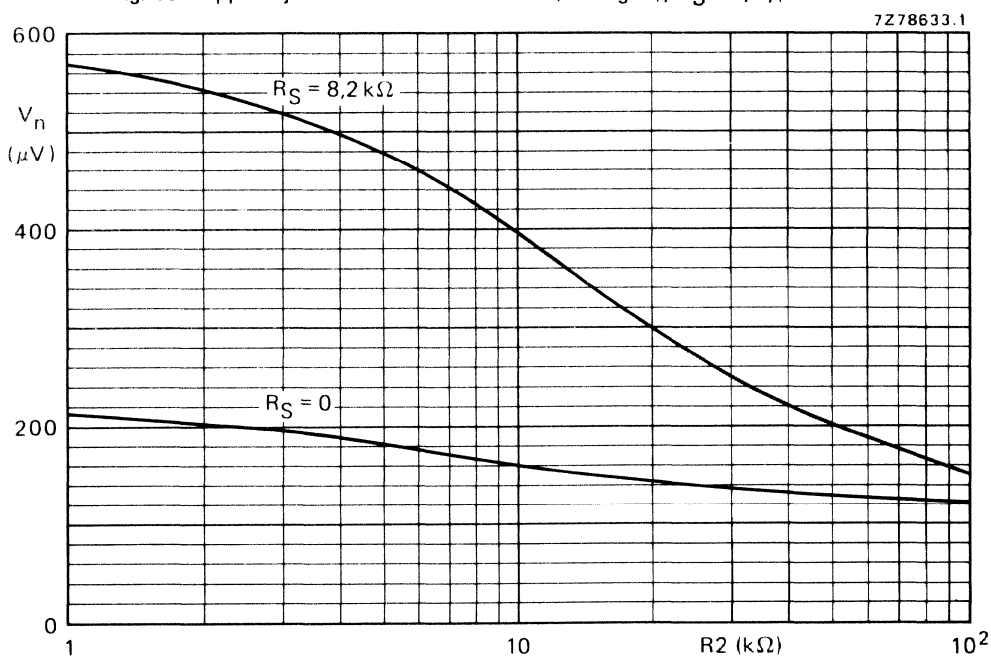


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

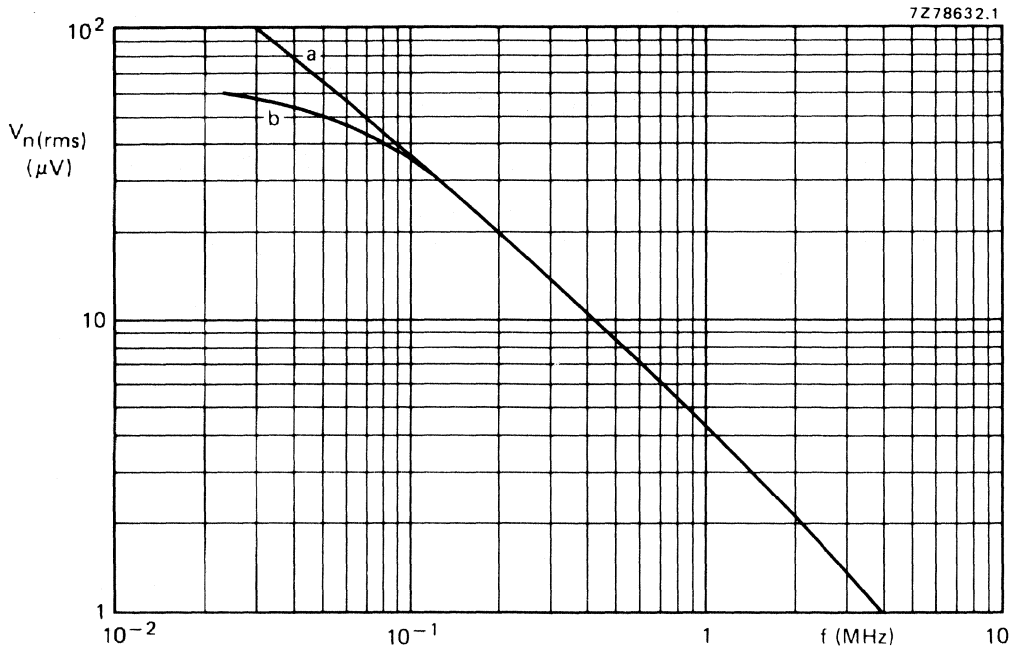


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

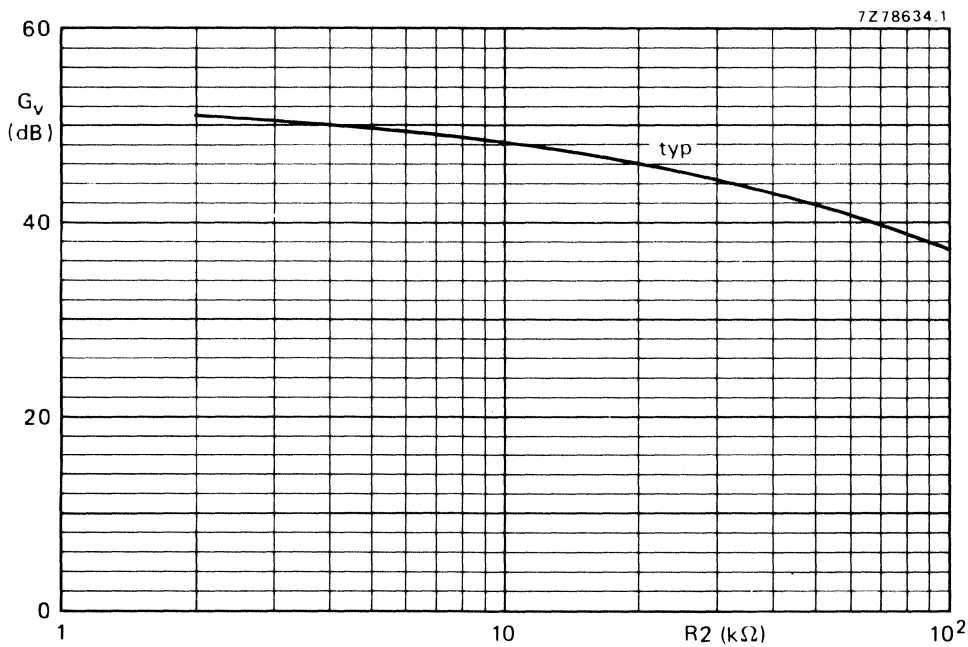


Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

0,5 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 12	V
Peak output current	I_{OM}	max.	1	A
Output power	P_o	typ.	0,5	W
Voltage gain power amplifier	G_{v1}	typ.	29	dB
Voltage gain preamplifier	G_{v2}	typ.	23	dB
Total quiescent current	I_{tot}	max.	22	mA
Operating ambient temperature range	T_{amb}		−25 to +150	°C
Storage temperature range	T_{stg}		−55 to +150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO-8; SOT-96A).

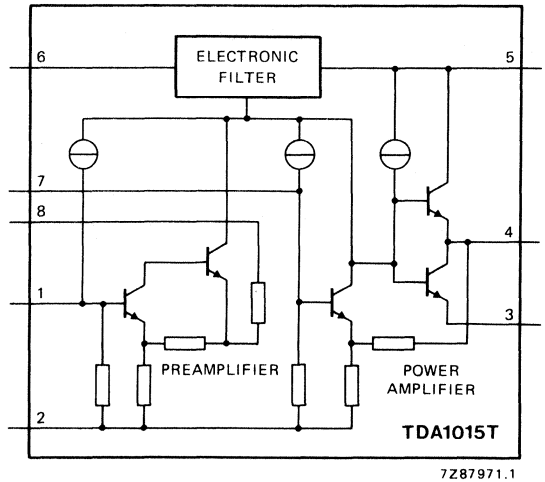


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	12 V
Peak output current	I_{OM}	max.	1 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range			−55 to +150 °C
A.C. short-circuit duration of load during sine-wave drive at V_P = 9 V	t_{sc}	max.	1 hour

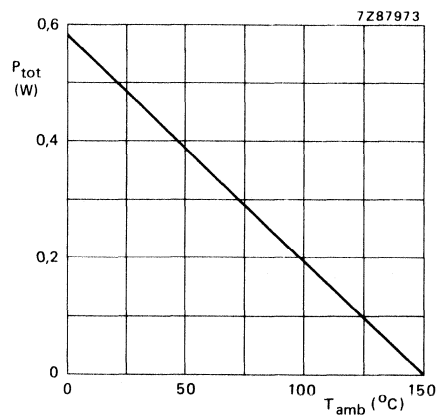


Fig. 2 Power derating curve.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 9 V; R_L = 16 Ω; f = 1 kHz; see Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_P	3,6	9	12	V
Repetitive peak output current	I_{ORM}	–	–	1	A
Total quiescent current	I_{tot}	–	12	22	mA
A.F. output power at d_{tot} = 10% (note 1)					
V_P = 9 V; R_L = 16 Ω	P_o	–	0,5	–	W
V_P = 6 V; R_L = 8 Ω	P_o	–	0,3	–	W
Voltage gain power amplifier	G_{v1}	–	29	–	dB
Voltage gain preamplifier (note 2)	G_{v2}	–	23	–	dB
Total voltage gain	G_{tot}	49	52	55	dB
Frequency response at −3 dB (note 3)	B	–	60 to 15 000	–	Hz
Input impedance power amplifier	$\|Z_{i1}\|$	–	20	–	kΩ
Input impedance preamplifier (note 4)	$\|Z_{i2}\|$	100	200	–	kΩ
Output impedance preamplifier	$\|Z_{o2}\|$	0,5	1	1,5	kΩ
Output voltage preamplifier (r.m.s. value) $d_{tot} < 1\%$ (note 2)	$V_{o2(rms)}$	–	0,7	–	V
Noise output voltage (r.m.s. value) (note 5)					
R_S = 0 Ω	$V_{n(rms)}$	–	0,2	–	mV
R_S = 10 kΩ	$V_{n(rms)}$	–	0,5	–	mV
Noise output voltage (r.m.s. value) f = 500 kHz; B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	–	8	–	μV
Ripple rejection at f = 100 Hz; C2 = 1 μF (note 6)	RR	–	38	–	dB

Notes to the characteristics

1. Output power is measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistance of 20 kΩ.
3. The frequency response is mainly determined by the capacitors, C1, C3 (low frequency) and C4 (high frequency).
4. Independent of load impedance of preamplifier.
5. Effective unweighted r.m.s. noise voltage measured in a bandwidth from 60 Hz to 15 kHz (slopes 12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude of 2 V).

APPLICATION INFORMATION

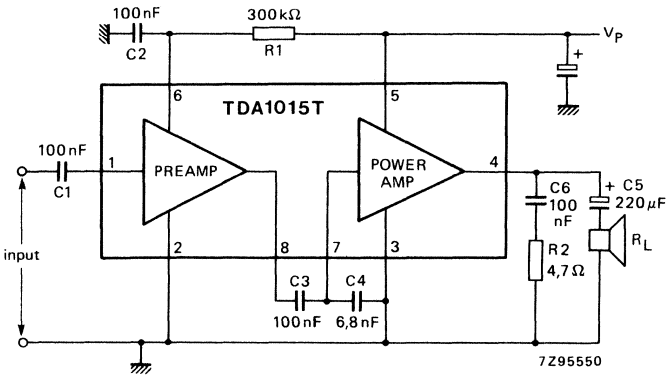


Fig. 3 Test circuit.

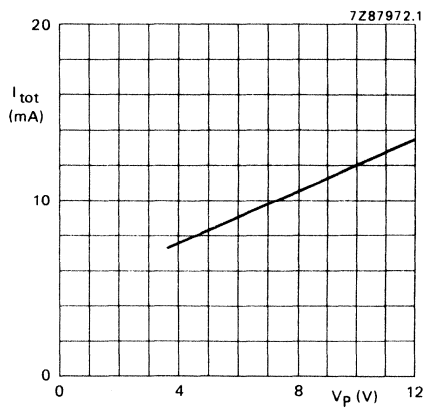


Fig. 4 Total quiescent current as a function of supply voltage.

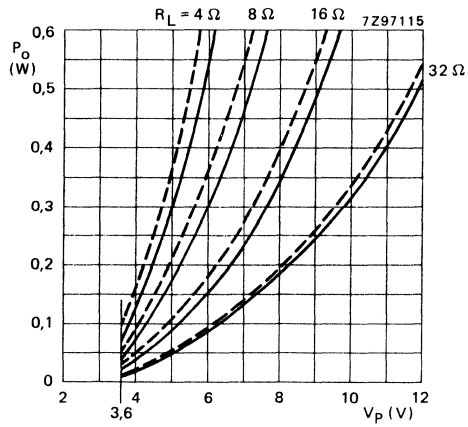


Fig. 5 Output power as a function of supply voltage; d_{tot} = 10%; f = 1 kHz.
——— measured in Fig. 3
– – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

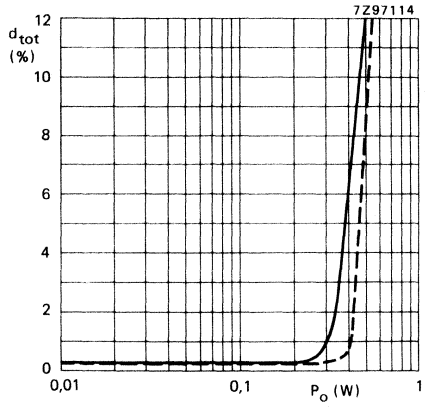


Fig. 6 Total distortion as a function of output power; V_P = 9 V; R_L = 16 Ω; f = 1 kHz.
——— measured in Fig. 3
– – – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

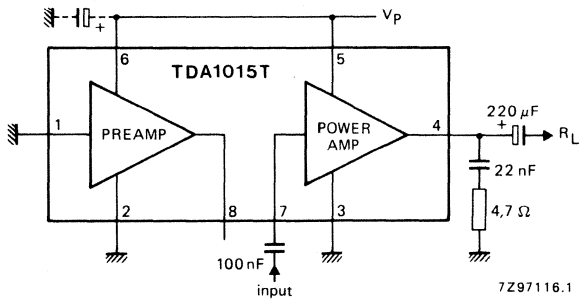


Fig. 7 Application circuit for power stage only and battery power supply; G_{v1} = 29 dB; $|Z_{i1}|$ = 20 kΩ.

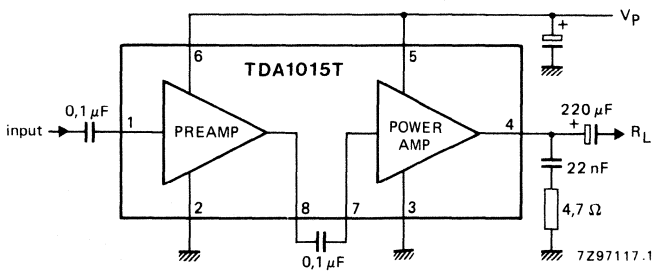


Fig. 8 Application circuit for preamplifier and power amplifier stages and battery power supply; $G_{v\,tot}$ = 52 dB; $|Z_{i2}|$ = 200 kΩ.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P	6 to 23	V
Operating ambient temperature	T_{amb}	−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ. 20	V
Current consumption	I_{14}	typ. 3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ. 6	V
Voltage gain	G_v	typ. 1	
Total harmonic distortion	d_{tot}	typ. 0,01	%
Crosstalk	α	typ. 70	dB
Signal-to-noise ratio	S/N	typ. 120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

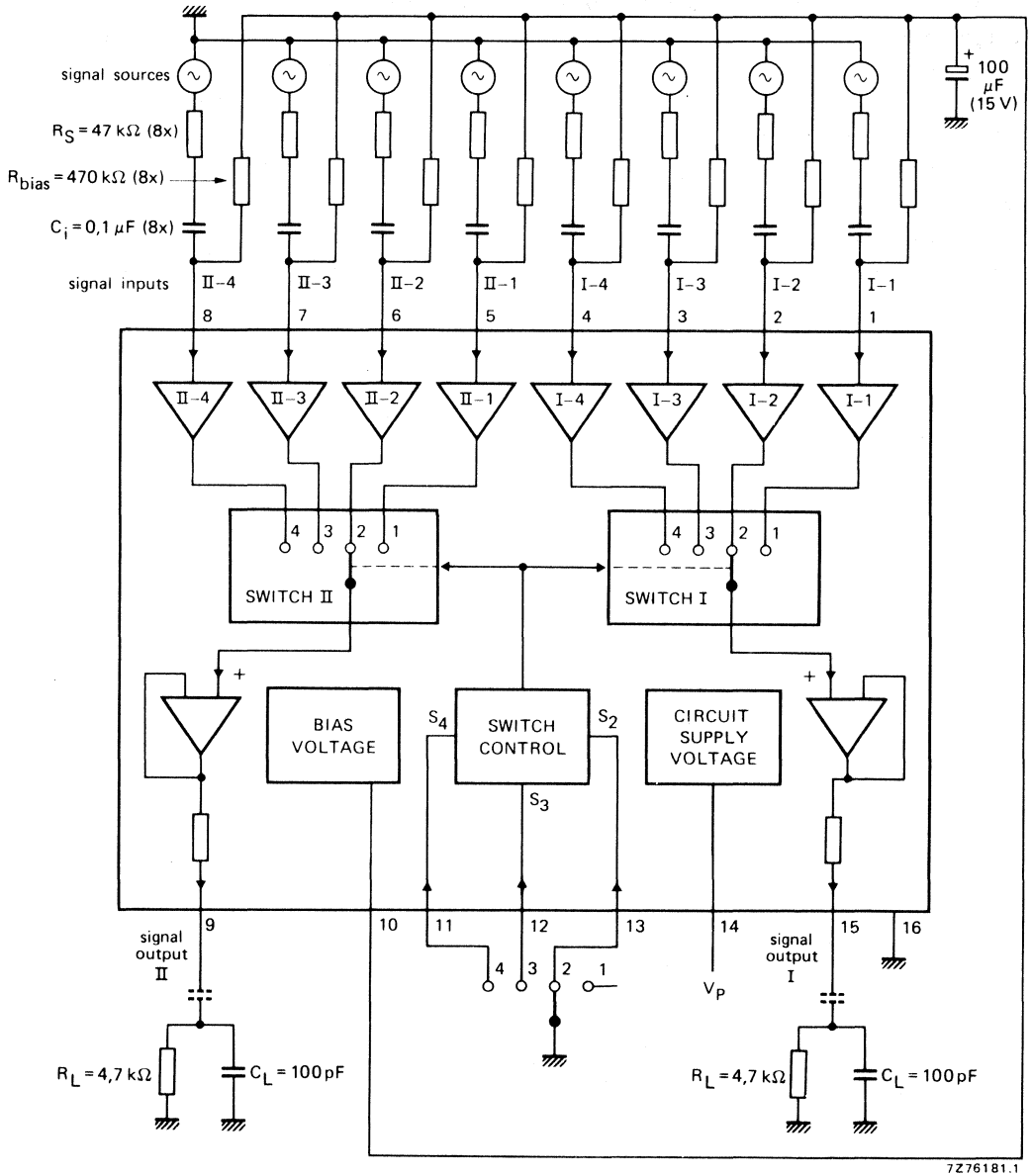


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 20 V; T_{amb} = 25 °C; unless otherwise specified

Current consumption				
without load; $I_g = I_{15} = 0$	I_{14}	typ.	3,5	mA
			2 to 5	mA
Supply voltage range (pin 14)	V_P		6 to 23	V
Signal inputs				
Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ	V_{io}	typ.	2	mV
		<	10	mV
Input offset current of switched-on inputs	I_{io}	typ.	20	nA
		<	200	nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ.	20	nA
		<	200	nA
Input bias current independent of switch position	I_i	typ.	250	nA
		<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	μV/V
Equivalent input noise voltage R_S = 0; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	μV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at R_S = 1 kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_9$; $\pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; R_S = 1 kΩ; R_L = 10 MΩ; C_L = 10 pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9\text{-}16}/\Delta t$; $\Delta V_{15\text{-}16}/\Delta t$ R_L = 10 MΩ; C_L = 10 pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	$V_{10\text{-}16}$	typ. 10,2 to 11,8	11 V * V
Output resistance	$R_{10\text{-}16}$	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

* $V_{10\text{-}16}$ is typically $0{,}5 \cdot V_{14\text{-}16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5 dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 mV 100 mV
Total harmonic distortion			
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01 %
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02 %
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03 %
Output signal handling			
d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 V 5,3 V
Noise output voltage (unweighted)			
f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5 μV
Noise output voltage (weighted)			
f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12 μV
Amplitude response			
V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1 dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75 dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90 dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

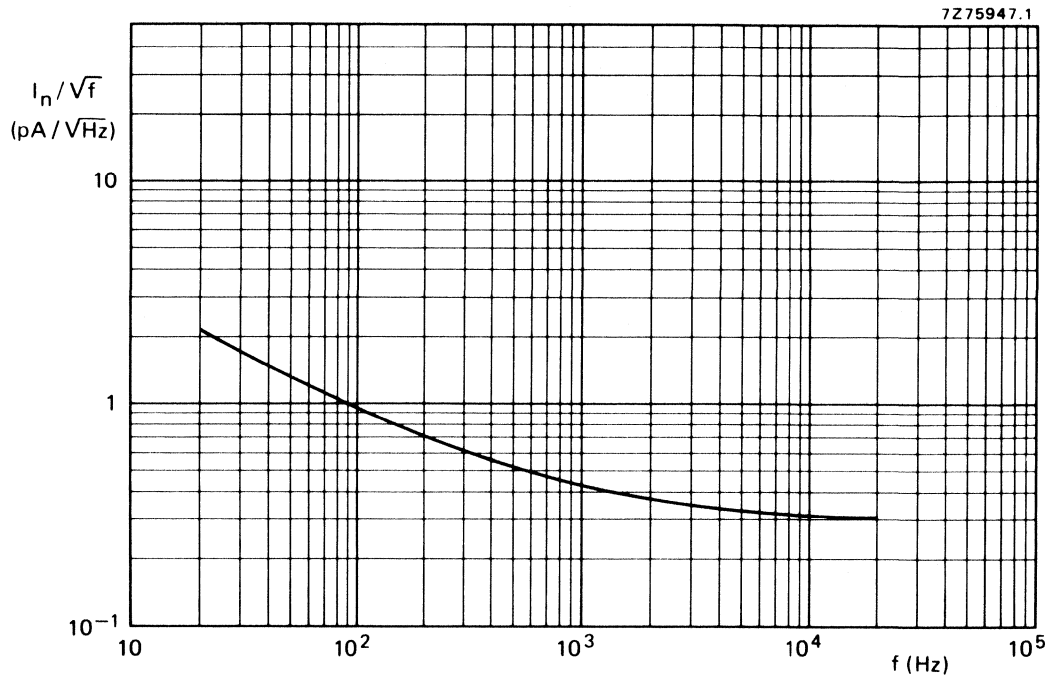


Fig. 2 Equivalent input noise current.

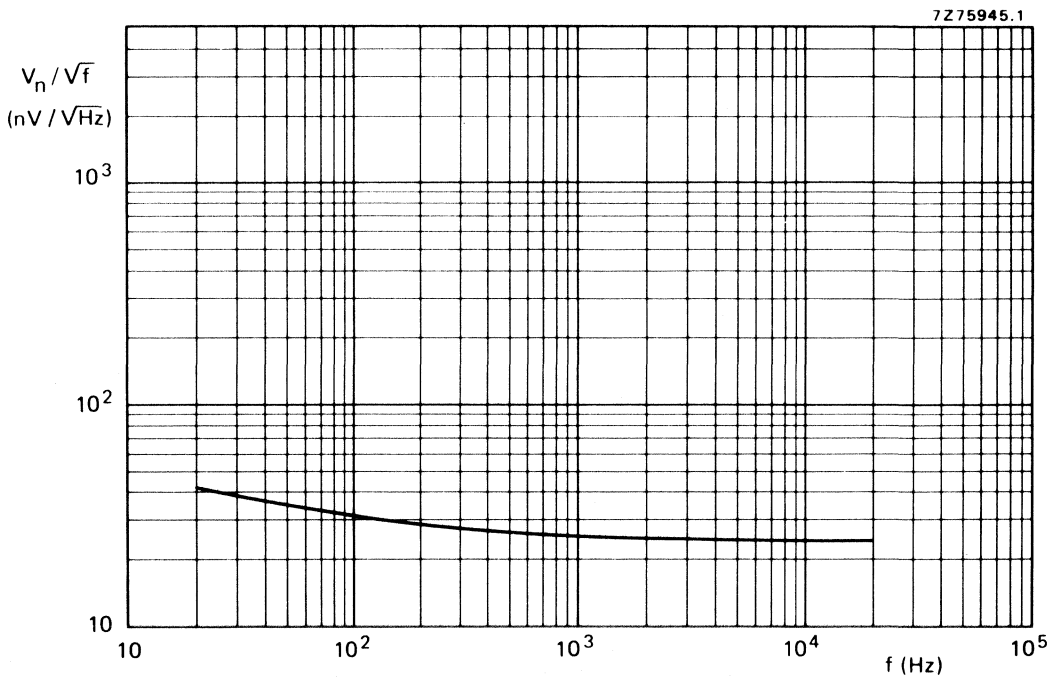


Fig. 3 Equivalent input noise voltage.

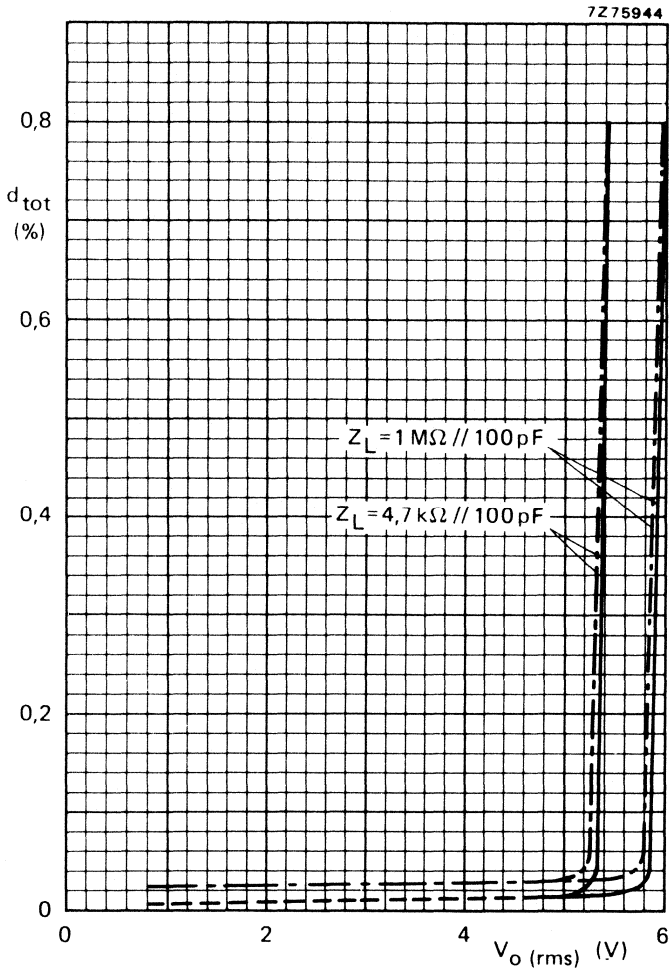


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; —— · —— · f = 20 kHz.

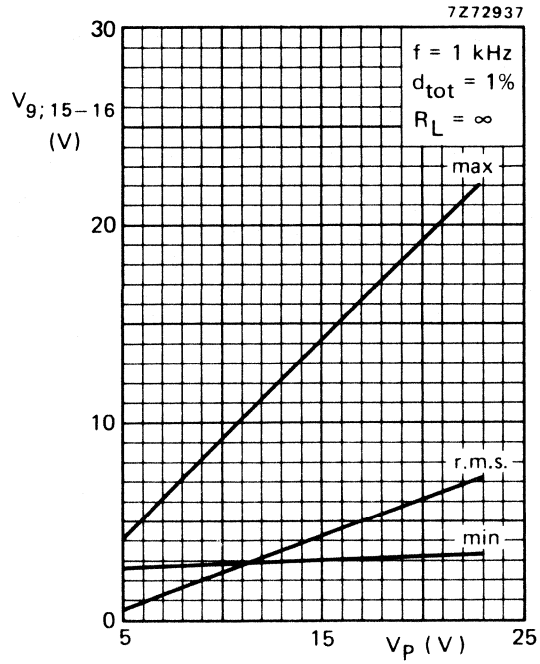


Fig. 5 Output voltage as a function of supply voltage.

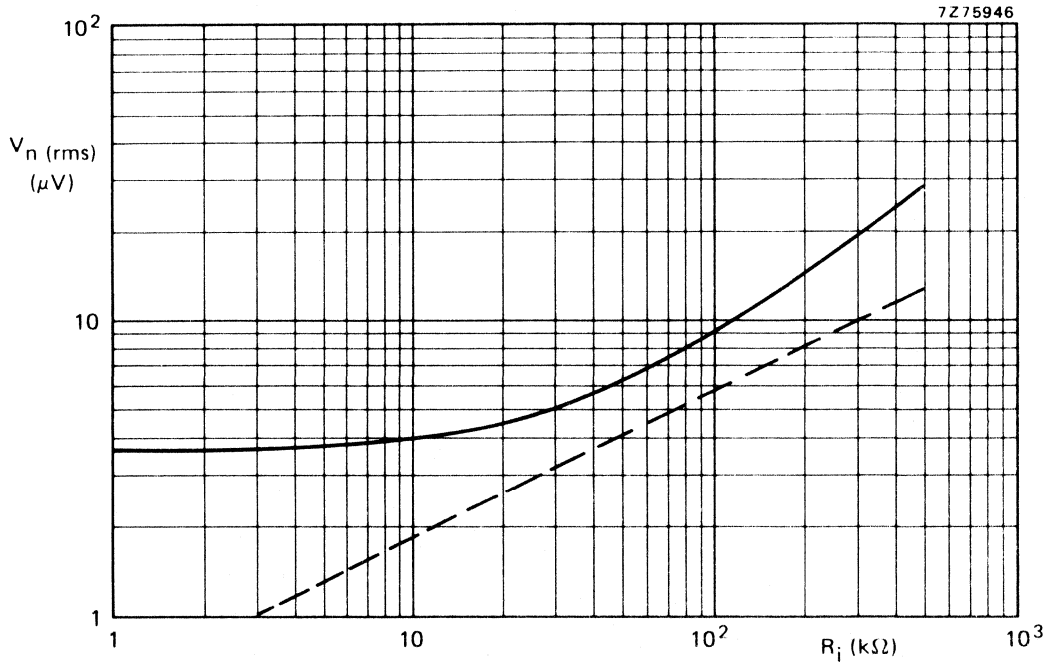


Fig. 6 Noise output voltage as a function of input resistance; G_v = 1; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

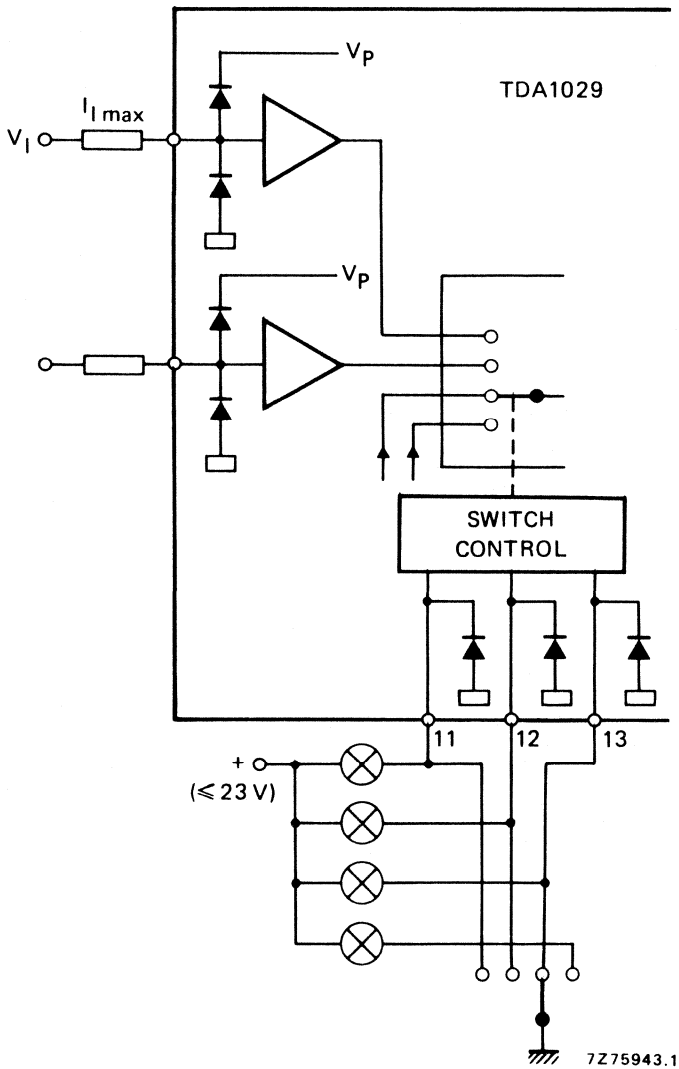


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

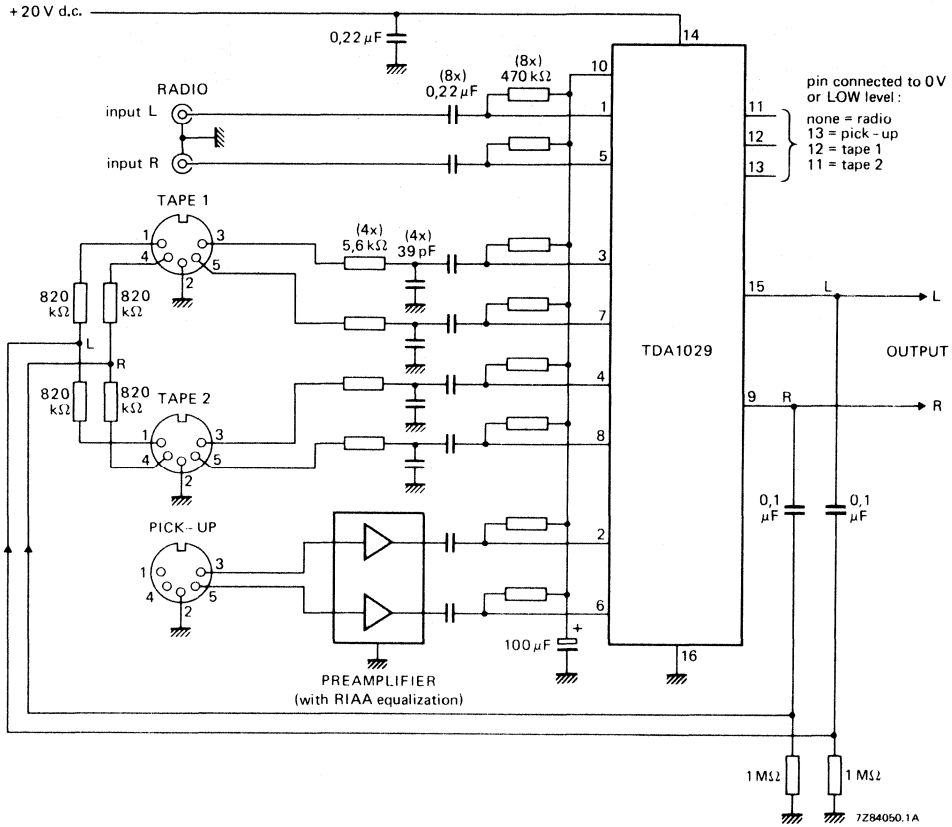


Fig. 8 TDA1029 connected as a four input stereo source selector.

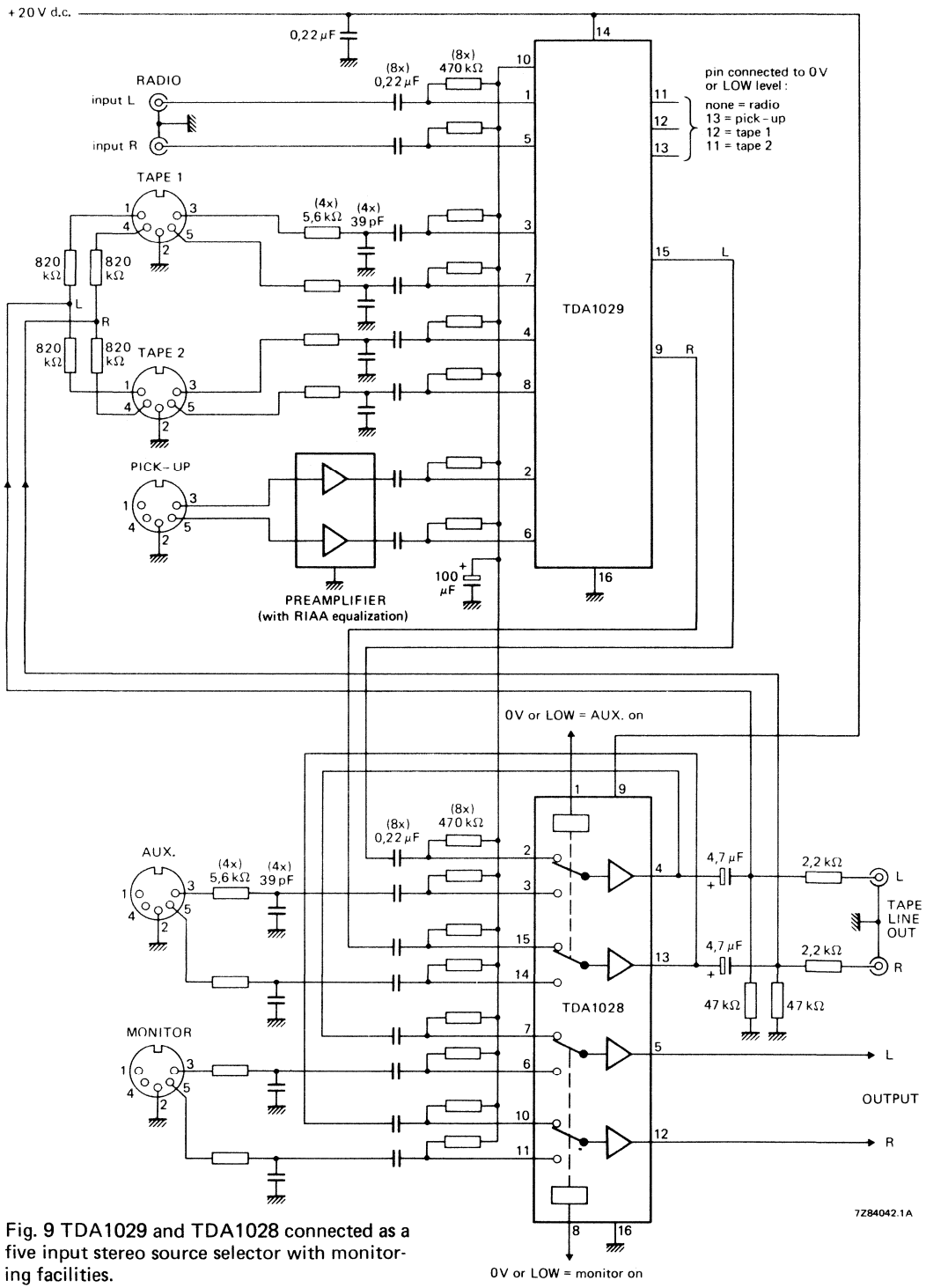


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

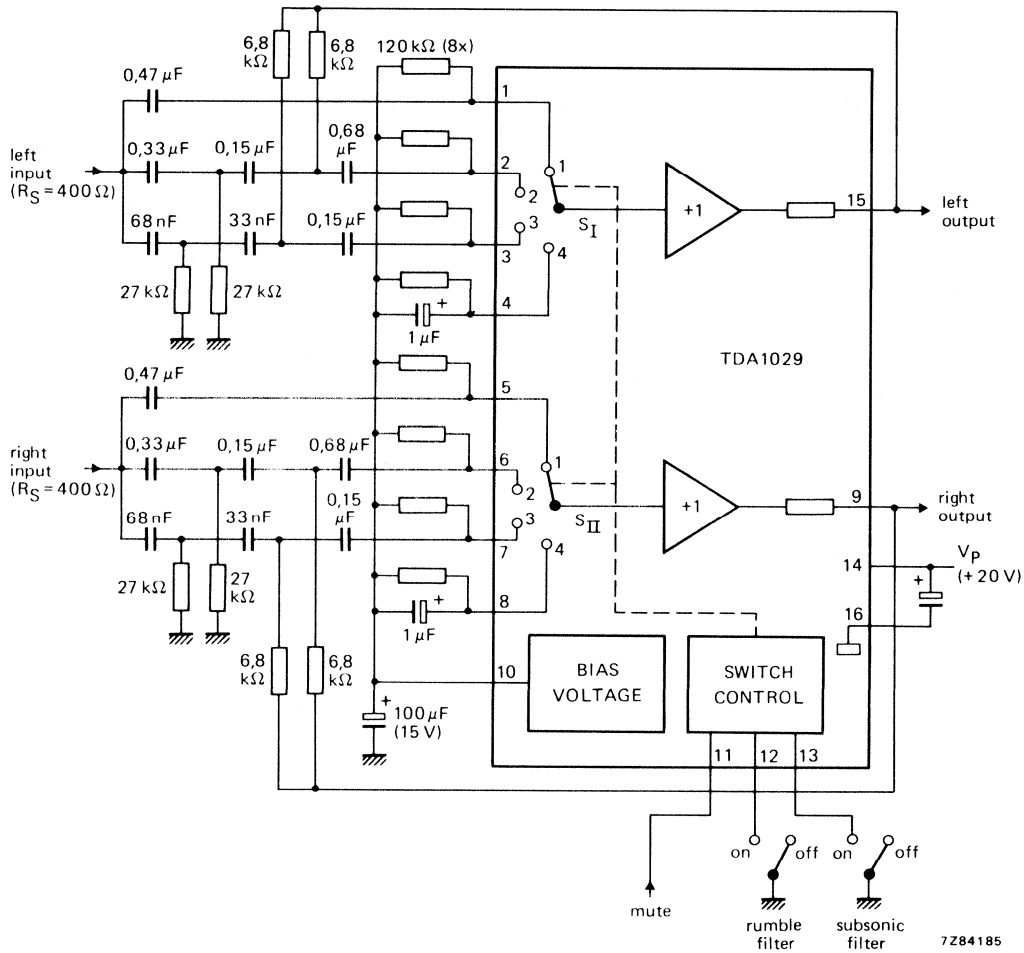


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

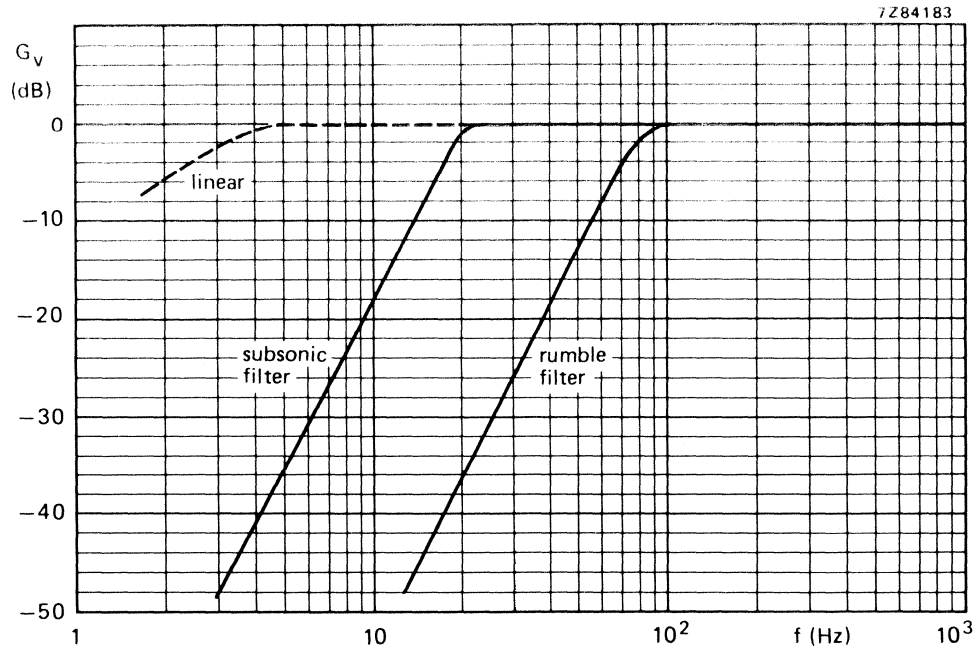


Fig. 11 Frequency response curves for the circuit of Fig. 10.

EAST-WEST CORRECTION DRIVER CIRCUIT

The TDA1082 is a monolithic integrated circuit driving east-west correction of colour tubes in television receivers. The circuit can be used for class-A and class-D operation and incorporates the following functions:

- differential input amplifier
- squaring stage
- differential output amplifier with driver stage
- protection stage with threshold
- switching off the correction during flyback
- voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 1)	V_P	typ.	12 V
Current consumption	I_P	typ.	17 mA
Total power dissipation	P_{tot}	max.	600 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C
Collector voltage drift external transistor	ΔV_C	typ.	0,7 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

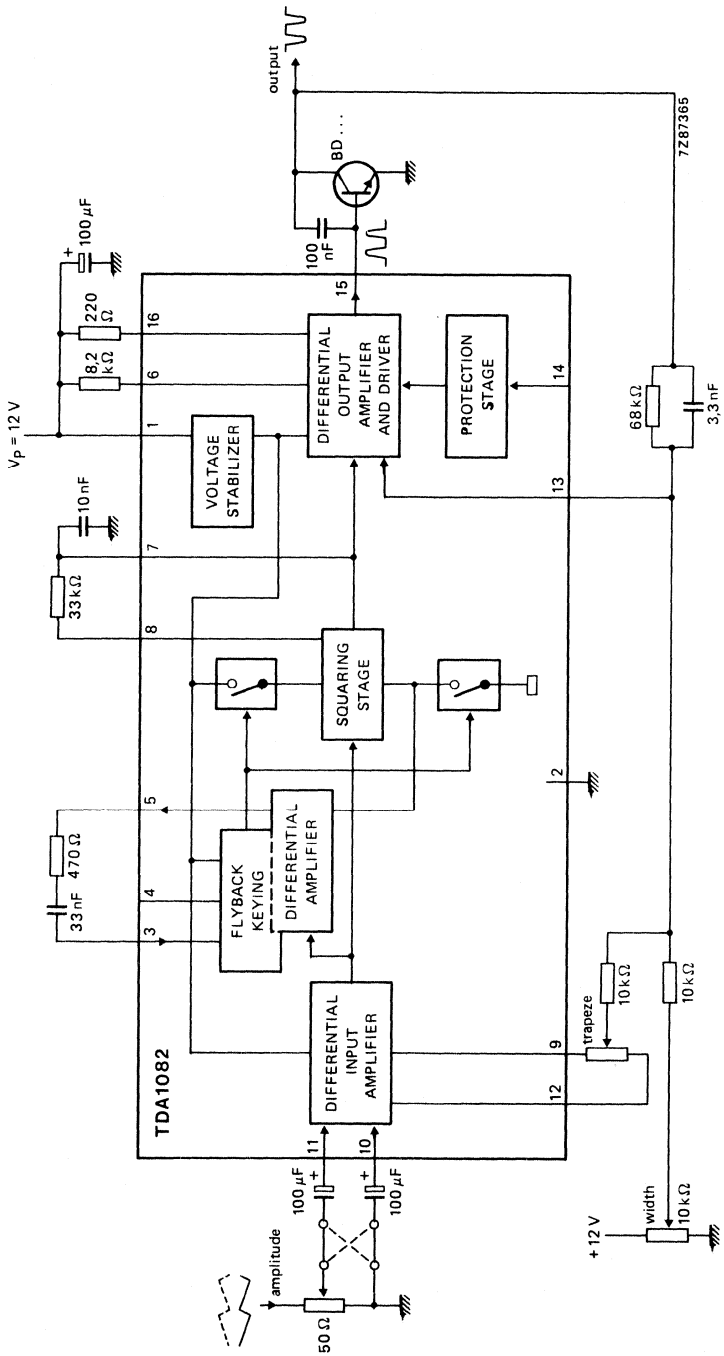


Fig. 1 Block diagram with external components (class-A operation). Also used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	V_P	max.	16 V
Output current (pin 15)	$-I_O$	max.	50 mA
Total power dissipation	P_{tot}	max.	600 mW
Storage temperature range	T_{stg}	−25 to +150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

Voltages

with respect to ground (pin 2)		min.	max.
Pins 1, 5, 7, 8, 9, 12, 13 and 16		0	16 V
Pins 3 and 4		0	— V
Pins 10, 11 and 15		0	5 V

Currents

Pins 3, 4 and 6		—	5 mA
Pin 14		0	1,5 mA
Pins 15 and 16 ($-I_{15}$ and $+I_{16}$)		0	50 mA

CHARACTERISTICS

V_P = 12 V (range 10,5 to 14 V); T_{amb} = 25; measured in circuit Fig. 1 with colour tube A66-500X; unless otherwise specified

Supply

Voltage range	V_P	10,5 to	14 V
Voltage peak value	V_{PM}	max.	15 V
Current range	I_P	11 to	30 mA
Current typical value	I_P	typ.	17 mA

Sawtooth signal (pin 10 or 11)

Input voltage d.c. value	V_i	typ.	2,5 V
Input resistance	R_i	typ. <	5,6 kΩ 7,0 kΩ

Correcting signals (pin 13)

Input voltage d.c. value	V_{13}	typ.	0,6 V
Input current	I_{13}	typ.	0,5 mA

Flyback keying (pin 3)

Input current range	I_3	0,05 to	5 mA
Peak value, d = 5%	I_3	typ.	20 mA

Threshold (pin 14)

Input voltage at I_{14} = 200 μA for switching off the driver stage	V_i	typ. 7,2 to	8 V 8,8 V

Output stage (pin 6)			
Generator current	I_6	typ.	1 mA
Flyback differential amplifier (pin 5)			
D.C. value output voltage	V_5	typ.	6 V
Output resistance	R_5	typ.	5,6 kΩ
Squaring stage (pin 7)			
D.C. value output voltage	V_7	typ.	6 V
Peak to peak value output voltage	$V_{7(p-p)}$	typ.	1,5 V
Output resistance	R_7	5,6 to typ.	9,4 kΩ 7,5 kΩ
Correction trapezoidal deformation (pins 9 and 12)			
D.C. voltage	$V_{9,12}$	typ.	5 V
Output resistance	$R_{9,12}$	typ.	7,5 kΩ
Driver output (pin 15)			
Output current	$-I_{15}$	<	50 mA
Drift of d.c. collector voltage			
Of external transistor in closed loop T_{amb} = 15 to 70 °C; V_{CO} = 8 V	ΔV_C	typ.	0,7 V

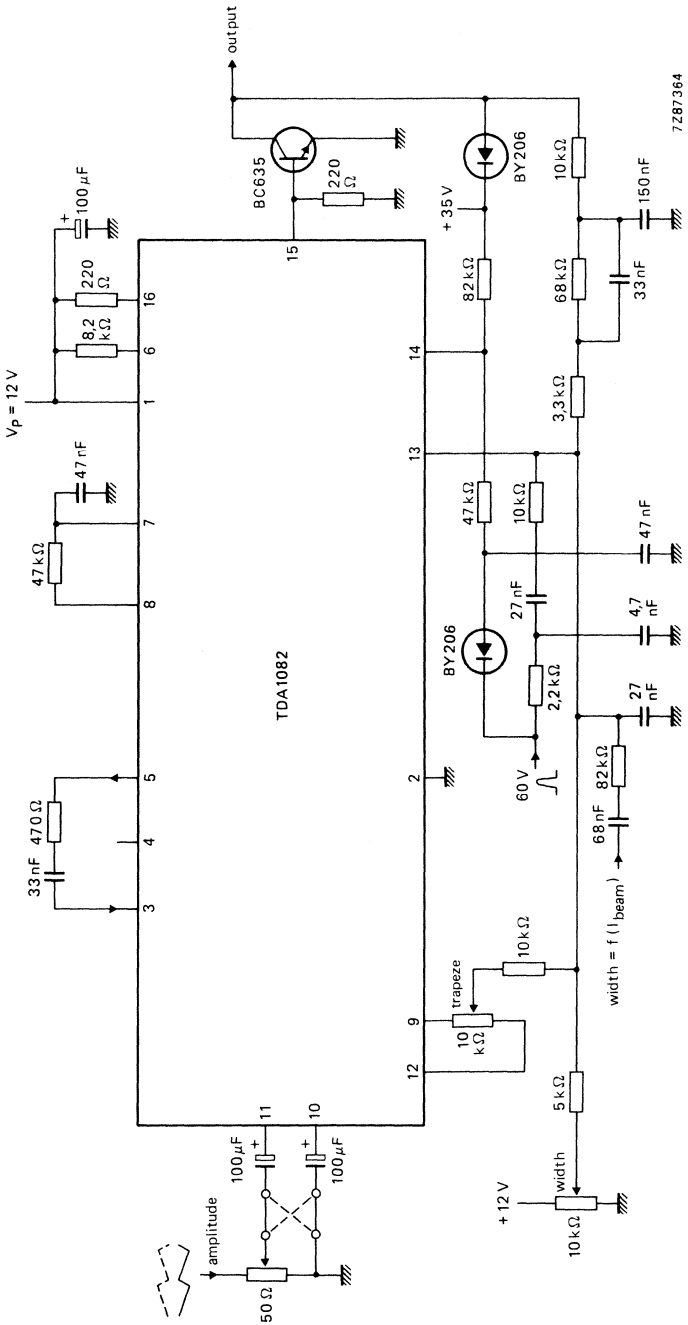


Fig. 2 Application circuit E-W-correction (class-D operation).

12 to 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA
Output power at d_{tot} = 0,7%			
sine-wave power			
V_P = 25 V; R_L = 4 Ω	P_o	typ.	13 W
V_P = 25 V; R_L = 8 Ω	P_o	typ.	7 W
music power			
V_P = 32 V; R_L = 4 Ω	P_o	typ.	21 W
V_P = 32 V; R_L = 8 Ω	P_o	typ.	12 W
Closed-loop voltage gain (externally determined)	G_c	typ.	30 dB
Input resistance (externally determined)	R_i	typ.	20 kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	72 dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50 dB

PACKAGE OUTLINES

TDA1512: 9-lead SIL; plastic power (SOT-131).
TDA1512Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157).

PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply (V_P)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

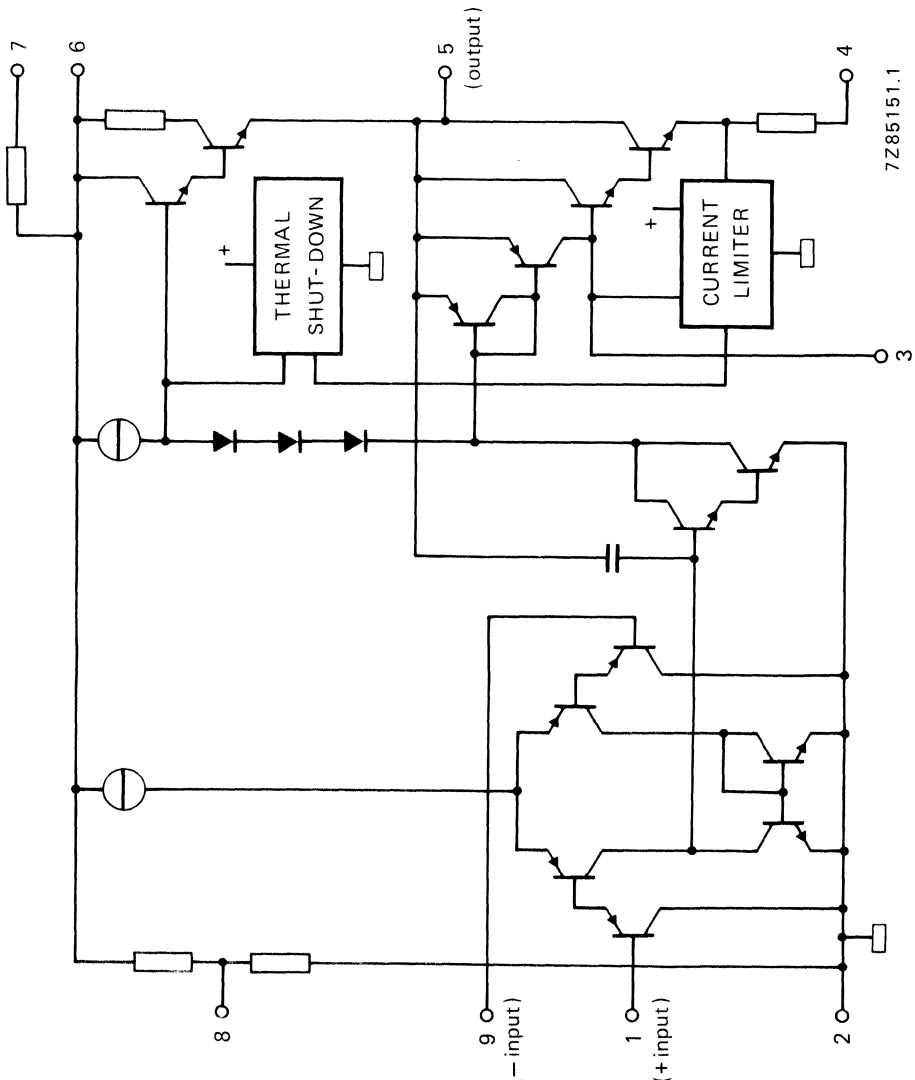


Fig. 1 Simplified internal circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Repetitive peak output current	I_{ORM}	max.	3,2 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100 hours

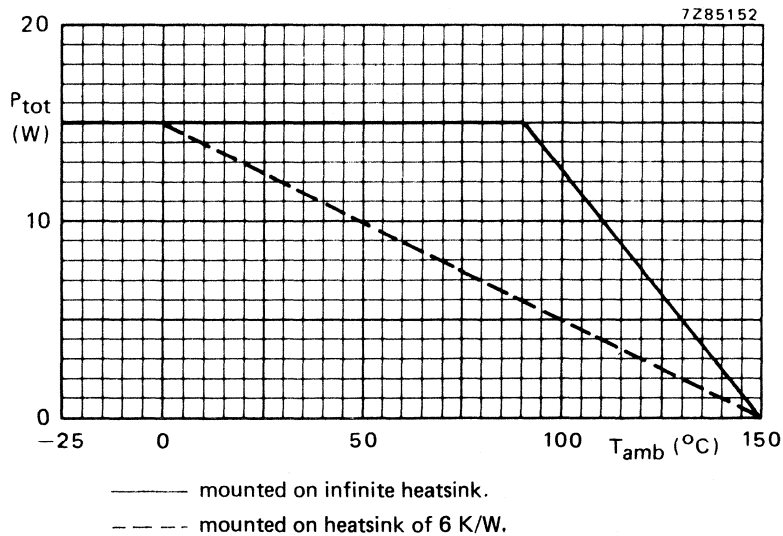


Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	typ.	3 K/W
		⩽	4 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA

A.C. CHARACTERISTICS

V_P = 25 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,7 %			
R_L = 4 Ω	P_o	typ.	13 W
R_L = 8 Ω	P_o	typ.	7 W
music power at V_P = 32 V			
R_L = 4 Ω; d_{tot} = 0,7 %	P_o	typ.	21 W
R_L = 4 Ω; d_{tot} = 10 %	P_o	typ.	25 W
R_L = 8 Ω; d_{tot} = 0,7 %	P_o	typ.	12 W
R_L = 8 Ω; d_{tot} = 10 %	P_o	typ.	15 W
Power bandwidth; −1,5 dB; d_{tot} = 0,7%	B		40 Hz to 16 kHz
Voltage gain			
open-loop	G_o	typ.	74 dB
closed-loop	G_c	typ.	30 dB
Input resistance (pin 1)	R_i	>	100 kΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20 kΩ
Input sensitivity			
for P_o = 50 mW	V_i	typ.	16 mV
for P_o = 10 W	V_i	typ.	210 mV
Signal-to-noise ratio			
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	>	68 dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	76 dB
Ripple rejection at f = 100 Hz	RR	typ.	50 dB
Total harmonic distortion at P_o = 10 W	d_{tot}	typ. <	0,1 % 0,3 %
Output resistance (pin 5)	R_o	typ.	0,1 Ω

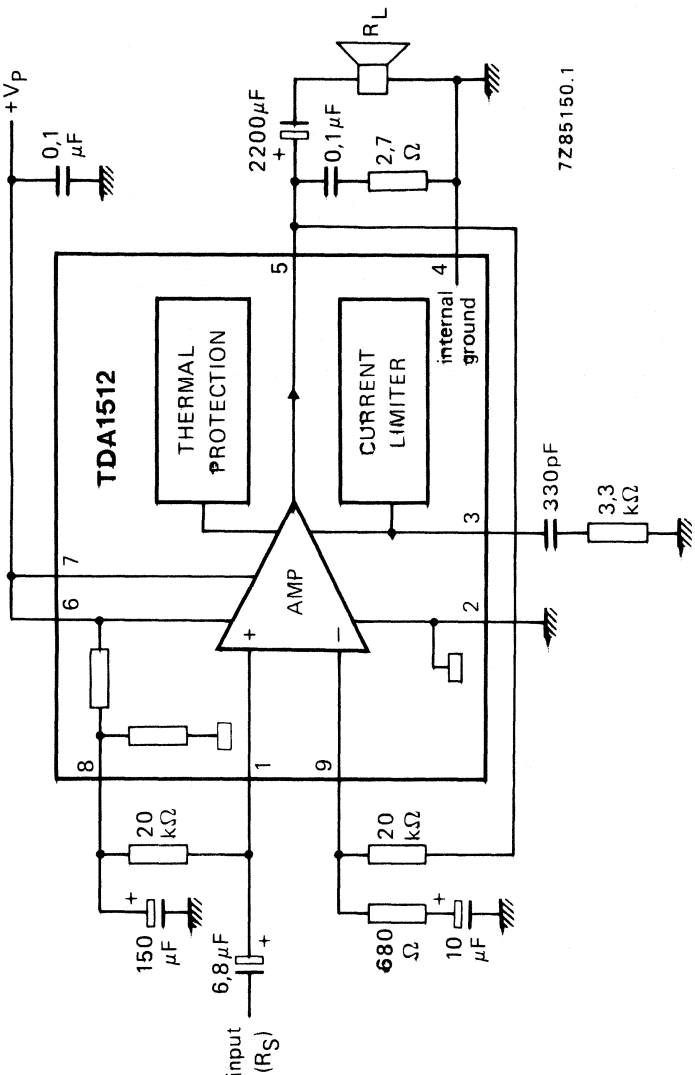


Fig. 3 Test circuit.

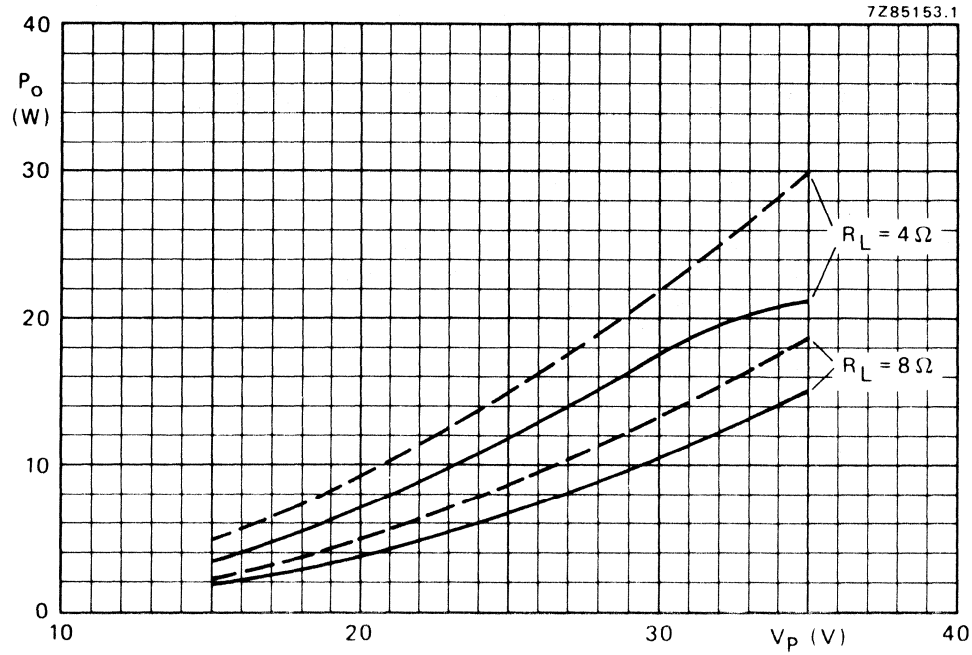


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz;
——— d_{tot} = 0,7 %; – – – d_{tot} = 10 %.

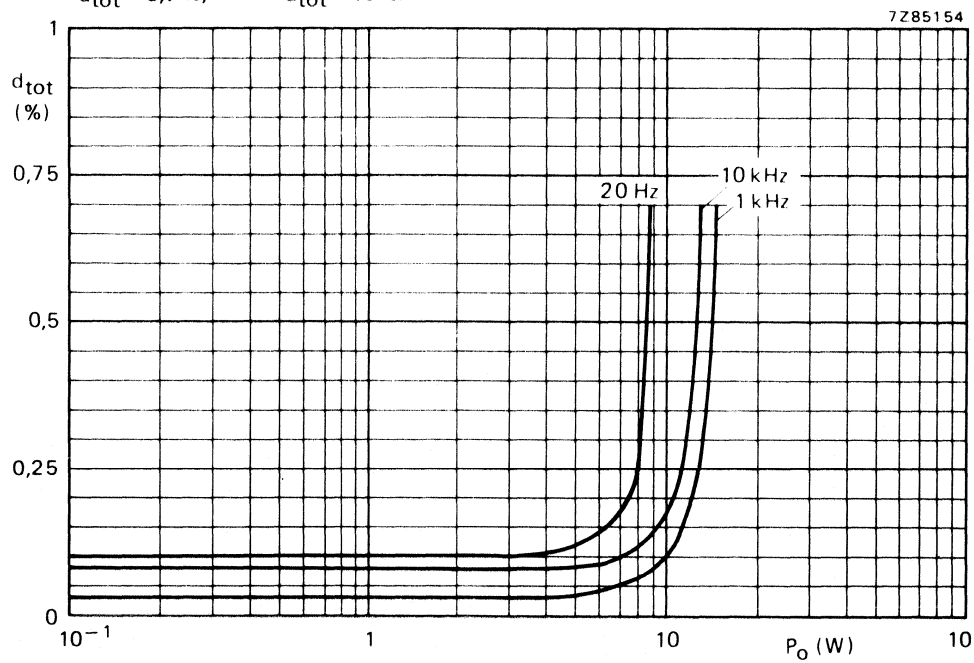


Fig. 5 Total harmonic distortion as a function of the output power.

20 WATT HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1520B is an integrated hi-fi audio power amplifier designed for use with non-stabilized symmetrical or stabilized asymmetrical power supplies in mains-fed applications (e.g. stereo radio, stereo TV sound and cassette recorder).

FEATURES

- Low offset voltage at output (suitable for BTL application)
- Low cross-over and secondary cross-over distortion
- Low intermodulation and transient intermodulation distortion
- Low harmonic distortion
- Good hum suppression
- High slew rate
- No switch-on/switch-off plop
- Thermal protection

QUICK REFERENCE DATA (note 1)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	15	–	50	V
Total quiescent current		I_{tot}	22	60	105	mA
Output power at THD = 0,5%		P_o	20	22	–	W
Input impedance		Z_I	1000	–	–	kΩ
Signal plus noise to noise ratio at P_O = 50 mW	note 2	(S+N)/N	70	75	–	dB
Supply voltage ripple rejection at R_S = 0 Ω	f = 100 Hz	SVRR	45	60	–	dB
	f = 10 kHz	SVRR	45	80	–	dB

Notes to the Quick Reference Data

1. All values measured from test circuit, Fig. 3 and V_P = 33 V; R_L = 4 Ω; f = 1 kHz and T_{amb} = 25 °C; unless otherwise specified.
2. Bandwidth is 20 Hz to 20 kHz and R_S = 2 kΩ (r.m.s. value).

PACKAGE OUTLINE

9-lead SIL; plastic power (SOT-131).

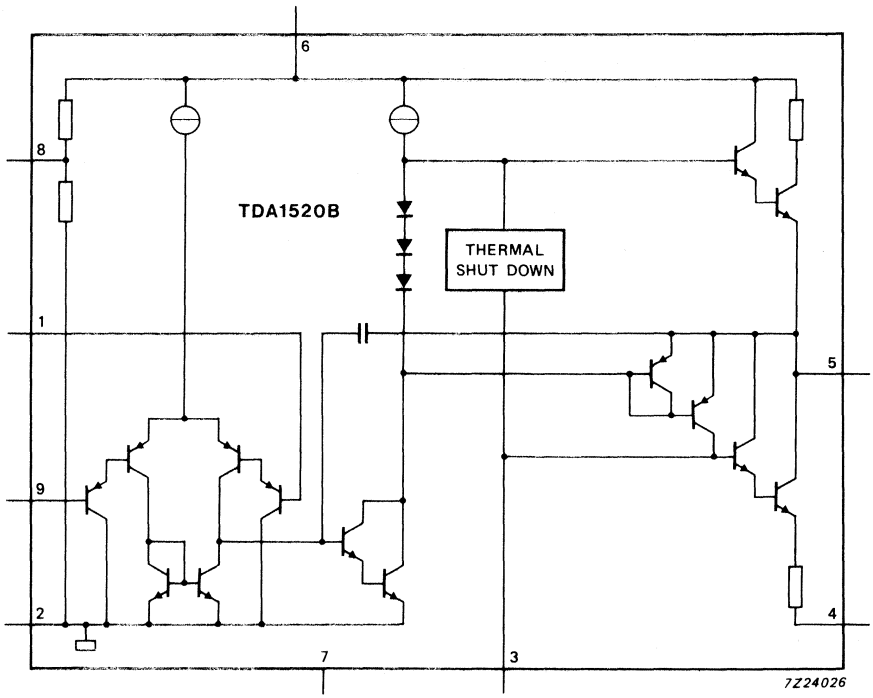


Fig. 1 Block diagram.

PINNING

1 Non-inverting input
2 Input ground (substrate)
3 Compensation
4 Negative supply (ground)
5 Output
6 Positive supply (V_P)
7 Not connected
8 Supply voltage ripple rejection
9 Inverting input (feedback)

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	note 1	V_P	–	50	V
Repetitive peak output current		I_{ORM}	–	4	A
Non-repetitive peak output current	note 2	I_{OSM}	–	5	A
Total power dissipation		P_{tot}	see Fig. 2		
AC short-circuit time of the load impedance during signal drive at					
$V_P = \pm 20$ V	symmetrical supply; $R_S = 2\ \Omega$; $f = \geqslant 20$ Hz	T_{sc}	–	60	s
$V_P = 30$ V	asymmetrical supply; $R_S = 4\ \Omega$	T_s	–	60	s
Operating ambient temperature range		T_{amb}	–	150	°C
Storage temperature range		T_{stg}	−65	+ 150	°C

Notes to the Ratings

1. Minimum rise time of the supply must be $\geqslant 20$ ms.
2. Maximum peak current is defined by the internal protection circuits.

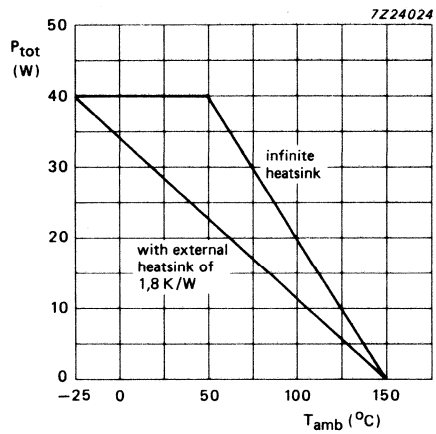


Fig. 2 Power derating curve.

POWER DISSIPATION AND HEATSINK INFORMATION

The maximum theoretical power dissipation with a stabilized power supply is (V_P = 33 V and R_L = 4 Ω):

$$\frac{V_P^2}{2\pi^2 R_L} = 13{,}8 \text{ W}.$$

Worst case power dissipation with a non-stabilized power supply is (regulation factor of 15%; over voltage of 10% and R_L min. = 0,8 x R_L typ.; V_{PL} is the loaded supply voltage):

$$\frac{(1{,}1 \times V_{PL})^2}{2\pi^2 R_L \text{ min.}} = 23{,}4 \text{ W}.$$

With a maximum ambient temperature of 50 °C and a maximum crystal temperature of 150 °C, the required thermal resistance is:

$$R_{th\,j\text{-}a} = \frac{150 - 50}{23{,}4} = 4{,}3 \text{ K/W}.$$

The thermal resistance of the encapsulation is < 2,5 K/W, therefore the thermal resistance of the heatsink must be < 1,8 K/W.

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified; measured from test circuit, Fig. 3.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	15	–	50	V
Total quiescent current		I_P	22	60	105	mA
Peak output current		I_{OM}	–	–	3,2	A
Power output at THD = 0,5%	note 1	P_O	20	22	–	W
Total harmonic distortion at P_O = 12 W	note 1	THD	–	0,01	0,1	%
Power bandwidth at THD = 0,5%	P_O = 50 mW to 10 W	B	–	20 to 20 000	–	Hz
Input voltage at P_O = 20 W	note 2	V_I	225	290	325	mV
Input impedance	note 3	Z_I	1000	–	–	kΩ
Signal plus noise to noise ratio at P_O at 50 mW	note 4	(S+N)/N	70	75	–	dB
Offset voltage		$\lvert V_{5-8} \rvert$	0	± 10	± 100	mV
Input offset current		I_{os}	–	0	1	μA
Output impedance		Z_O	–	–	0,1	Ω
Supply voltage ripple rejection at R_S = 0 Ω	f = 100 Hz	SVRR	45	60	–	dB
	f = 10 kHz	SVRR	45	80	–	dB
Intermodulation distortion at P_O = 10 W		d_{IM}	–	0,02	–	%
Transient intermodulation distortion	note 5	d_{TIM}	–	0,01	–	%
Slew rate		SR	–	6	–	V/μs

Notes to the Characteristics

1. Output power is measured directly at the output pin.
2. The closed-loop gain is determined by external resistors and is variable between 20 to 40 dB.
3. Input impedance in the test circuit is determined by the bias resistor R.
4. Unweighted noise measured in a bandwidth of 20 Hz to 20 kHz at R_S = 2 kΩ.
5. The transient intermodulation distortion is measured at P_O = 10 W. The input signal is a 3,18 kHz square-wave signal mixed with a 15 kHz sine-wave signal and a peak-to-peak voltage ratio of 4:1.

APPLICATION INFORMATION

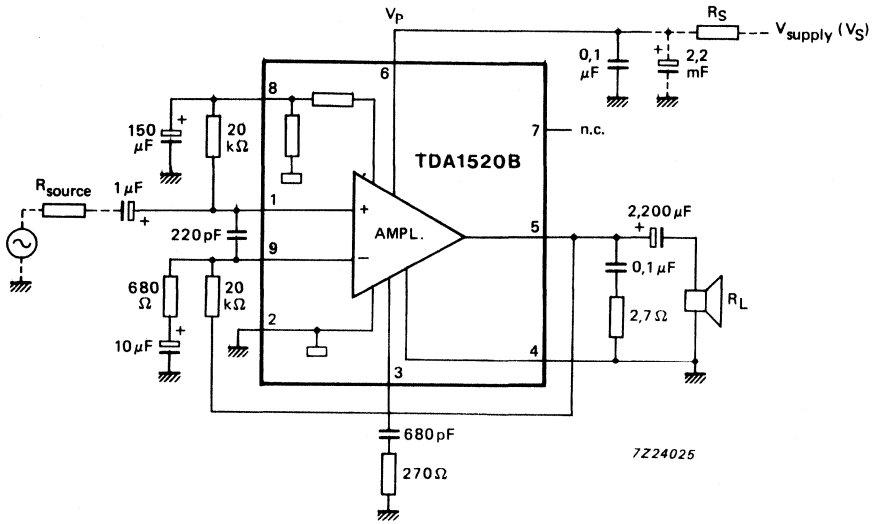


Fig. 3 Test and application diagram.

2 x 12 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521/TDA1521Q is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 16 V	P_O	typ. 12	W
Voltage gain	G_v	typ. 30	dB
Gain balance between channels	ΔG_v	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINES

TDA1521: 9-lead single in-line; plastic power (SOT-131).
TDA1521Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157).

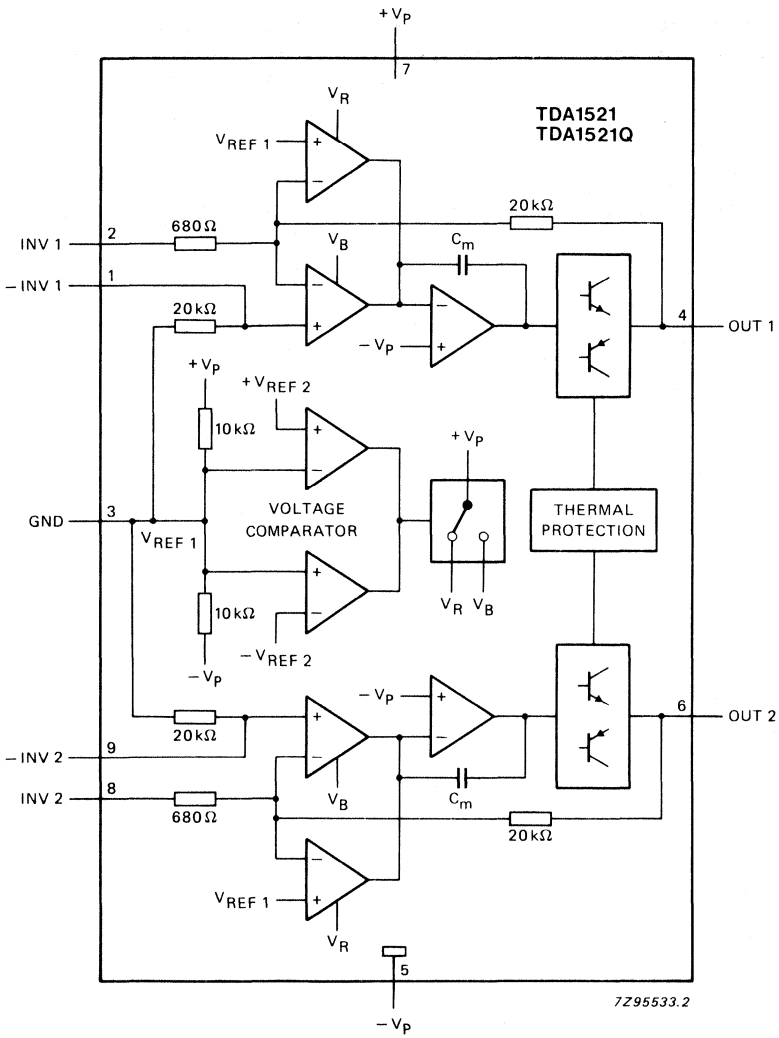


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ V_P (asymmetrical)
4	OUT1	output 1
5	$-V_P$	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	$+V_P$	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 12 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 16 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 13, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+ 20	V
	pin 5	$-V_P = V_{5-3}$	–	−20	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	−65	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply; $V_P < 32$ V (unloaded); $R_i \geqslant 4\ \Omega$	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_i) > 4 Ω, the maximum unloaded supply voltage is increased to 32 V.

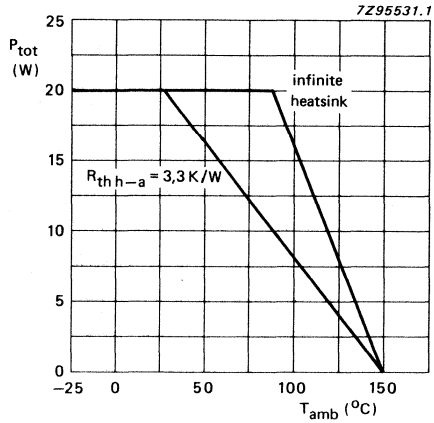


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c}$ = 2,5 K/W

HEATSINK DESIGN EXAMPLE

With derating of 2,5 K/W, the value of heatsink thermal resistance is calculated as follows:

given R_L = 8 Ω and V_P = ±16 V, the measured maximum dissipation is 14,6 W; then, for a maximum ambient temperature of 65 °C, the required thermal resistance of the heatsink is

$$R_{th\ h\text{-}a} = \frac{150 - 65}{14{,}6} - 2{,}5 = 3{,}3\ \text{K/W}$$

Note: The internal metal block (heatsink) has the same potential as pin 5 (−V_P)

DEVELOPMENT DATA

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 16,0	± 20,0	V
input mute mode		V_P	± 2,0	–	± 5,5	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 16 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	10	12	–	W
	THD = 10%	P_o	12	15	–	W
Total harmonic distortion	P_o = 6 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 13; V_S = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	40	50	–	dB
Channel separation	R_S = 0 Ω	α	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\,max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

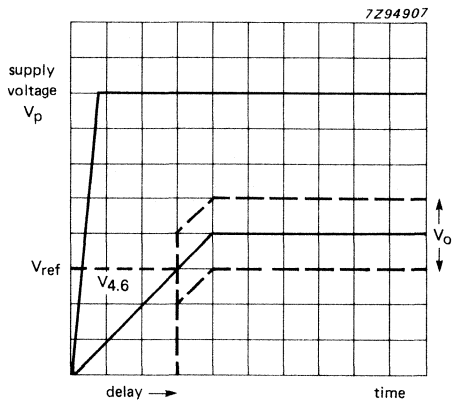


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

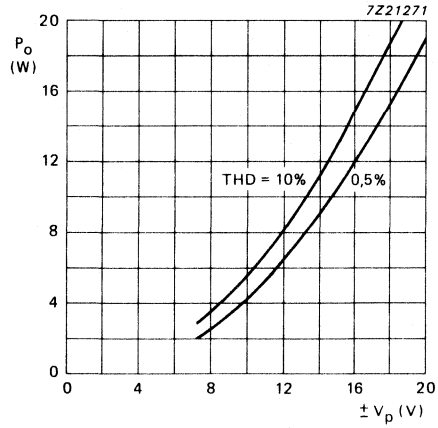


Fig. 4 Output power as a function of supply voltage, symmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

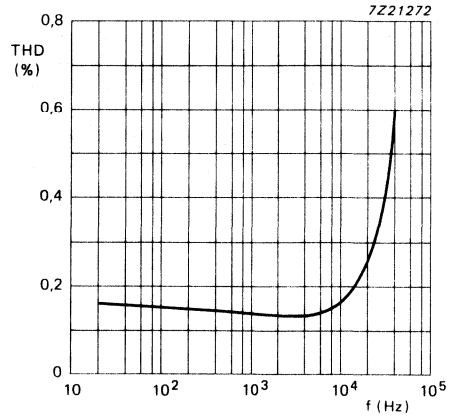


Fig. 5 Distortion as a function of frequency; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; $P_O = 6$ W.

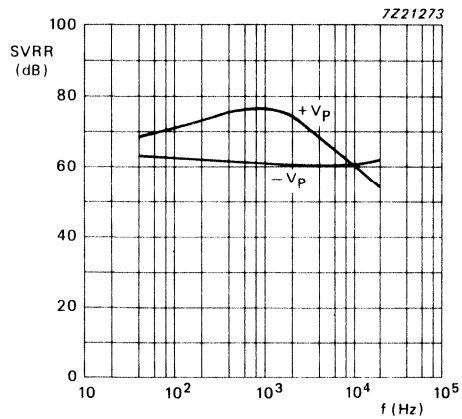


Fig. 6 Supply voltage ripple rejection; symmetrical supply; $V_P = \pm 16$ V; $V_{RR} = 200$ mV.

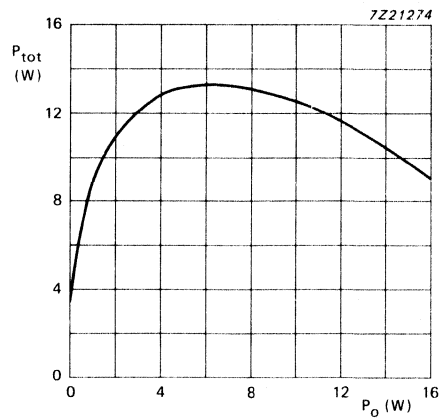


Fig. 7 Power dissipation as a function of output power; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; f = 1 kHz.

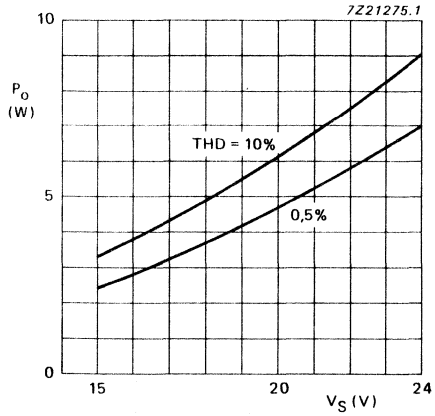


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; R_L = 8 Ω; f = 1 kHz.

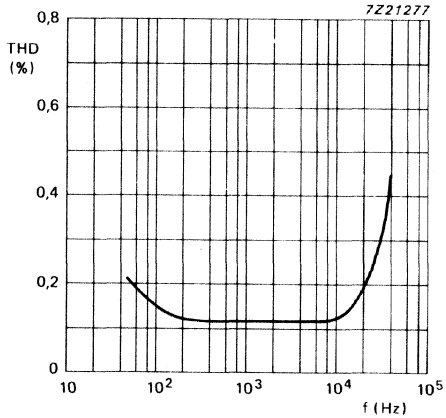


Fig. 9 Distortion as a function of frequency; asymmetrical supply; V_S = 24 V; R_L = 8 Ω; P_o = 4 W.

DEVELOPMENT DATA

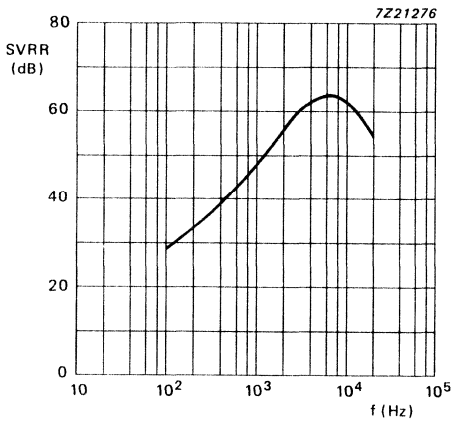


Fig. 10 Supply voltage ripple rejection; asymmetrical supply; V_S = 24 V; V_{RR} = 200 mV.

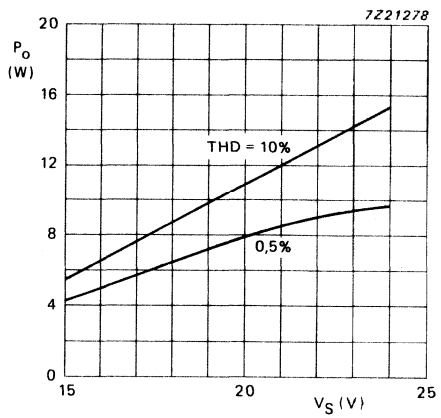
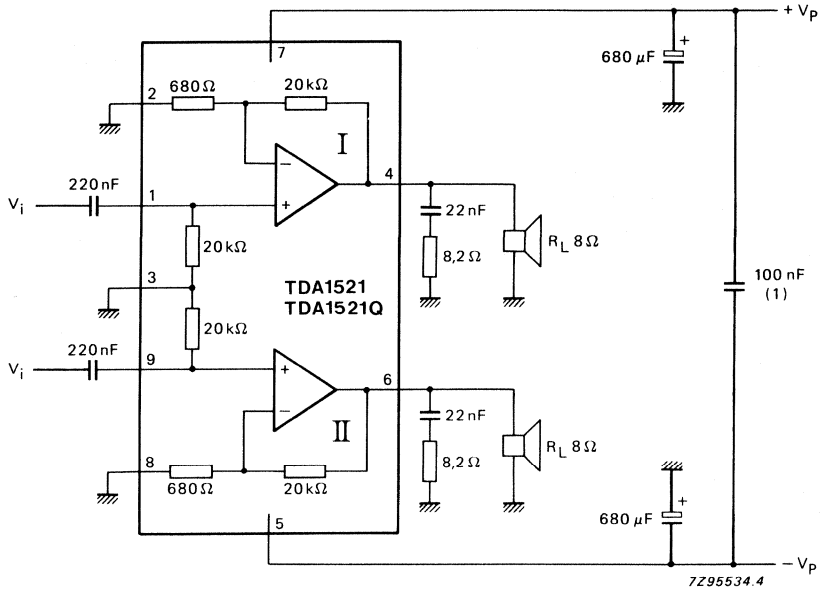
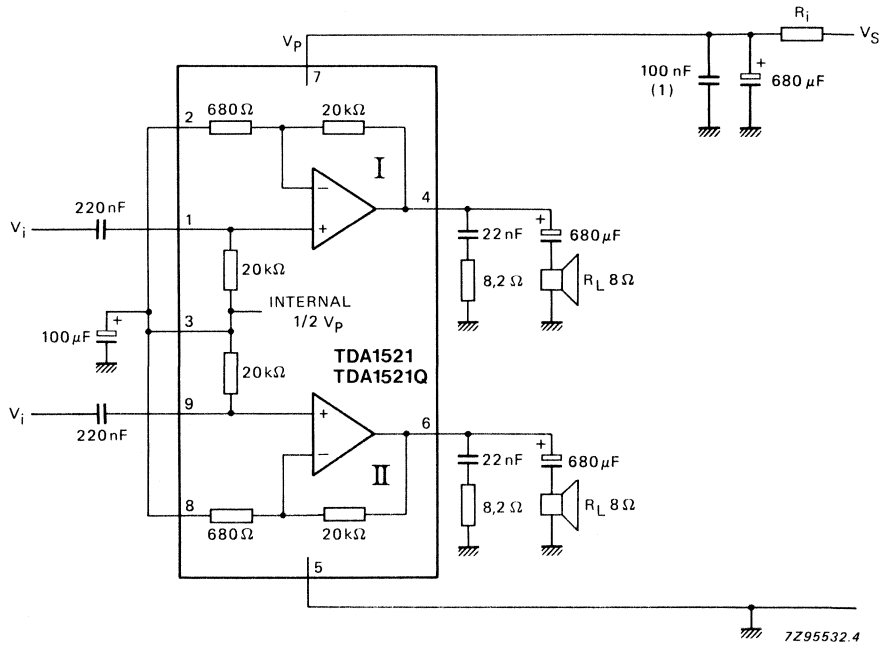


Fig. 11 Output power as a function of supply voltage; asymmetrical supply; R_L = 4 Ω; f = 1 kHz.



1 To be connected as close as possible to the IC

Fig. 12 Test and application circuit; symmetrical power supply.



1 To be connected as close as possible to the IC

Fig. 13 Test and application circuit; asymmetrical power supply.

2 x 6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521A is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 12 V	P_O	typ. 6	W
Voltage gain	G_V	typ. 30	dB
Gain balance between channels	ΔG_V	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINE

TDA1521A: 9-lead single in-line; plastic power (SOT-110B).

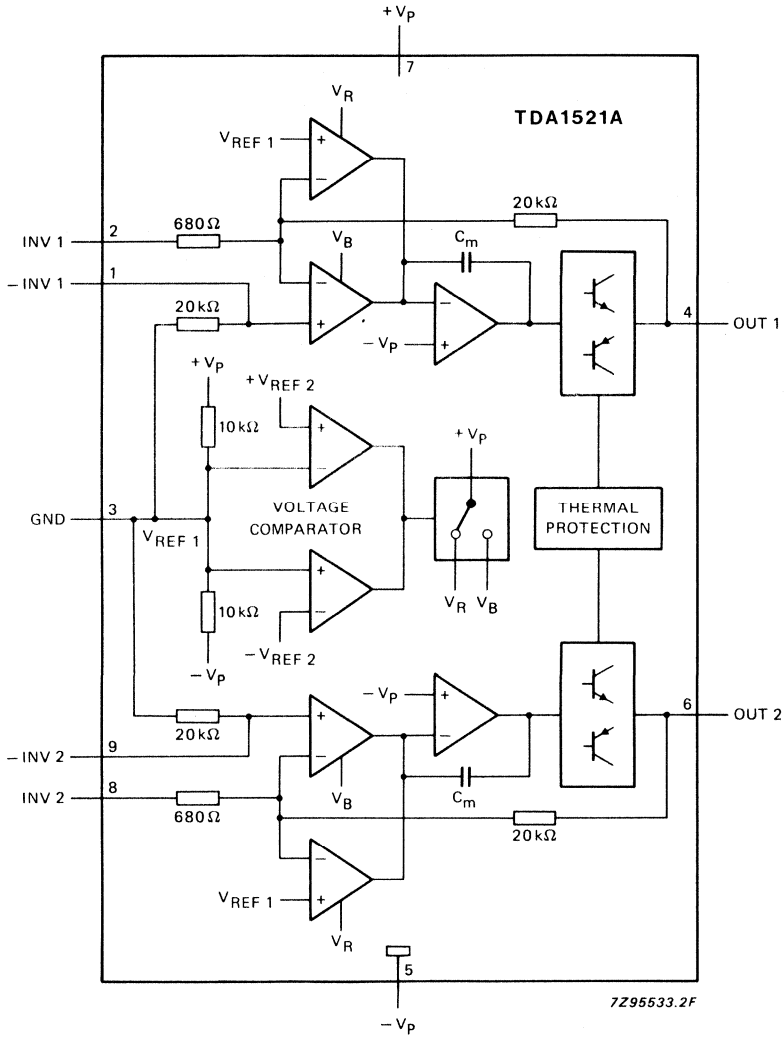


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ VP (asymmetrical)
4	OUT1	output 1
5	–VP	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	+ VP	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 12 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 12, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+ 20	V
	pin 5	$-V_P = V_{5-3}$	–	−20	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	−65	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V.

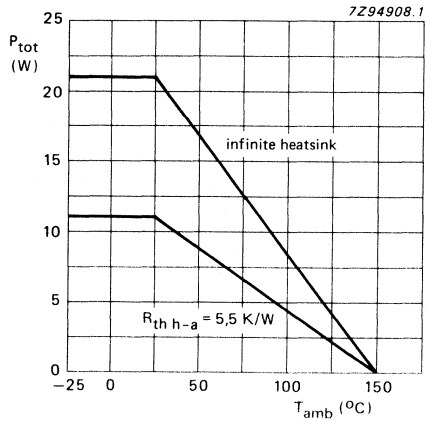


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j-c} = 6$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 6 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = \pm 12$ V, the measured maximum dissipation is 7,8 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is

$$R_{th\ h-a} = \frac{150 - 60}{7,8} - 6 = 5,5\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 ($-V_P$).

DEVELOPMENT DATA

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 12,0	± 20,0	V
input mute mode		V_P	± 2,0	–	± 5,5	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 12 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 12; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	40	50	–	dB
Channel separation	R_S = 0 Ω	α	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

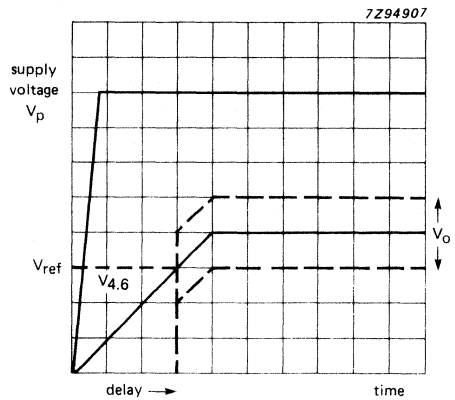


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

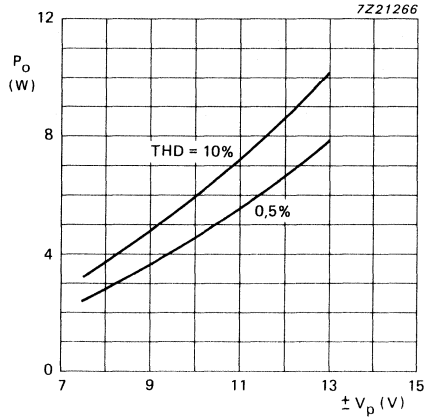


Fig. 4 Output power as a function of supply voltage; symmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

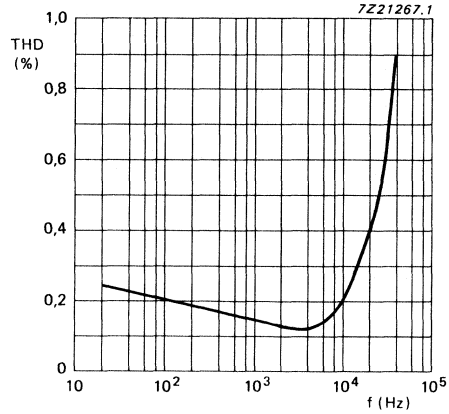


Fig. 5 Distortion as a function of frequency; symmetrical supply; $V_p = \pm 12$ V; $R_L = 8\ \Omega$; $P_o = 3$ W.

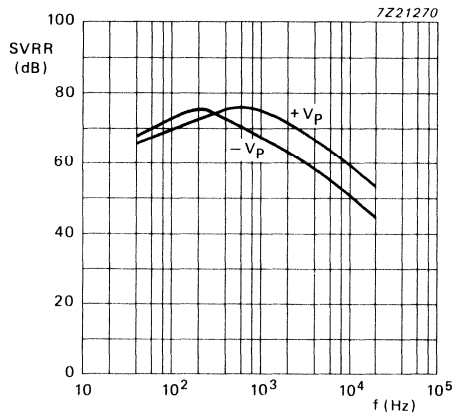


Fig. 6 Supply voltage ripple rejection; symmetrical supply, $V_P = \pm 12$ V; $V_{RR} = 200$ mV.

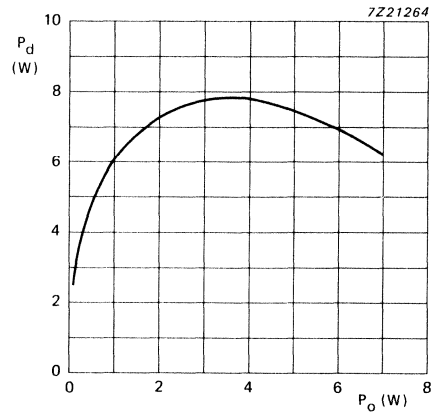


Fig. 7 Power dissipation as a function of output power; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; f = 1 kHz.

APPLICATION INFORMATION (continued)

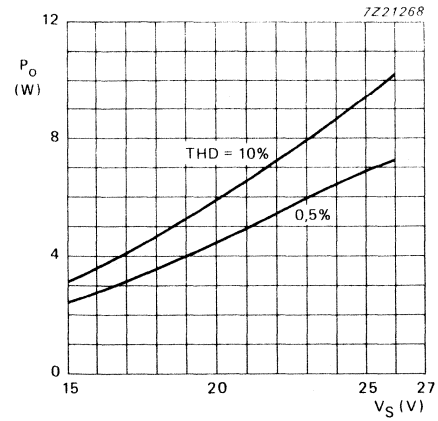


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

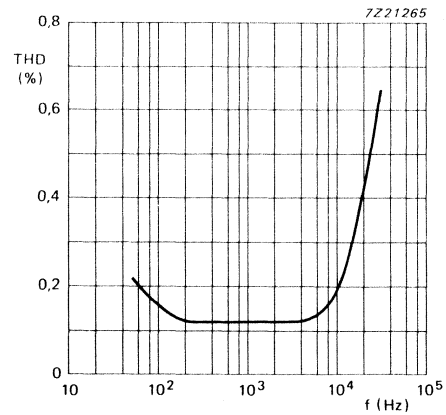


Fig. 9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; $P_O = 3$ W.

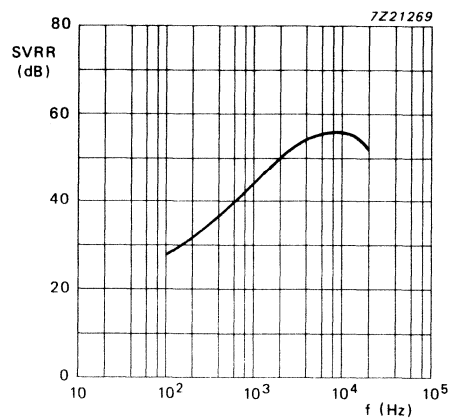
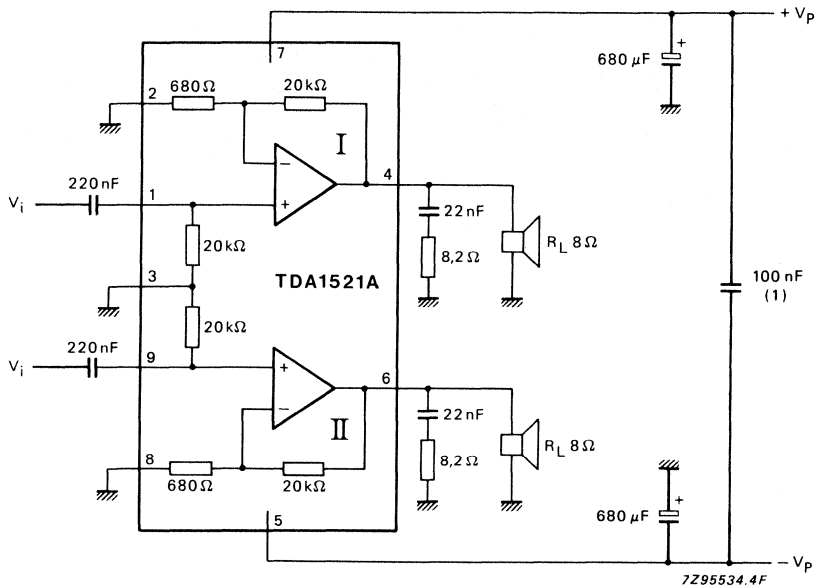


Fig. 10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mW.

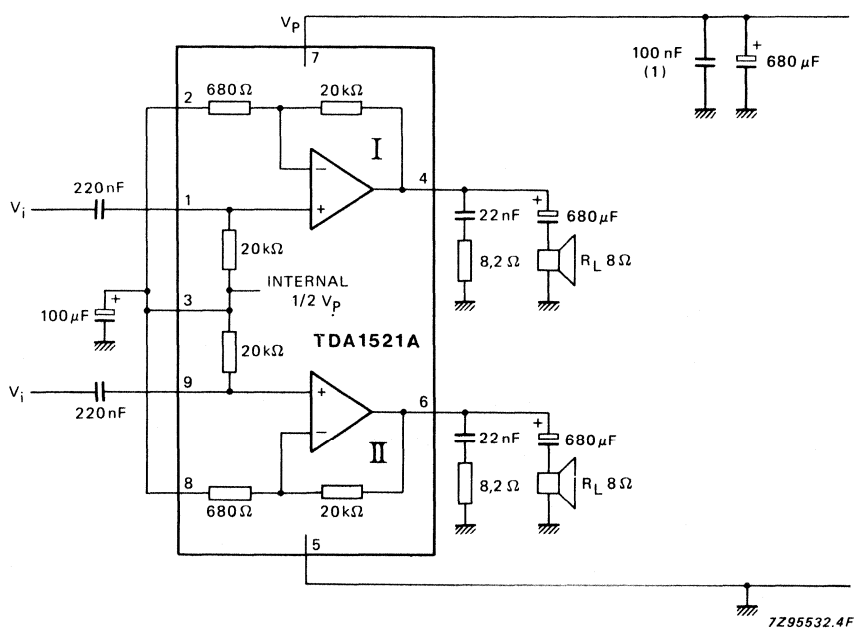
DEVELOPMENT DATA

APPLICATION INFORMATION (continued)



(1) To be connected as close as possible to the I.C.

Fig. 11 Test and application circuit; symmetrical power supply.



(1) To be connected as close as possible to the I.C.

Fig. 12 Test and application circuit; asymmetrical power supply.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

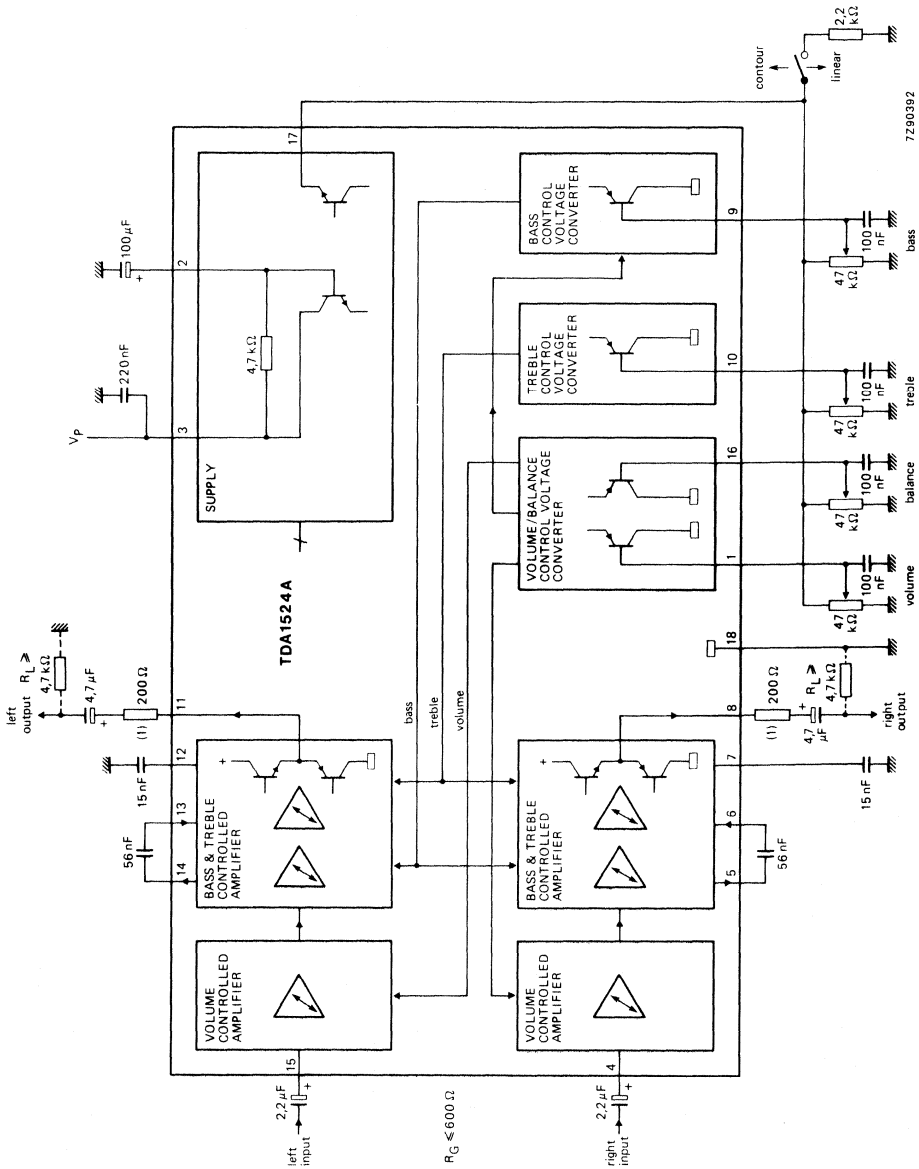
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	typ.	12 V
Supply current (pin 3)	$I_P = I_3$	typ.	35 mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5 V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3 V
Volume control range	G_v		−80 to + 21,5 dB
Bass control range at 40 Hz	ΔG_v		−19 to + 17 dB
Treble control range at 16 kHz	ΔG_v	typ.	± 15 dB
Total harmonic distortion	THD	typ.	0,3 %
Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; V_P = 12 V;			
for max. voltage gain	$V_{no(rms)}$	typ.	310 μV
for voltage gain G_v = −40 dB	$V_{no(rms)}$	typ.	100 μV
Channel separation at G_v = −20 to + 21,5 dB	α_{cs}	typ.	60 dB
Tracking between channels at G_v = −20 to + 26 dB	ΔG_v	max.	2,5 dB
Ripple rejection at 100 Hz	RR	typ.	50 dB
Supply voltage range (pin 3)	$V_P = V_{3\text{-}18}$		7,5 to 16,5 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102H).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

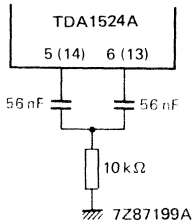


Fig. 2 Double-pole low-pass filter for improved bass-boost.

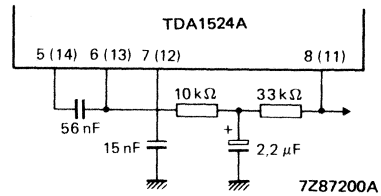


Fig. 3 D.C. feedback with filter network for improved signal handling.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	max.	20 V
Total power dissipation	P_{tot}	max.	1200 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

D.C. CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7,5	–	16,5	V
Supply current					
at V_P = 8,5 V	$I_P = I_3$	19	27	35	mA
at V_P = 12 V	$I_P = I_3$	25	35	45	mA
at V_P = 15 V	$I_P = I_3$	30	43	56	mA
D.C. input levels (pins 4 and 15)					
at V_P = 8,5 V	$V_{4,15-18}$	3,8	4,25	4,7	V
at V_P = 12 V	$V_{4,15-18}$	5,3	5,9	6,6	V
at V_P = 15 V	$V_{4,15-18}$	6,5	7,3	8,2	V
D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3)					
at V_P = 8,5 V	$V_{8,11-18}$	3,3	4,25	5,2	V
at V_P = 12 V	$V_{8,11-18}$	4,6	6,0	7,4	V
at V_P = 15 V	$V_{8,11-18}$	5,7	7,5	9,3	V
Pin 17					
Internal potentiometer supply voltage at V_P = 8,5 V	V_{17-18}	3,5	3,75	4,0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0,5	mA
linear (switch closed)	$-I_{17}$	1,5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10{,}8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4,5	–	$V_P/2-V_{BE}$	V
D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at V_{17-18} = 5 V	$V_{1,9,10,16}$	1,0	–	4,25	V
using internal supply	$V_{1,9,10,16}$	0,25	–	3,8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

A.C. CHARACTERISTICS

$V_P = V_{3-18} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Max. gain of volume (Fig. 5)	$G_{V\,max}$	20,5	21,5	23	dB
Volume control range; $G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range; $G_V = 0$ dB (Fig. 6)	ΔG_V	–	–40	–	dB
Bass control range at 40 Hz (Fig. 7)	ΔG_V	–	–19 to + 17 ± 3		dB
Treble control range at 16 kHz (Fig. 8)	ΔG_V	–	± 15 ± 3	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: $G_V = 20$ dB	$R_{i4,15}$	10	–	–	kΩ
$G_V = -40$ dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; $G_V = 0$ dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at $G_V = -20$ to + 21,5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0{,}5\ V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0{,}5\ V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1,5	dB
Tracking between channels					
for $G_V = 21{,}5$ to –26 dB					
f = 250 Hz to 6,3 kHz; balance adjusted at					
$G_V = 10$ dB	ΔG_V	–	–	2,5	dB

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with d.c. feedback (Fig. 3)					
Input signal handling					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 8,5 V; THD = 0,7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,8	2,4	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 12 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 15 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
Output signal handling (note 2 and note 3)					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	1,8	2,0	–	V
at V_P = 8,5 V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	–	2,2	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	2,5	3,0	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	–	3,5	–	V
Noise performance (V_P = 8,5 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	260	–	μV
for G_v = –3 dB (note 4)	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	890	–	μV
for maximum emphasis of bass and treble (contour off; G_v = –40 dB)	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	310	–	μV
for G_v = –16 dB (note 4)	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	940	–	μV
for maximum emphasis of bass and treble (contour off; G_v = –40 dB)	$V_{no(m)}$	–	400	–	μV

parameter	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	350	–	μV
for G_V = 16 dB (note 4)	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN 45405					
of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	980	–	μV
for maximum emphasis of bass and treble					
(contour off; G_V = −40 dB)	$V_{no(m)}$	–	420	–	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ k\Omega}{1 + G_V}\ ;\ G_{V\ max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4,5 dB to r.m.s. values.

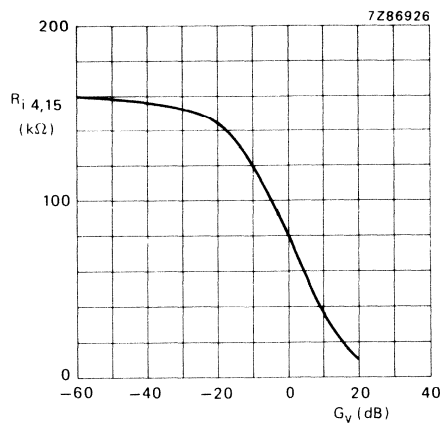


Fig. 4 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

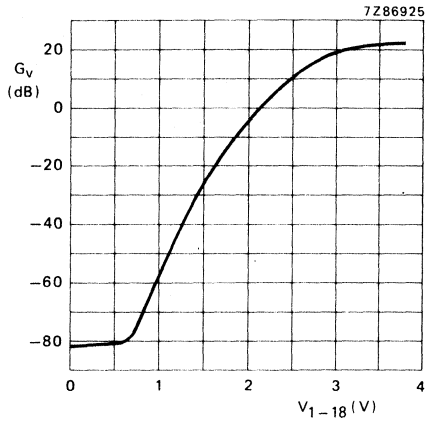


Fig. 5 Volume control curve; voltage gain (G_v) as a function of control voltage ($V_{1\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 1 kHz.

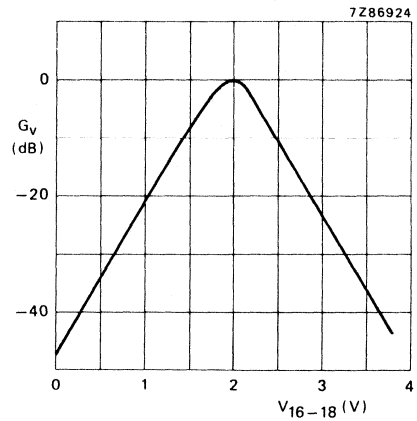


Fig. 6 Balance control curve; voltage gain (G_v) as a function of control voltage ($V_{16\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V.

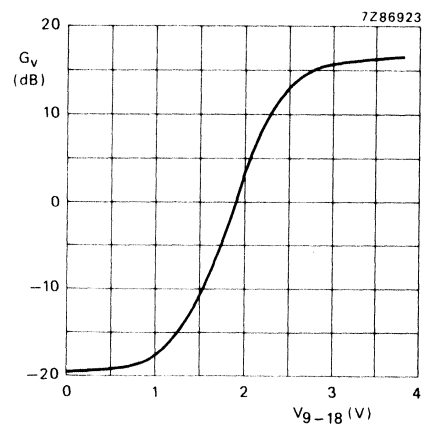


Fig. 7 Bass control curve; voltage gain (G_v) as a function of control voltage ($V_{9\text{-}18}$). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 40 Hz.

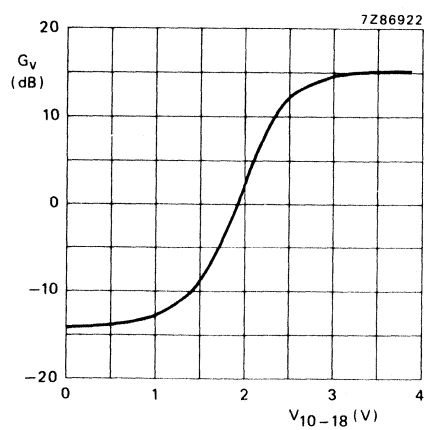


Fig. 8 Treble control curve; voltage gain (G_v) as a function of control voltage ($V_{10\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 16 kHz.

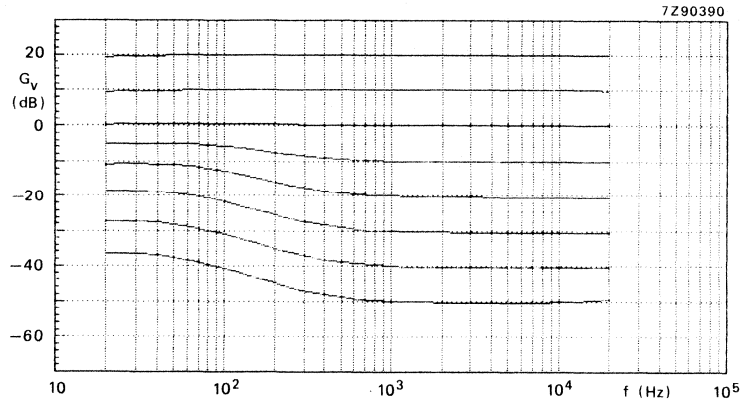


Fig. 9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

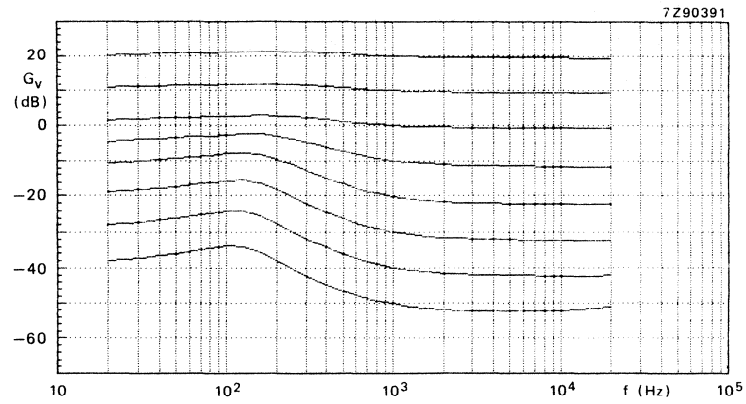


Fig. 10 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

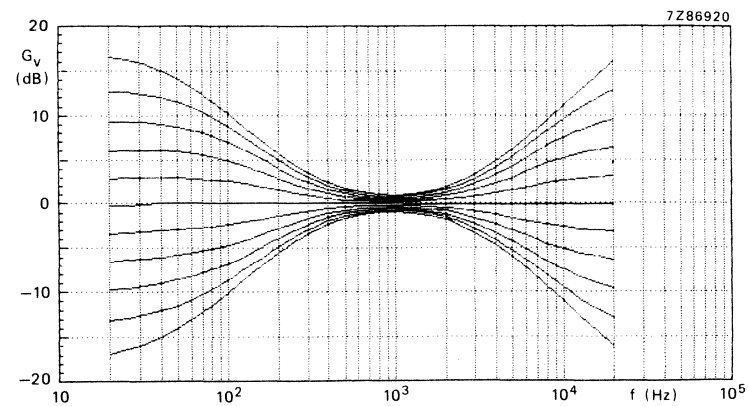


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

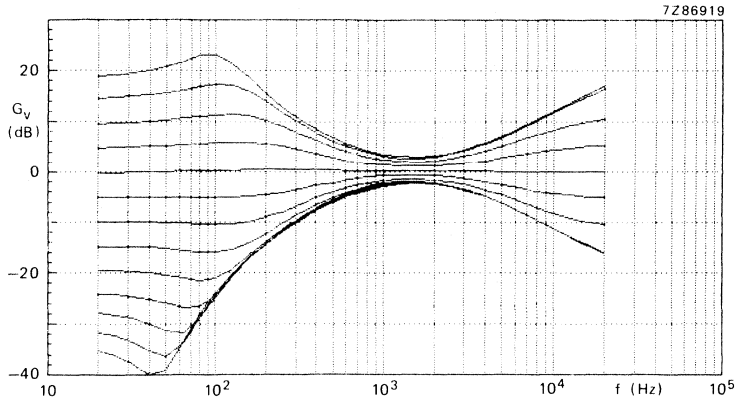


Fig. 12 Tone control frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

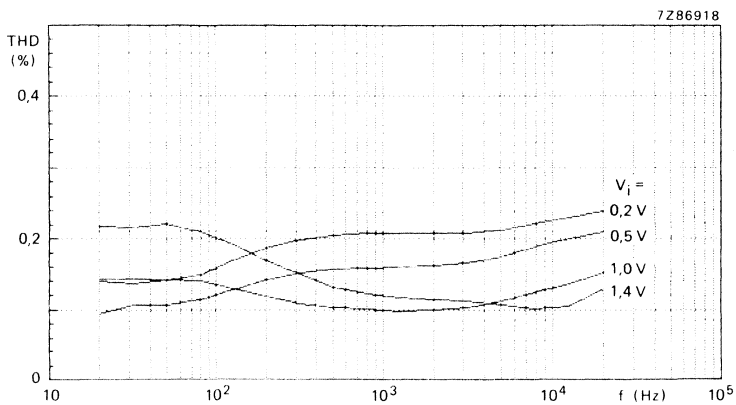


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; V_P = 8,5 V; volume control voltage gain at

$$G_v = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

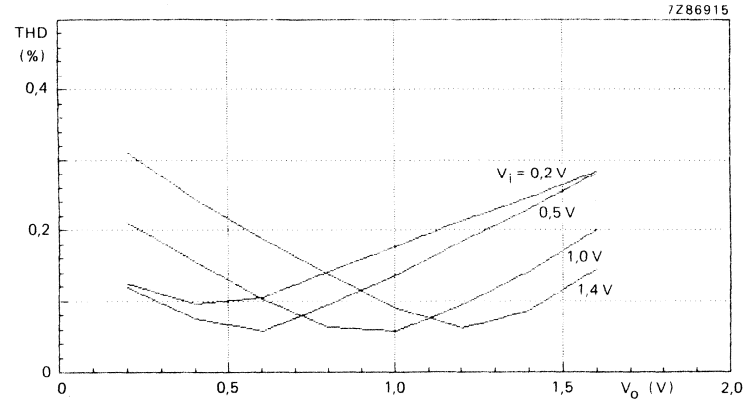
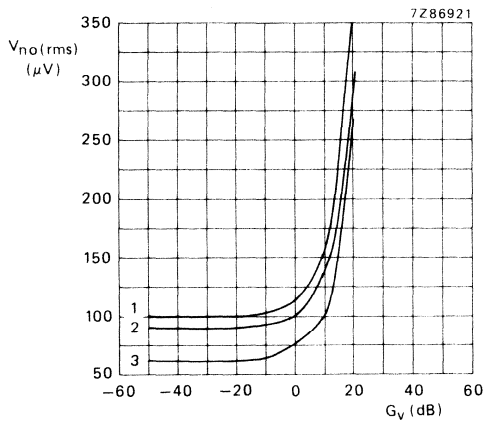


Fig. 14 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig. 1; V_P = 8,5 V; f_i = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8,5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

NOTES

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